ADDRESS SEQUENCING

Address Sequencing

- Each machine instruction is executed through the sequence of microinstructions.
- The collection of microinstructions which implements a particular machine instruction is called a *routine.*
- Each computer has it own microprogram routine in control memory to generate the microoperations.
- The CAR should contain the address of the first microinstruction to be executed.
- Sequential retrieval of microinstructions can be done by simply incrementing the current CAR contents and branching requires determining the desired Control Word address, and loading that into the CAR.

Address Sequencing

- The address sequencing capabilities required in a control memory are:

  1. Incrementing the CAR

  2. Unconditional branch or Conditional branch depending on the status bit condition.

  3. A mapping process from the bits of the instruction to the address for control memory.

  4. A facility for subroutine call and return.

Selection of address for Control memory
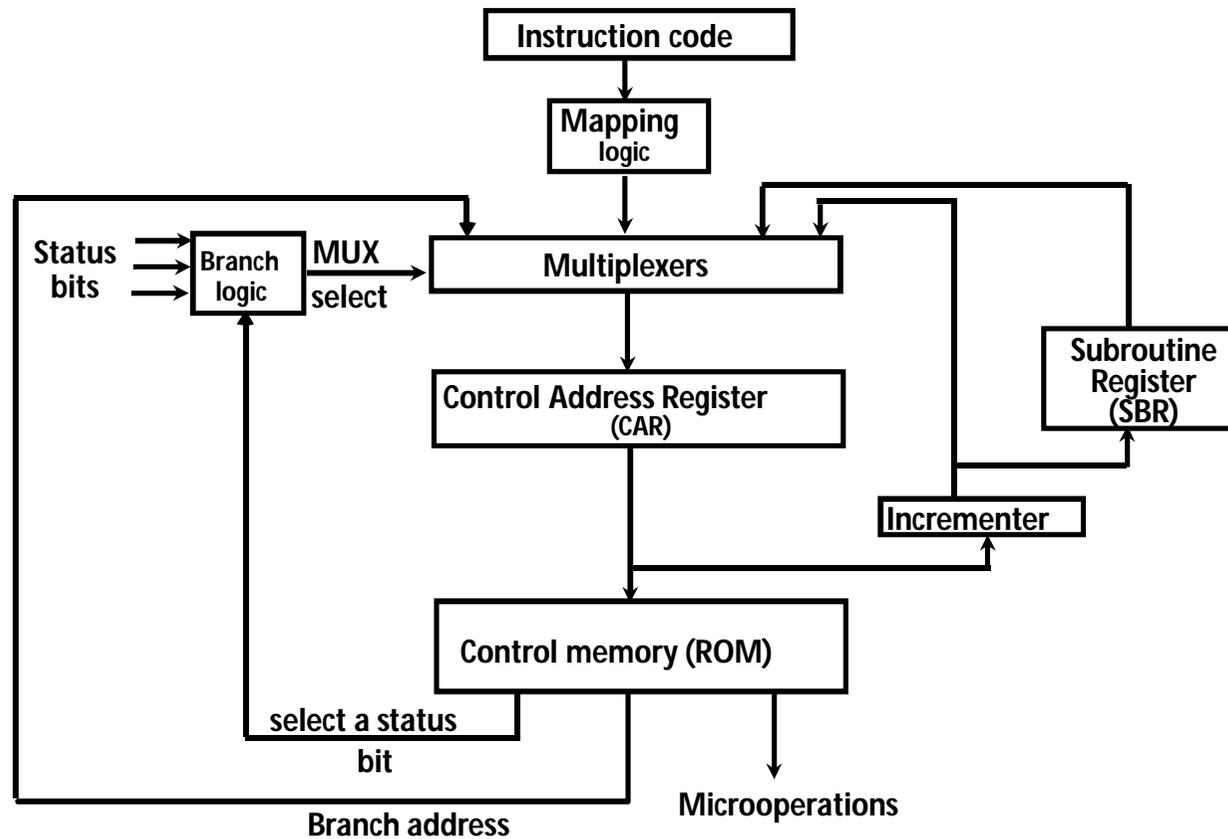
Selection of address for Control memory

- The diagram shows four different path from which the CAR receives the address.
- The incrementer increments the content of CAR by one to select the next microinstruction in sequence.
- Branching is achieved by specifying the branch address in one of the fields of the microinstruction.
- Conditional branching is obtained by using part of the microinstruction to select a specific status bit.
- An external address is transferred into control memory via mapping logic.
- The return address for subroutine is stored in a special register whose value is then used when the microprogram wishes to return from the subroutine.

Conditional Branching

- The status conditions are the specified bits in the system such as carry out of an adder, sign bit of a number, mode bit of the instruction and zero value at AC.

- Information in these bits are tested and action is initiated based on their condition.

- The branch logic H/W may be implemented by testing the specified condition and branching to the indicated address.

- If the status test condition is false, the control address register is incremented by one which can be implemented by incrementer.

- An unconditional branch microinstruction can be implemented by loading the branch address from control memory into CAR directly.

Subroutine

- Subroutine are the programs that are used by other routine to perform a particular task.
- Microprogram that uses subroutine must have a provision for storing the return address during the subroutine call.
- The subroutine register becomes the source for transferring the return address to the main program.
- The best way to structure the subroutine register is to use Last In First Out Stack.

Mapping Instruction

- Consider the computer with a simple instruction format as shown in following diagram:

	Opcode	Address
Machine Instruction	1 0 1 1	

Mapping Mask   0   x x x x   0 0

Microinstruction Address   0 1 0 1 1 0 0
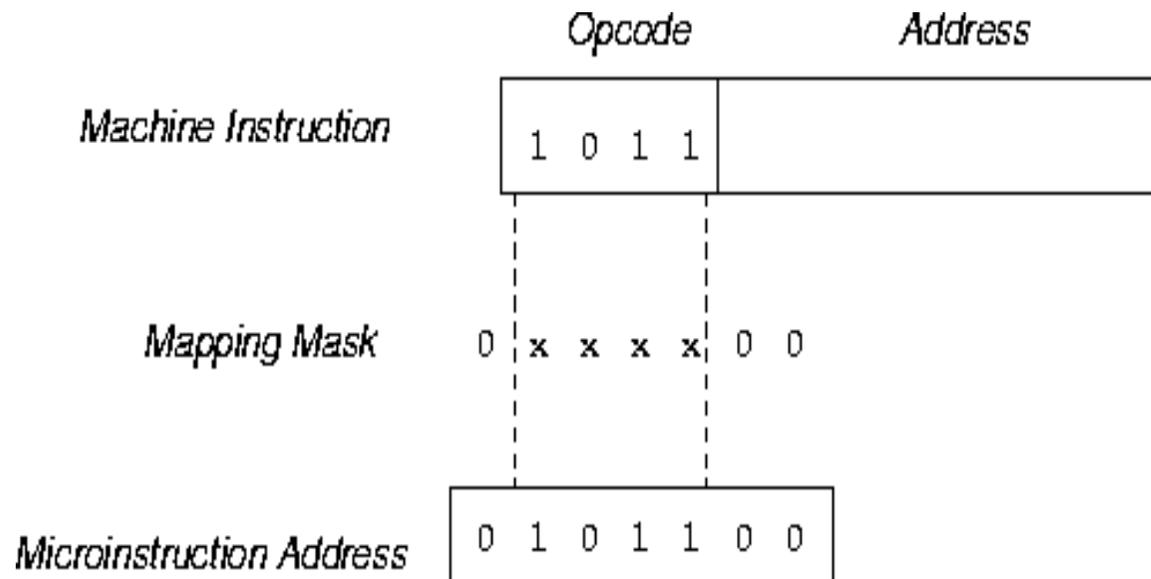
Mapping Instruction

- Assume that control memory has 128 bits. The mapping process converts the 4 bits opcode to a 7 bit address of control memory.

- This mapping consist of placing a 0 in the MSB of the address, transferring the 4 opcode bits and clearing 2 LSB of CAR to 0's.

- The bits of the instruction specify the address of a mapping ROM.

- The address of Control memory is given to CAR to fetch the microinstruction in the control memory.