SREENIVASA INSTITUTE of TECHNOLOGY and MANAGEMENT STUDIES
(autonomous)

(COMPUTER ORGANIZATION)

Question bank

II - B.TECH / II - SEMESTER regulation: r18

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SREENIVASA INSTITUTE OF TECHNOLOGY AND MANAGEMENT STUDIES

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

QUESTION BANK **COMPUTER ORGANIZATION (18CSE221)**

II B.Tech II Semester

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18CSE221 COMPUTER ORGANIZATION

Course Educational Objectives:

CEO 1: To conceptualize the basics of organizational and architectural issues of a digital computer.
CEO 2: To articulate design issues in the development of processor or other components that satisfy design requirements and objectives.
CEO 3: To study various data transfer techniques in digital computer and the design of control unit.
CEO 4: To learn the function of each element of a memory hierarchy and I/O devices.
CEO 5: To develop skill to apply the concept of Pipelining in designing multiprocessor system.

UNIT-1: BASIC STRUCTURE OF COMPUTERS

Computer Types - Functional Units - Basic Operational Concepts - Bus Structures – Software – Performance - Multiprocessors and Multi Computers - Data Representation- Fixed Point Representation - Floating Point Representation - Error Detection Codes.

UNIT-2: CPU DESIGN AND COMPUTER ARITHMETIC

CPU Design: Instruction Cycle - Memory Reference Instructions–Input/output and Interrupt - Addressing Modes - DATA Transfer and Manipulation - Program Control

Computer Arithmetic: Addition and Subtraction - Multiplication Algorithms - Division Algorithms - Floating Point Arithmetic Operations - Decimal Arithmetic Unit.

UNIT-3: REGISTER TRANSFER LANGUAGE AND DESIGN OF CONTROL UNIT

Register Transfer: Register Transfer Language - Register Transfer - Bus and Memory Transfers - Arithmetic Micro operations - Logic Micro Operations - Shift Micro Operations.

Control Unit: Control Memory - Address Sequencing–Micro program Example - Design of ControlUnit.

UNIT- 4: MEMORY AND INPUT/OUTPUT ORGANIZATION

Memory Organization: Memory Hierarchy–Main Memory–Auxiliary Memory–AssociativeMemory – Cache Memory – Virtual Memory.

Input/output Organization: Input-Output Interface - Asynchronous data transfer - Modes ofTransfer - Priority Interrupt - Direct memory Access.

UNIT- 5: PIPELINE AND MULTIPROCESSOR

Pipeline: Parallel Processing–Pipelining - Arithmetic Pipeline - Instruction Pipeline. **Multiprocessor:** Characteristics of Multiprocessors - Interconnection Structures–Inter processorArbitration - Inter Processor Communication and Synchronization.

Course Outcomes:
On successful completion of the course the student will be able to,

Course Outcomes		POs related to COs
CO1	Demonstrate the knowledge on fundamentals of organizational and architectural issues of a digital computer	PO1, PO2
CO2	Identify design issues in the development of processor or other components	PO1, PO2, PO3, PO4
CO3	Demonstrate control unit operations and conceptualize various data transfer operation among registers.	PO1, PO3
CO4	Categorize memory organization and explain the function of each element of a memory hierarchy and compare different methods for computer I/O mechanisms.	PO1, PO3, PO5
CO5	Understand and use the concept of Pipelining in various multiprocessor applications.	PO1, PO4, PO5

Text Books:

1. Computer Organization – Carl Hamacher, ZvonksVranesic, SafeaZaky, 5/e, MCG, 2002.
2. Computer Systems Architecture – M.Moris Mano, 3/e, PEA, 2007.

Reference Books:

1. Computer Systems Organization and Architecture- John D. Carpinelli, PEA, 2009
2. Computer Organization and Architecture – William Stallings,6/e, Pearson/PHI.
3. Structured Computer Organization – Andrew S. Tanenbaum, 4/e, PHI/Pearson.
4. Fundamentals or Computer Organization and Design - SivaraamaDandamudi Springer Int. Edition.
5. Computer Architecture a quantitative approach, John L. Hennessy and David A. Patterson, 4th Edition, Elsevier.
6. Computer Architecture: Fundamentals and principles of Computer Design, Joseph D. Dumas II, BS Publication.

QUESTION BANK

UNIT – 1: BASIC STRUCTURE OF COMPUTERS (CO1)	
PART-A (Two Marks Questions)	
Question No.	**Questions**
1	Draw the basic functional units of a computer.
2	Give short notes on system software.
3	Write the basic performance equation?
4	Define clock rate.
5	What is the role of MAR and MDR?
6	Explain Fixed point representation.
7	Define the term Computer Architecture.
8	What is meant by instruction?
9	Define Multiprocessing.
10	What is Bus? Draw the single bus structure.
11	Define Pipeline processing.
12	Briefly explain Primary storage and secondary storage.
13	What is register?
14	Write down the operation of control unit?
15	Suggest about Program counter
16	Write the 2's complement of 1011011
17	Represent $(70)_{10}$ in a signed magnitude format and One's Complement form
18	Perform the 2's complement subtraction of smaller number(101011) from larger number(111001).
19	When can you say that a number is normalized?
20	Define Multi computing
PART-B (Ten Marks Questions)	
1	Explain briefly about performance evaluation by using various bench marks. List out the types of bench marks and mention its advantage and disadvantage.
2	Explain Fixed point representation.
3	What is bus explain it in detail?
4	Describe the operational concepts between the processor and memory
5	Explain the different functional units of a computer
6	a.What are the various ways of representing negative numbers? Explain with example b. Distinguish between Fixed point and Floating point representation of a given number
7	a. Perform the arithmetic operation in binary using 2's complement representation (i). (+42) + (-13) (ii) (-42) – (-13). b. Convert the following numbers with the indicated bases to decimal. (i) $(12121)_3$ (ii) $(4310)_5$ (iii) $(50)_7$

8	A program contains 1000 instructions. Out of that 25% instructions requires 4 clock cycles,40% instructions requires 5 clock cycles and remaining require 3 clock cycles for execution. Find the total time required to execute the program running in a 1 GHz machine.
9	Discuss in detail about error detection code.
10	Draw the connection between processor and memory and mention the functions of each component in the connection.

Question No.	Questions
UNIT – 2: CPU DESIGN AND COMPUTER ARITHMETIC(CO2)	
PART-A (Two Marks Questions)	
1	Discuss the principle behind the Booth's algorithm?
2	When performing signed division, the sign of the remainder should be the same as the sign of the dividend. Why?
3	What is a Instruction Code?
4	What is a Operation Code (Opcode)?
5	Define Instruction Format.
6	Specify the sequence of operation involved when an instruction is executed.
7	What are the Most Common Fields Of An Instruction Format?
8	What is Addressing Modes?
9	What are the different types of addressing Modes?
10	Define Register mode and Absolute Mode with examples.
11	State the principle of operation of a carry look-ahead adder
12	What are the main features of Booth's algorithm?
13	How can we speed up the multiplication process?
14	Write the Add/subtract rule for floating point numbers.
15	In floating point numbers when so you say that an underflow or overflow has occurred?
16	Write the algorithm for non restoring division.
17	What is a Immediate addressing Mode?
18	Define Indirect addressing Mode.
19	What is a Relative Addressing mode?
20	Write the multiply rule for floating point numbers.
PART-B (Ten Marks Questions)	
1	a. Draw and explain the flowchart of instruction cycle. b. Explain any three addressing modes with example.
2	a. Draw the flowchart and explain about booths algorithm b. Multiply 100111 with 11011 using booths algorithm
3	Explain in detail the different instruction formats with examples
4	What are addressing modes? Explain the various addressing modes with examples.
5	Explain different types of instructions with examples. Compare their relative merits and demerits
6	Explain with an example how to multiply two unsigned binary numbers

7	Derive and explain an algorithm for adding and subtracting two floating point binary numbers
8	With examples explain the Data transfer, Logic and Program Control Instructions?
9	Explain how the expression X=A X B + C X C will be executed in one address, two address and three address processors in an accumulator organization.
10	Describe the algorithm for integer division with suitable examples.

Question No.	Questions
UNIT – 3: REGISTER TRANSFER LANGUAGE AND DESIGN OF CONTROL UNIT(CO3)	
PART-A (Two Marks Questions)	
1	Compare hardwired and micro programmed controls
2	Write the register transfer sequence to read a word from memory
3	What is a micro program sequencer?
4	Write the register transfer sequence for storing a word in memory
5	What is hard-wired control? How is it different from micro-programmed control?
6	Under what situations the micro program counter is not incremented after a new instruction is fetched from micro program memory?
7	What is half adder?
8	What is full adder?
9	What is a carry look-ahead adder?
10	Write down the control sequence for Move (R1), R2.
11	Define microprogrammed control.
12	Define parallelism in microinstruction.
13	What is control Word and control address registers?
14	Explain address sequencer.
15	What is BCD Adder?
PART-B (Ten Marks Questions)	
1	Explain the following: i. Address sequencing in control memory. ii. Micro program sequencer
2	Explain the design of micro-programmed control unit in detail
3	Explain how control signals are generated using micro-programmed control.
4	What are logical micro operations? Explain about applications of logical micro operation.
5	Explain different types of computer registers with common bus system with a neat sketch.
6	Explain about shift micro operation
7	What is control memory? Explain with address sequence.
8	Discuss in detail about the hardwired control unit with block diagram.
9	Consider a processor is having single bus organization of the datapath inside a processor. Write the sequence of control steps required for each of the followinginstructions: a) Add the (immediate) number NUM to register R1 b) Add the contents of memory location NUM to register R1. c) Add the contents of the memory location whose address is at memory location NUM to register R1
10	Explain the design of ALU in detail

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Question No.	Questions
UNIT – 4: MEMORY AND INPUT/OUTPUT ORGANIZATION(CO4)	
PART-A (Two Marks Questions)	
1	Define Memory Access Time?
2	Define memory cycle time.
3	What is cache memory?
4	Explain virtual memory.
5	What is the mapping procedures adopted in the organization of a Cache Memory?
6	Define Hit and Miss?
7	Write the formula for the average access time experienced by the processor in a system with two levels of caches
8	What are the enhancements used in the memory management?
9	What do you mean by seek time?
10	How the data is organized in the disk?
11	Define latency time.
12	Why IO devices cannot be directly be connected to the system bus?
13	What are the major functions of IO system?
14	What is an I/O Interface?
15	Write the factors considered in designing an I/O subsystem?
16	Explain Direct Memory Access.
17	Define DMA controller.
18	What is a Priority Interrupt?
19	Define asynchronous bus.
20	What do you mean by memory mapped I/O?
PART-B (Ten Marks Questions)	
1	Draw the neat sketch of memory hierarchy and explain the need of cache memory?
2	Explain about direct and set associative map technique in cache.
3	a. What is DMA? Explain b. Write about daisy chaining priority
4	a. Write about asynchronous data transfer. b. Explain about serial communication
5	What is IO Interface? Discuss the differences that exist between central computer and Peripherals.
6	Explain source initiated asynchronous data transfer procedure with necessary diagram.
7	a. What is I/O interface and explain it with block diagram. b. Draw the block diagram of DMA controller
8	Explain how I/O devices can be interfaced with a block diagram
9	How data transfers can be controlled using handshaking technique?
10	Explain the following a) Memory mapped I/O b) I/O Registers c) Hardware Interrupts

	d) Vectored interrupt

Question No.	Questions
UNIT – 5: PIPELINE AND MULTIPROCESSOR (CO5)	
PART-A (Two Marks Questions)	
1	What are the major characteristics of a pipeline?
2	What is a pipeline hazard?
3	What are the types of pipeline hazards?
4	What do you mean by branch penalty?
5	What do you mean by delayed branching?
6	What are the two types of branch prediction techniques available?
7	Define parallel processing.
8	Define instruction pipeline.
9	What are the steps required for a pipelinened processor to process the instruction?
10	What are the classification of data hazards?
11	How data hazard can be prevented in pipelining?
12	How addressing modes affect the instruction pipelining?
13	Define – Superscalar Processor
14	What is (Division Overflow)/Arithmetic overflow?
15	Write the steps for subtraction of two floating numbers.
PART-B (Ten Marks Questions)	
1	Explain about arithmetic pipelining.
2	Draw and explain the flowchart of four segment instruction pipelining.
3	What is instruction pipelining? What are the conflicts that occurred during instruction Pipelining?
4	Why inter process synchronization needed? Explain
5	Describe the techniques for handling control hazards in pipelining
6	Define parallel processing and explain the flynn's classification of computer with suitable diagram.
7	Describe the data and control path techniques in pipelining
8	Discuss the basic concepts of pipelining
9	What is instruction hazard? Explain in detail how to handle the instruction hazards in pipelining with relevant examples
10	Explain the following a) Time shared common bus system b) Cross bar switch c) Multiport memory

----------All the Best----------