Digital Design through Verilog HDL LAB

In DDV lab students have the ability to code and simulate any digital function in Verilog HDL. Know the difference between synthesizable and non-synthesizable code. Understand library modeling, behavioral code and the differences between them. Understand the differences between simulator algorithms. Learn good coding techniques per current industrial practices. Understand logic verification using Verilog simulation.

It is also to be used as project Lab.

Figure 6.5 – Digital Design through Verilog HDL Lab