Instruction Pipeline

Instruction Pipeline

- An instruction pipeline reads consecutive instructions from memory while previous instructions are being executed in other segments.
- Computers with complex instructions requires 6 phases in instruction cycle as follows:

  [1] Fetch an instruction from memory

  [2] Decode the instruction

  [3] Calculate the effective address of the operand

  [4] Fetch the operands from memory

  [5] Execute the operation

  [6] Store the result in the proper place

Instruction Pipeline

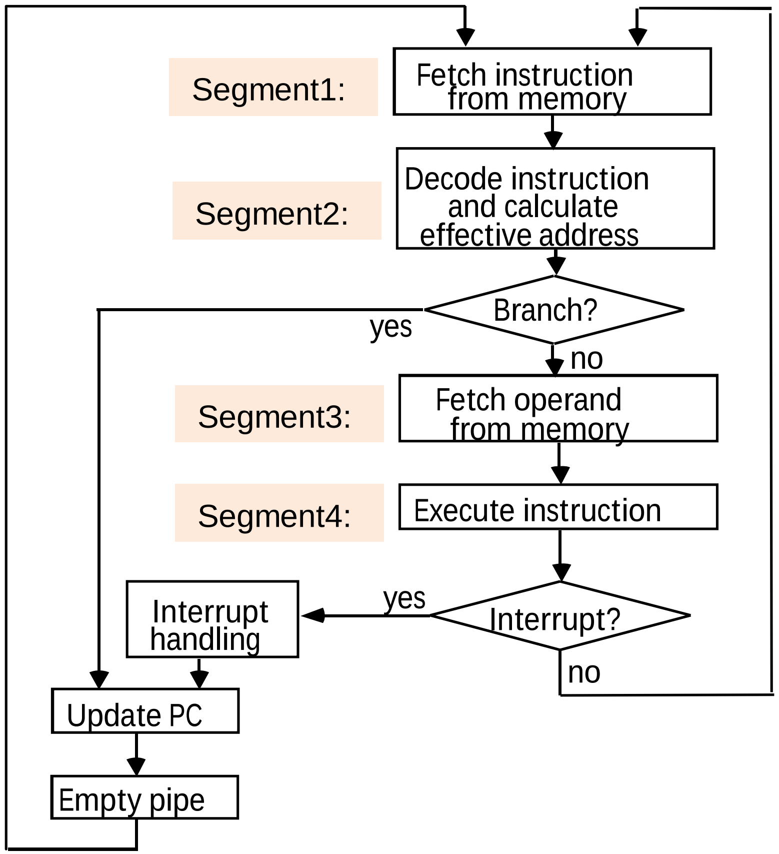
- Some segments are skipped for certain operations

  Ex: A register mode instruction does not need an effective address but remaining other segments may require it.
- Memory access conflicts are resolved by using two memory buses for accessing instruction and data in separate module.

Four Segment Instruction Pipeline

- Consider that the decoding of instruction can be combined with calculation of effective address into one segment.
- The instruction execution and storing of result can be combined into one segment. This reduces the instruction pipeline into four segments.
- The below figure shows the instruction cycle in the CPU with 4 segment pipeline.

Four Segment Instruction Pipeline



Four Segment Instruction Pipeline

- When an instruction is being executed in segment 4, the next instruction in sequence is busy in fetching an operand from memory in segment 3.
- The effective address may be calculated for the third instruction in the segment 2.
- Fourth and all subsequent instruction can be fetched and placed in FIFO at segment 1.
- Four different instruction can be in progress at four different segments.

Four Segment Instruction Pipeline

- An instruction in the sequence is program control type that causes a branch out of normal sequence.
- In that case the pending operation in last 2 segment are completed and all the instruction stored in instruction buffer are deleted.
- The pipeline then restarts from new address stored in PC.
- Similarly an interrupt request is also handled by making the pipeline empty and start again with a new address value.

Four Segment Instruction Pipeline

- The below figure shows the operation of instruction pipeline:

	Step:	1	2	3	4	5	6	7	8	9	10	11	12	13
Instruction	1	FI	DA	FO	EX									
	2		FI	DA	FO	EX								
(Branch)	3			FI	DA	FO	EX							
	4				FI	–	–	FI	DA	FO	EX			
	5					–	–	–	FI	DA	FO	EX		
	6									FI	DA	FO	EX	
	7										FI	DA	FO	EX

Four Segment Instruction Pipeline

- The four segments represented in the diagram are

  [1] FI: Fetch an instruction from memory

  [2] DA: Decode the instruction and calculate
  the effective address of the operand

  [3] FO: Fetch the operand

  [4] EX: Execute the operation

Pipeline Conflicts

Pipeline Conflicts : 3 major difficulties

1) Resource conflicts: memory access by two segments at the same time. Most of these conflicts can be resolved by using separate instruction and data memories.

2) Data dependency: This conflict arise when an instruction depend on the result of a previous instruction.

3) Branch difficulties: branch and other instruction (interrupt, ret, ..) that change the value of PC.