Unit-II
characteristics of opAmp

Introduction:-

The operational Amplifier most commonly referred as "opAmp" was introduced in 1940's. Robert J. Widlar at fairchild brought out the Nelinear 741 IC in 1964 to 1968 the IC version of opamp uses BJT & FETS which are fabricated along with the other supporting components on a single semiconductor chip.

→ As well as the circuit design become very simple, IC opamp inexpensive, take occupie less space & consume less Power opamp has become an integral part of almost circuit which uses linear integrated circuit the IC opamp works at lower voltages. It is so that am millions are now in use.

Symbol:-

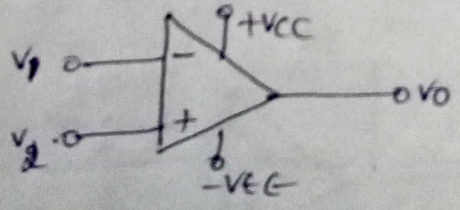


Fig:- op-amp

V_1 → Inverting input terminal

V_2 → Non Inverting input terminal

V_o → output terminal

+Vcc, -VEE → Power supplies.

chaxactexstics of Ideal op-amp:-

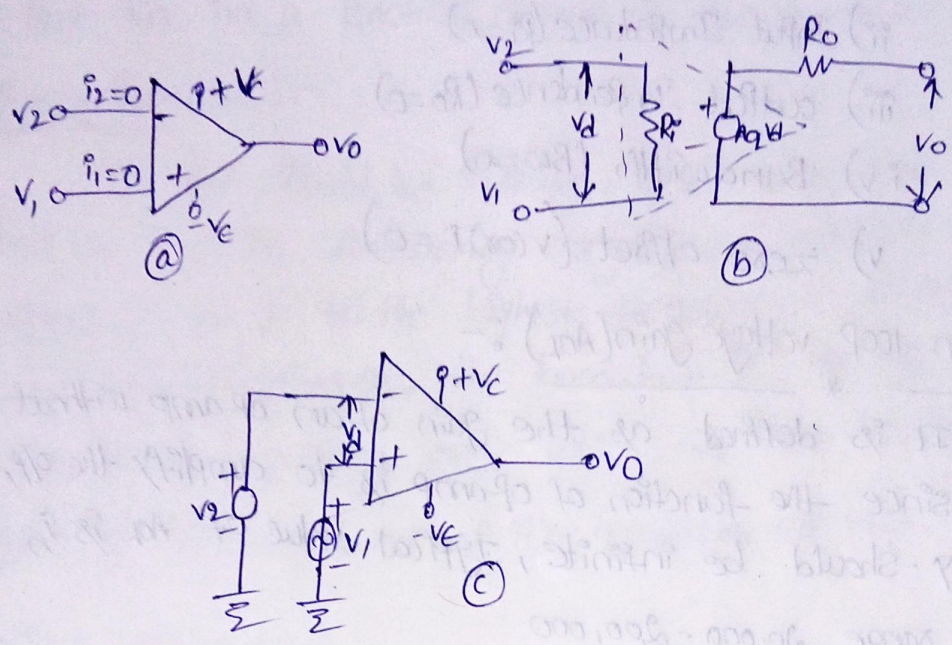


fig:- (a) Ideal op-amp (b) equivalent circuit (c) open-loop circuit.

An ideal op-amp is a 3-terminal linear device, which posses all the properties of heasly ideal dc-amplification. these are two input terminals designated as Inverting terminal (-ve sign) & Non-Inverting terminal (+ve sign) and one output terminal that can act as source (or) sink for both voltage & cussent. If $V_1 = 0$ output V_0 is 180° out of phase with input signal V_2. when $V_2 = 0$, output V_0 will be in-phase with the input signal applied at V_1. the output voltage is dependent on the diffexence of two input voltage signals ($V_2 - V_1$), the op-amp is called a "diffexential-Amplifiex".

⇒ the op-amp is said to be ideal if it has the following chaxactexstics.

i) open loop gain (A_{OL})

ii) Input Impedence ($R_i = \infty$)

iii) output Impendance ($R_o = 0$)

iv) Bandwidth ($B_W = \infty$)

v) zero offset ($V_{(OS)I} = 0$)

i) open-loop voltage gain (A_{OL}) :-

It is defined as the gain of an op amp without any since the function of op amp is to amplify the o/p, ideally should be infinite, Typical value of A_{OL} is in the range 20,000 - 2,00,000

$$A_{OL} = \frac{V_O}{V_i}$$

ii) Input Impedence (R_i) :-

Input Impedence is defined as the ratio of input voltage to input current (I_i). Ideally R_i should also be infinite to zero current flow b/w input terminals of the op amp. However in practical op amp the input current called leakage current, voltage a few Pico amperes to few milli amperes.

iii) output Resistance (or) output Impedence (R_O) :-

Ideally R_O which Represents the internal Resistance of o/p voltage source & is connected in series with the load. So zero to ensure that the latter can supply as much current to load as is required due to voltage drop in the internal resistance

Resistance

output voltage is very small. Typically it contains

Ideally zero.

∴ But R_o in a practical opamp is b/w 20-100Ω

Bandwidth (BW):-

The BW should be infinite, which means that it has an infinite frequency range & can amplify any signal from dc to the highest frequency's. However in working opamps, the bandwidth is defined as the frequency range over which the open loop voltage gain is -3dB (or) 70.7% of it's maximum o/p value.

offset voltage (V_{io}) :-

Ideally V_{io} should be zero. It represents a condition of an opamp's zero o/p & is brought by the inverting(V_{i1}) & non-inverting(V_{i2}) input signals being zero (or) equal (or) both the inputs being grounded. In real opamps, some amount of output offset voltage is invariably present.

Practical op-amp characteristics:-

i) open-loop voltage gain A_{OL} =

ii) Input Impedance $R_i = 10^7 - 10^{12}$

iii) output Resistance $R_o = < 100\Omega$

iv) Bandwidth

v) → offset voltage = mV
→ offset current = nA (or) pA

MOSFET op-amp - CA3130 (RCA corporation)

Op-amp DC characteristics:

- Ideal op-amp draws no current from the source, response independent of temperature.
- Real op-amp does not.
- current taken from the source into op-amp i/ps.
- Two i/p's respond differently to current and voltage due to mismatch in transistors.
- Real op-amp shifts its operation with temperature.

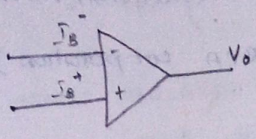
The non-ideal characteristics that add error components to the dc o/p voltage are,

1) I/p bias current
2) I/p offset current
3) I/p offset voltage
4) Thermal drift

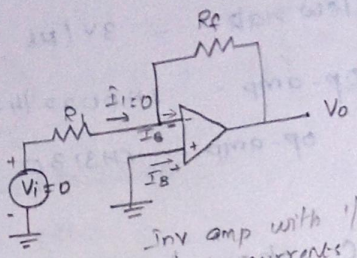
i) I/p bias current:

- op-amp's i/p to diff. amp. may be made of BJT or FET.
- In either case, i/p trls must be biased into their linear region by supplying currents into the bases, by external circuits.

- In Ideal op-amp no current is drawn from the i/p terminals
- Practically i/p terminals do conduct a small value of dc current to bias the i/p transistors.
- Base current entering into the inv & non-inv terminals are I_B^- & I_B^+ resp.



I/p bias currents



Inv amp with i/p bias currents

Even though, both transistors are identical, I_B^- and I_B^+ are not exactly equal, due to internal imbalances b/w 2

Avg. value of base current $\Rightarrow I_B = \frac{I_B^+ + I_B^-}{2}$

For 741, the bias current = 500 nA or less

FET op-amp $\Rightarrow$ I_B as low as 50 pA at room temp.

Consider the basic inv. amp above,

I/p V_i is set to 0V,

V_o should also be 0V.

o/p voltage is offset by $V_o = (I_B^-) R_f$

1 MΩ feedback resistor $\Rightarrow V_o = 500\,nA \times 1\,M\Omega$

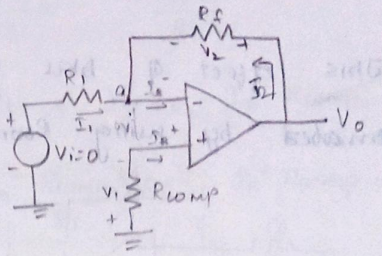
$= 500\,mV.$

o/p is driven to 500 mV with zero i/p because of bias current.

But this is unacceptable in applications.

This effect can be compensated by Rcomp compensation resistors.

- Rcomp added b/w the NI i/p and ground.
- Current I_B^+ flowing thru Rcomp develops V_1 across it.



By KVL,

$$-V_1 + 0 + V_2 - V_o = 0$$

$$V_o = V_2 - V_1 \rightarrow (1)$$

By selecting proper value of Rcomp, V_2 can be cancelled with V_1 and o/p V_o will be '0'

Rcomp is derived as,

$$V_1 = I_B^+ R_{comp} \rightarrow (2)$$

$$I_B^+ = \frac{V_1}{R_{comp}} \rightarrow (3)$$

At node 'a' voltage is $\rightarrow V_1$

with $V_i = 0 \Rightarrow I_1 = \frac{V_1}{R_1} \rightarrow (4)$

$$I_2 = \frac{V_2}{R_f} \rightarrow (5)$$

V_o should be '0' for $V_i = 0 \Rightarrow V_2 - V_1 = 0$ (from (1))

$$\therefore V_1 = V_2 \rightarrow (6)$$

$$(5) \Rightarrow I_2 = \frac{V_1}{R_f} \rightarrow (7)$$

KCL at node 'a', $I_B^- = I_2 + I_1$

$$= \frac{V_1}{R_f} + \frac{V_1}{R_1} \rightarrow (8)$$

$$I_B^- = \frac{V_1 (R_1 + R_f)}{R_1 R_f} \rightarrow (9)$$

$$V_1 = I_B^+ R_{comp}$$

$$I_1 = V_1/R_1 = I_B^+ \cdot R_{comp}/R_1$$

KCL at node 'a'

$$I_2 = (I_B^- - I_1) = I_B^- - \frac{I_B^+ R_{comp}}{R_1}$$

$I_B^- - I_1 = I_2$

$$V_0 = I_2 R_f + V_1 = I_2 R_f - I_B^+ R_{comp}$$

$$= \left(I_B^- - \frac{I_B^+ R_{comp}}{R_1}\right) R_f - I_B^+ R_{comp}$$

Sub $R_{comp} = R_1 R_f / R_1 + R_f$

$$\therefore V_0 = \left(I_B^- - I_B^+ \cdot \frac{R_f R_1}{(R_1+R_f) R_1}\right) R_f - I_B^+ \frac{R_1 R_f}{R_1+R_f}$$

$$= I_B^- R_f - \frac{I_B^+ R_f^2}{R_1+R_f} - I_B^+ \frac{R_1 R_f}{R_1+R_f}$$

$$= I_B^- R_f - I_B^+ \left[\frac{R_f^2}{R_1+R_f} + \frac{R_1 R_f}{R_1+R_f}\right]$$

$$= I_B^- R_f - I_B^+ \left[\frac{R_f^2 + R_1 R_f}{R_1+R_f}\right]$$

$\frac{R_f^2}{2R_f} + \frac{R_f^2}{2R_f}$

$I_B^- \left(\frac{R_f}{2} + \frac{R_f}{2}\right)$

Manipulated as,

$$V_0 = \left(I_B^- - I_B^+\right) R_f$$

$$\boxed{V_0 = R_f \cdot I_{os}}$$

With bias current compensation & with F/B resistor 1MΩ (741),

BJT op amp has an o/p offset voltage of

$$V_0 = 1\,M\Omega \times 200\,nA$$

$$= 200\,mV$$ with zero i/p volt,

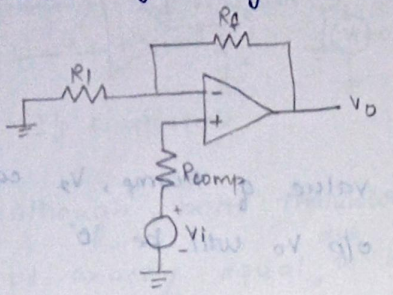
The effect of bias current can be minimized by keeping f/b resistance small.

If $I_B^+ = I_B^-$

from ③ & ④ $\Rightarrow \frac{V_1}{R_{comp}} = \frac{V_1(R_1+R_f)}{R_1 R_f}$

$$R_{comp} = \frac{R_1 R_f}{R_1+R_f} = R_1 \| R_f$$

This effect of bias current in N.I is also compensated by using R_{comp} in series with i/p signal V_i



→ Bias current compensation in a Non-Inv. amplifier

a) I/p offset current:

The bias current compensation works only when $I_B^+ = I_B^-$. The i/p terms. not identical, there is a diff. b/w I_B^+ & I_B^-, $I_B^+ \neq I_B^-$. This difference is called offset current I_{os}, can be written as,

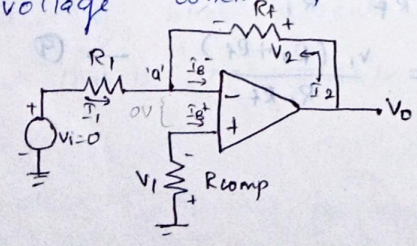
$$|I_{os}| = I_B^+ - I_B^-$$

The absolute value sign indicates that there is no way to predict which of the bias current will be larger.

Offset current I_{os} (BJT) op-amp : 200nA

FET op amp = 10pA

Even with bias current compensation, I_{os} provides o/p voltage when i/p $V_i = 0$



$V_1 = I_B^+ R_{comp}$

$I_1 = V_1/R_1 = I_B^+ \cdot R_{comp}/R_1$

KCL at node 'a'

$I_2 = (I_B^- - I_1) = I_B^- - \frac{I_B^+ R_{comp}}{R_1}$

$I_B^- - I_1 = I_2$

$V_0 = I_2 R_f - V_1 = I_2 R_f - I_B^+ R_{comp}$

$= \left(I_B^- - \frac{I_B^+ R_{comp}}{R_1}\right) R_f - I_B^+ R_{comp}$

Sub $R_{comp} = R_1 R_f / R_1 + R_f$

$V_0 = \left(I_B^- - I_B^+ \cdot \frac{R_f R_1}{(R_1+R_f)R_1}\right) R_f - I_B^+ \cdot \frac{R_1 R_f}{R_1+R_f}$

$= I_B^- \cdot R_f - \frac{I_B^+ R_f^2}{R_1+R_f} - I_B^+ \frac{R_1 R_f}{R_1+R_f}$

$= I_B^- R_f - I_B^+ \left[\frac{R_f^2}{R_1+R_f} + \frac{R_1 R_f}{R_1+R_f}\right]$

$= I_B^- R_f - I_B^+ \left[\frac{R_f^2 + R_1 R_f}{R_1+R_f}\right]$

$\frac{R_f^2}{2R_f} + \frac{R_f^2}{2R_f}$

$I_B^- \left(\frac{R_f}{2} + \frac{R_f}{2}\right)$

Manipulated as,

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with bias current compensation & with F/B resistor 1MΩ 741,

BJT op-amp has an o/p offset voltage of

$V_0 = 1M\Omega \times 200nA$

$= 200mV$ with zero i/p volt,

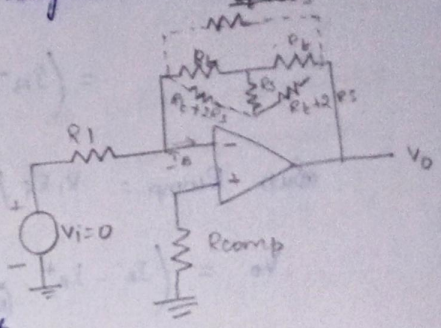
The effect of bias current can be minimized by keeping f/b resistance small.

But R_1 should be high for high i/p impedance, so that R_f should also be high to obtain reasonable gain.

T-fb nlw is a good solution

T nlw provides large FB resistance while keeping the resistance to ground low as in dotted nlw.

T nlw provides feedback signal as if the nlw use a single F/B resistor.



By T to π conversion,

$$R_f = \frac{R_t^2 + 2R_tR_s}{R_s}$$

To design a T nlw; $R_t << \frac{R_f}{2}$

$$R_s = \frac{R_t^2}{R_f - 2R_t}$$

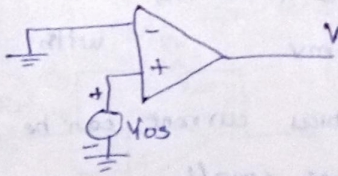
3) Input offset voltage:

Inspite of the above compensation techniques, it is found that the o/p voltage may still not be zero with i/p voltage.

This is due to unavoidable imbalances inside the op-amp & one may have to apply a small voltage at the i/p to make the o/p zero. This voltage is called i/p offset voltage (V_{IOS})

Thus is the volt. required to be applied at the input for making output voltage to zero volts.

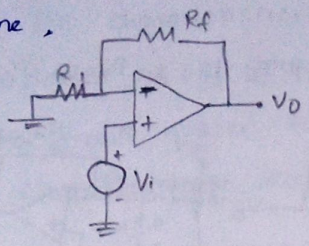
$$V_2 = \left(\frac{R_1}{R_1+R_f}\right) V_o$$



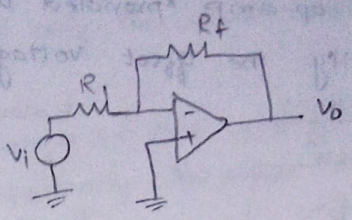
$$\Rightarrow V_o = \left(1 + \frac{R_f}{R_1}\right) V_2$$

Op.amp showing i/p offset voltage

If V_i is set to zero, both inv & non-inv become same.

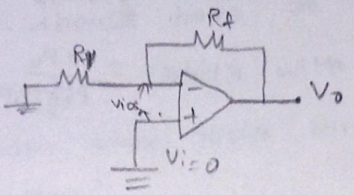


NI Amp



Inv

If $V_i = 0 \Rightarrow$



$$V_{ios} = |V_1 - V_2| = |0 - V_2| = V_2$$

$$\boxed{V_o = \left(1 + \frac{R_f}{R_1}\right) V_{ios}}$$ → i/p offset voltage in closed loop configuration.

Total output offset voltage (V_{OT}):

V_{OT} could be either more or less than the offset voltage produced at the o/p due to i/p bias current and i/p offset voltage alone.

Bec. of I/p offset voltage (V_{ios}) & i/p bias current, I_B, could be either +ve (or) -ve w.r.t gnd.

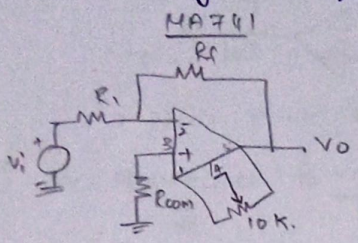
Max. offset voltage at the o/p of an inv. & non-inv. amp. without any compensating tech used is,

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{ios} + I_B R_f$$

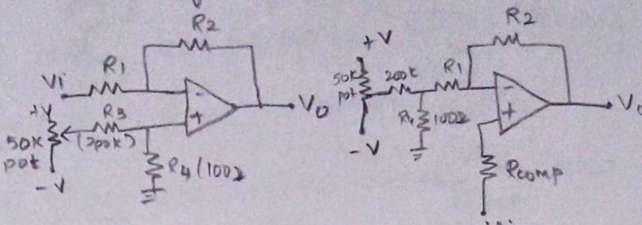
However with R_{comp} in the circuit, the total o/p offset volt. will be

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{ios} + R_f I_{os}$$

The op-amp provided with offset compensation pin to nullify the offset voltage.



Balancing ckt for Inv & Non-Inv.



$V_{os} = \pm \frac{V R_4}{R_3 + R_4}$

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In 741 op-amp, manufacturers recommend that a 10k pot be placed across offset null-pins 1 & 5 & wiper be connected to -ve supply pin 4. The position of wiper is adjusted to nullify o/p offset voltage.

However, when the gn. op-amp does not have offset null pins, external balancing tech. are used.

4) Thermal drift :

Bias current, offset current, offset voltage changes with temperature.

A circuit carefully nulled at 25°C may not remain same, when temp is increased to 35°C. This is called drift.

Offset current drift → nA/°C
" voltage " → mV/°C

These indicate the change in ct or voltage for each degree celsius change in temp.

These are very few ckts for drift compensation

→ careful PCB layout → to keep op-amp away from heat.

→ Forced air cooling → to stabilize the ambient temp.

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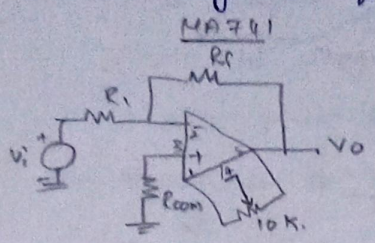

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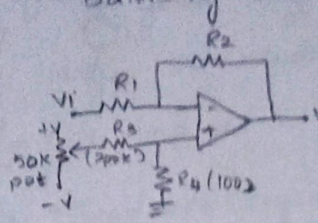
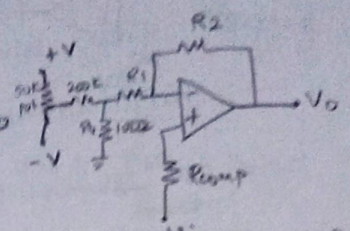


$$V_{os} = \pm \frac{V R_4}{R_3 + R_4}$$



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AC characteristics:

DC characteristics - affects only the steady state dc response of op-amp.

For small signal AC applications :→ one should know the ac characteristics such as frequency response & slew rate.

Frequency response:

Ideal op-amp should have ∞ BW.

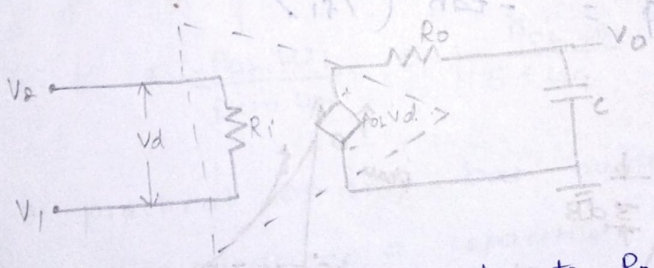
(ie) If its open loop gain = 90dB with dc signal, its gain should remain same 90dB thru audio & on to high radio frequencies.

The practical op-amp gain decreases at high frequencies. what causes the gain of op-amp to roll off (decrease) after certain frequency?

There must be a capacitor in the eqnt. circuit of op-amp. This capacitance is due to physical char. of device (FET or BJT) used and the internal construction of op-amp.

For an op-amp with one break freq. all the capacitor effects can be represented by a single capacitor 'C'.

High freq. model of op-amp with single corner frequency



There is one pole due to $R_o C$ and -20 dB/decade roll off comes into effect.

The open loop gain of an op-amp with only one corner freq. is obtained from

$$V_o = \frac{X_C}{R_o + X_C} A_{OL} V_d$$

$$A = \frac{V_o}{V_d} = \frac{-j/\omega C}{R_o - j/\omega C} \cdot A_{OL}$$

$$= \frac{-j/2\pi f C}{R_o - j/2\pi f C} \cdot A_{OL}$$

$$= \frac{-j \quad A_{OL}}{-j\left[1 + j 2\pi f C R_o\right]} \qquad f_1 = \frac{1}{2\pi R_o C}$$

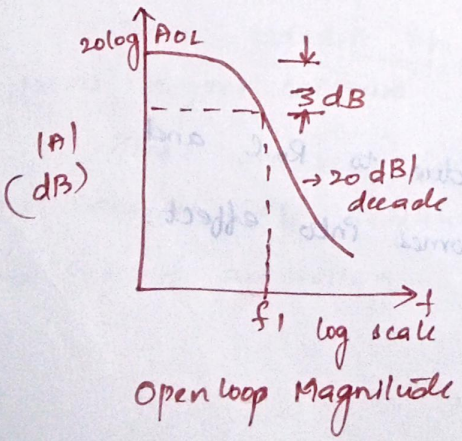
$$A = \frac{A_{OL}}{1 + j\left(f/f_1\right)}$$

where $f_1 \rightarrow$ corners frequency or upper 3dB freq. of op-amp.

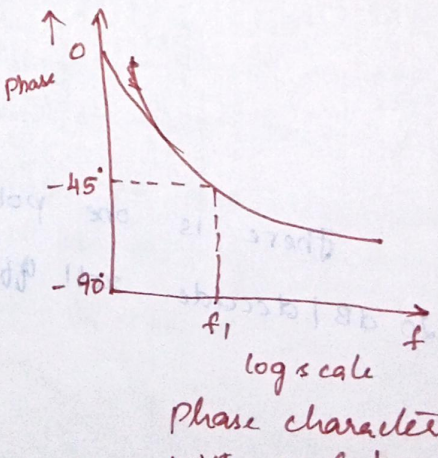
Mag. & phase angle of open loop voltage gain is

$$|A| = \frac{A_{OL}}{\sqrt{1 + \left(f/f_1\right)^2}}$$

$$\phi = -\tan^{-1}\left(f/f_1\right)$$



Open loop Magnitude



Phase characteristics with single break frequency

For i) $f << f_1$, $|A| \rightarrow 20 \log A_{OL}$ in dB

ii) $f = f_1$, $|A| \rightarrow$ 3dB down from dc value of A_{OL} in dB. This f_1 is corner frequency.

iii) $f >> f_1$, $|A|$ rolls off at the rate of -20dB/dec or -6dB/octave.

Phase angle,

Phase angle = 0 at $f = 0$

At $f = f_1$, angle $= -45^\circ$ (lagging)

At $f = \infty$, angle $= -90^\circ$

$90^\circ \rightarrow$ max phase change occures in op-amp with single capacitor.

- Zero freq. does not occur in log scale
- For practical cases, zero freq is taken as one decade below corner freq.
- Infinite freq $\rightarrow$ one decade above corner freq.

Voltage transfer function in s-domain

$$A = \frac{A_{OL}}{1 + j f/f_1} = \frac{A_{OL}}{1 + j \omega/\omega_1} \qquad s = j\omega$$

$$= \frac{A_{OL}\,\omega_1}{j\omega + \omega_1} = \frac{A_{OL}\,\omega_1}{s + \omega_1}$$

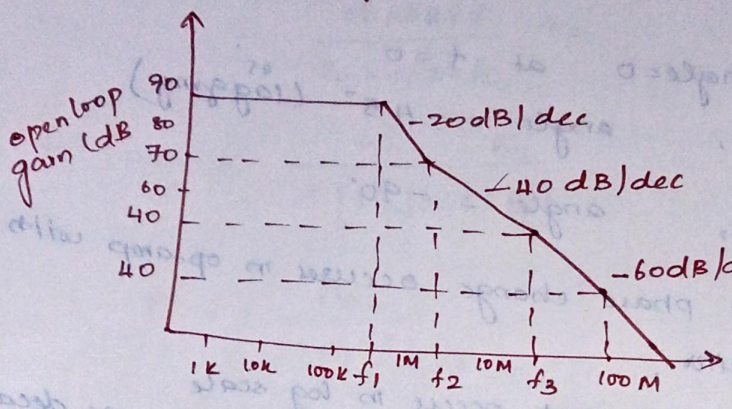
A practical op-amp has number of stages, Each stage produces a capacitive component. Thus due to a no. of RC pole pairs, there will be number of break frequencies.

Ex. 3 break freq.

$$A = \frac{A_{OL}}{(1+jf/f_1)(1+jf/f_2)(1+jf/f_3)} \qquad 0 < f_1 < f_2 < f_3$$

$$= \frac{A_{OL}\,\omega_1\omega_2\omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)} \qquad 0 < \omega_1 < \omega_2 < \omega_3$$

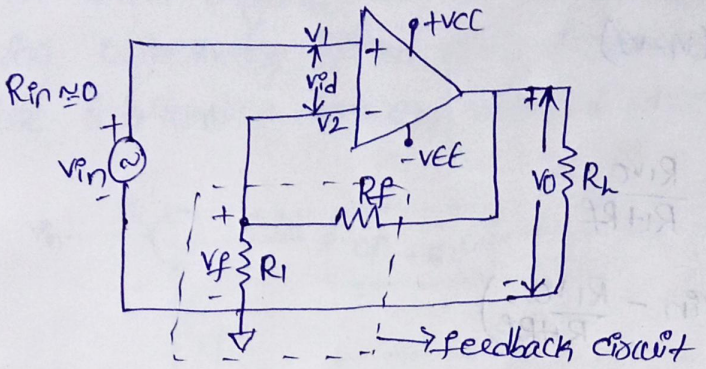
Openloop gain Vs freq. in log scale.



- Open loop freq. response → +90dB for low frq. to 200 KHz first break freq. (f_1)
- 200KHz to 2 MHz — Grain drops from 90 to 70 dB
- 2M to 20MHz — roll off rate → -40dB/dec

⇒ Frequency increases ⇒ cascading effect of RC pairs come into effect & roll off rate increases by -20dB/dec at each corner frequency.

Voltage-Series feedback Amplifier:-



the op-amp represented by a schematic symbol, including it's large-signal voltage gain 'A' and feedback circuit composed of two Resistors R_1 & R_f. it is commonly known as "non-inverting feedback amplifier".

→ specifically the voltage gain of the op-amp with and without feedback and the gain of the feedback circuit are defined as follows

i) open-loop voltage gain (without f/b) $A = \frac{V_o}{V_{id}}$

ii) closed-loop voltage gain (with f/b) $A_f = \frac{V_o}{V_{in}}$

iii) Gain of the feedback circuit $\beta = \frac{V_f}{V_o}$

i) Negative feedback:-

KVL for the input loop is

$$V_{id} = V_{in} - V_f \rightarrow (1)$$

where V_{in} = input voltage ; V_f = feedback voltage

V_{id} = differential input voltage.

ii) closed loop gain:-

the closed-loop voltage gain is $A_F = \frac{V_o}{V_{in}}$

however $V_o = A(V_1 - V_2)$

But $V_1 = V_{in}$

$$V_2 = V_f = \frac{R_1 V_o}{R_1 + R_f}$$

$$V_o = A\left(V_{in} - \frac{R_1 V_o}{R_1 + R_f}\right)$$

$$V_o + \frac{R_1 V_o A}{R_1 + R_f} = AV_{in}$$

$$AV_{in} = V_o\left[1 + \frac{R_1 A}{R_1 + R_f}\right]$$

$$\frac{V_o}{V_{in}} = \frac{A(R_1 + R_f)}{R_1 + R_f + AR_1} \rightarrow (2)$$

we know that

$AR_1 >> (R_1 + R_f)$, so Generally 'A' very large.

$$A_F = \frac{A(R_1 + R_f)}{AR_1}$$

$$\boxed{A_F = 1 + \frac{R_f}{R_1}} \rightarrow (3)$$

eqn (3) defines the voltage-gain of the feedback amplifier is determined by the ratio of the two Resistors R_f & R_1.

→ the gain of the feedback circuit is

$$\beta = \frac{V_f}{V_o}$$

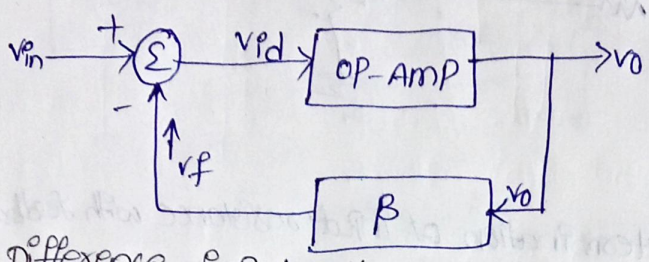
$$= \frac{R_1}{R_1 + R_f} \rightarrow (4)$$

on comparing eqn (3) & (4) we can conclude.

$$A_f = \frac{1}{\beta}$$

where $\boxed{A_f = \frac{A}{1+AB}}$ → (6)

→ A block diagram can be constructed to represent eqn (6) for representing system with feedback and also indicates the relationship between different variables of the system.



iii) Difference input voltage Ideally zero:-

open loop voltage gain $A = \frac{V_O}{V_{id}}$

$$V_{id} = \frac{V_O}{A}$$

since A is very large (ideally $A = \infty$)

$$V_{id} \cong 0$$

$$i.e\ V_1 - V_2 \cong 0$$

$$V_1 \cong V_2 \rightarrow (7)$$

where $V_1 = V_{in}$

$$V_2 = V_f = \frac{R_1 V_O}{R_1 + R_f}$$

(7) $\Rightarrow$ $V_{in} = \frac{R_1 V_O}{R_1 + R_f}$

$$A_F = \frac{V_O}{V_{in}} = 1 + \frac{R_F}{R_1}$$

iv) Input Resistance with feedback:-

the below circuit shows R_i is the input Resistance of the op amp (open-loop) and R_{if} is the input Resistance with the f/b is defined as

$$R_{if} = \frac{V_{in}}{I_{in}}$$

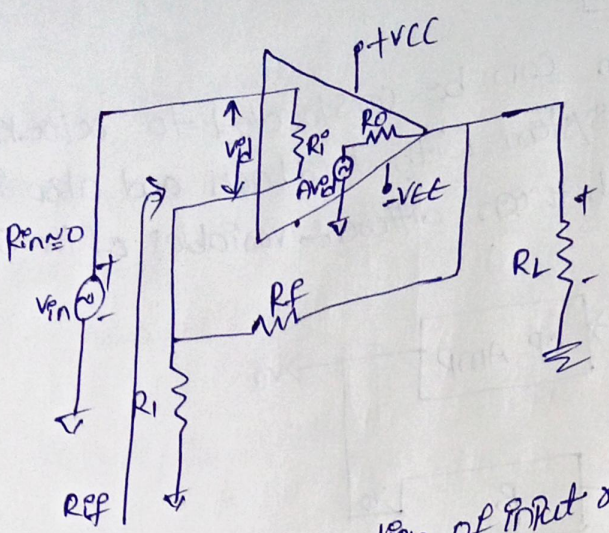


fig:- determination of input resistance with feedback

$$= \frac{V_{in}}{\frac{V_{id}}{R_i}}$$

But $V_{id} = \frac{V_o}{A}$ & $V_o = \frac{A}{1+A\beta} V_{in}$

$$\therefore R_{if} = R_i \frac{V_{in}}{\frac{V_o}{A}}$$

$$= AR_i \frac{V_{in}}{\frac{AV_{in}}{(1+A\beta)}}$$

$$\boxed{R_{if} = R_i (1+A\beta)} \rightarrow (8)$$

this means that input Resistance of the opamp with feedback is $(1+A\beta)$ times that without feedback.

(v) output Resistance with feedback:-

output Resistance is the Resistance determined looking back into feedback amplifier from the output end. this resistance can be obtained by using thevenin's theorem from dependent sources.

Specifically to find output resistance with feedback R_{OF}, with $V_{in}=0$.

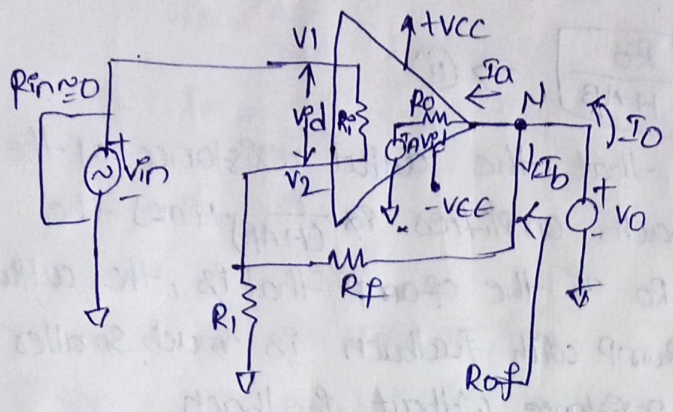


fig:- Derivation of output Resistance with feedback.

$$R_{of} = \frac{V_o}{i_o}$$

writing KCL at node N; we get

$$i_o = i_a + i_b$$

Since $[(R_f+R_1)\|R_1] \gg R_o$ & $i_a \gg i_b$

$$i_o \cong i_a$$

the current I_o can be found by writing KVL for output loop.

$$V_o - R_o I_o - A V_{id} = 0$$

$$i_o = \frac{V_o - A V_{id}}{R_o} \rightarrow (9)$$

But $V_{id} = V_1 - V_2$

$$= 0 - V_f$$

$$= -\frac{R_1 V_o}{R_1+R_f}$$

$\left\{ \beta = \frac{R_1}{R_1+R_f} \right.$

$$V_{id} = -\beta V_o$$

$$\therefore i_o = \frac{V_o + A\beta V_o}{R_o} \rightarrow (10)$$

$$R_{of} = \frac{V_o}{(V_e(1+AB))/R_o}$$

$$\boxed{R_{of} = \frac{R_o}{1+AB}} \rightarrow (11)$$

This result shows that the output resistance of the voltage series feedback amplifier is $\frac{1}{(1+AB)}$ times the output resistance R_o of the opamp. That is, the output Resistance of the opamp with feedback is much smaller than the output resistance without feedback.

vi) Bandwidth with feedback:-

The Bandwidth of an amplifier is defined as the range of frequencies for which the gain remain constant. Manufacturer generally specify either the gain-bandwidth product (or) supply open-loop gain versus frequency curve of opamp.

From this curve for a gain of 2,00,000, the Bandwidth is approximately 5Hz (or) gain-bandwidth product is $(200000 \times 5) = 1MHz$. on the other hand, the Bandwidth is approximately 1MHz when the gain is 1.

For 741, 5Hz is the break frequency, the frequency at which the gain 'A' is 3dB down from it's value at 0Hz & it is denoted by "f_0". on the other hand, the frequency at which the gain equals '1' is known as "unity-gain Bandwidth" (UGB).

$$UGB = Af_0$$

Similarly, the UGB of a FB system is

$$V_{GIB} = A_F F_F$$

$$\therefore A_{fo} = A_F f_f$$

$$f_f = \frac{A_{fo}}{A_F}$$

But $$A_F = \frac{A}{1+AB}$$

$$F_F = \frac{A_{fo}}{\frac{A}{1+AB}}$$

$$f_f = f_o(1+AB) \rightarrow (12)$$

eqn (12) shows the Bandwidth of the feedback op-amp, f_f is equal to it's bandwidth without feedback, f_o times $(1+AB)$.

vii) Total output offset voltage with feedback :-

In an op-amp when input is zero, the output is also expected to be zero, however, because of the effect of input offset voltage & current, the output is significantly larger., as result in large part of very high open-loop gain. that is, the high gain aggravates the effect of input offset voltage & current at the output. we call this enhanced output voltage level the "Total output offset voltage V_{OOT}".

→ In an open-loop op-amp the total output offset voltage is equal to either the positive (or) Negative saturation voltage.

$$V_{OOT} = \frac{\pm V_{Sat}}{1+AB} \rightarrow (13)$$

(2) voltage - shunt feedback amplifier :-

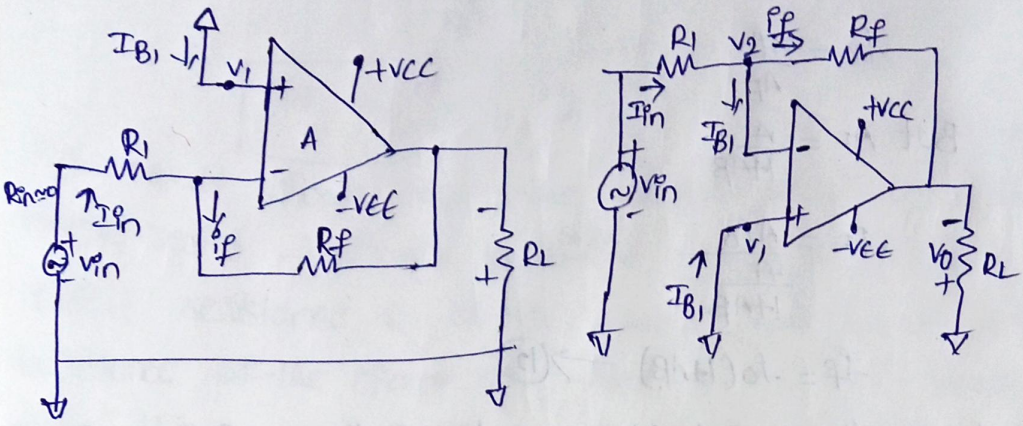


fig:- voltage - shunt feedback amplifier.

In this, the input voltage drives the inverting terminal and the amplified as well as inverted output signal is also applied to the inverting input via feedback resistor R_f. this arrangement forms a -ve f/b because any increase in the output signal results in a feedback signal into the inverting input., causing a decrease in the output signal.

i) closed - loop voltage gain :-

the closed - loop voltage gain A_F of the voltage - shunt feedback amplifier can be obtained by KCL at V_2.

$$i_{in} = i_f + I_{B2} \rightarrow (1)$$

since R_i is very large, I_{B2} is negligibly small

$$\therefore i_{in} \cong i_f$$

$$\frac{V_{in} - V_2}{R_1} = \frac{V_2 - V_0}{R_f} \rightarrow (2)$$

But $V_0 = A(V_1 - V_2)$

$$V_1 - V_2 = \frac{V_0}{A} \qquad (V_1 = 0)$$

$$\boxed{V_2 = -\frac{V_0}{A}}$$

Sub value of V_2 in eau (2) we get

$$\frac{V_{in} + \frac{V_0}{A}}{R_1} = \frac{-(\frac{V_0}{A}) - V_0}{R_f}$$

$$\therefore R_F = \frac{V_0}{V_{in}} = \frac{-ARf}{R_1 + Rf + AR_1} \rightarrow (3)$$

the -ve sign indicates that the i/p & o/p signals are 180° out of phase. since the internal gain of OP-amp(A) is very large (ideally $A = \infty$) i.e $AR_1 \gg R_1 + Rf$

$$\therefore AF = \frac{V_0}{V_{in}} = -\frac{Rf}{R_1} \rightarrow (4) \text{ (Ideal)}$$

this equation shows that the gain of the inverting amplifier is set by selecting ratio of f/B Resistance Rf to the input Resistance R_1. In fact, the ratio $\frac{Rf}{R_1}$ can be set to any value what so ever, even to < 1 due to this property it is used in majority of applications than non-inverting amplifier

Re-writing eau (1)

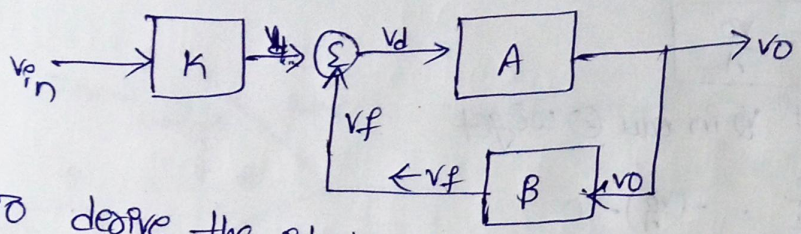
$$A_F = \frac{-A\left(\frac{Rf}{R_1 + Rf}\right)}{1 + \frac{AR_1}{R_1 + Rf}} \rightarrow (5)$$

$$\therefore A_f = \frac{-A_K}{1 + AB}$$

where $K = \frac{Rf}{R_1 + Rf}$, a voltage attenuation factor.

$$\beta = \frac{R_1}{R_1 + Rf}$$

→ overall Block diagram of inverting amplifier



To derive the ideal closed-loop gain, in eqn ⑤ $A\beta \gg 1$

So $(1+A\beta) \cong A\beta$

$$\therefore A_f = \frac{-K}{\beta} = \frac{-\left(\frac{R_f}{R_1+R_f}\right)}{\left(\frac{R_1}{R_1+R_f}\right)}$$

$$= \frac{-R_f}{R_1} \rightarrow ⑥$$

ii) Inverting Input terminal at virtual ground:-

Since the difference input voltage is ideally zero, ie the voltage at V_1 is equal to voltage at V_2 due to virtual ground.

$$i_{in} \cong i_f \rightarrow ⑦$$

$$\frac{V_{in}-V_2}{R_1} = \frac{V_2-V_o}{R_f} \quad (V_2=0)$$

$$\frac{V_{in}}{R_1} = \frac{-V_o}{R_f}$$

$$A_F = \frac{V_o}{V_{in}} = \frac{-R_f}{R_1}$$

iii) Input Resistance with feedback:-

The easiest method of finding the input impedance (or) resistance is to millerize the feedback resistor R_F. Split R_F into its miller components

$$R_{if} = R_1 + \frac{R_f}{1+A} \| R_i \rightarrow ⑧$$

Since R_i & A are very large $\frac{R_f}{1+A} // R_i \cong 0\Omega$

$R_{if} = R_1 \rightarrow (9)$

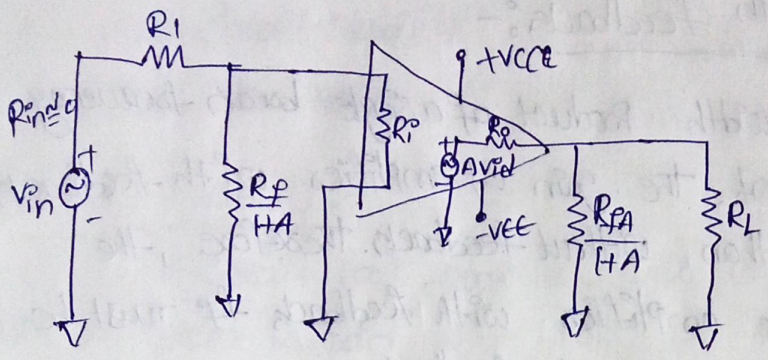


fig:- Inverting amplifier with millerized f/B Resistor.

iv) output resistance with feedback:-

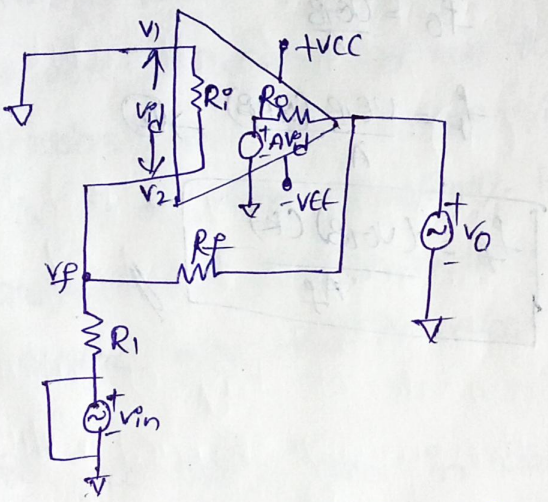


fig:- thevenin's equivalent circuit of inverting amplifier.

The output resistance with feedback R_{of} is the resistance measured at the output terminal of the feedback Amplifier. The output Resistance of non-Inverting amplifier was obtained by using thevenin's theorem. The thevenin's equivalent circuit is exactly the same as that for non-inverting amplifier & the output resistance R_{of} is the same.

$$R_{of} = \frac{R_o}{1+A\beta} \rightarrow (10)$$

v) Bandwidth with feedback:-

* The gain-bandwidth product of a single break frequency is always constant. The gain of amplifier with feedback is always less than without feedback. Therefore, the bandwidth of the amplifier with feedback f_f must be larger than that without feedback.

$$f_f = f_o(1+A\beta) \rightarrow (11)$$

Since $U_{GB} = Af_o$

$$f_o = \frac{U_{GB}}{A}$$

$$f_f = \frac{U_{GB}(1+A\beta)}{A} \rightarrow (12)$$

$$\boxed{f_f = \frac{(U_{GB})(K)}{A_f}}$$

Timer IC 555

Introduction:-

The timer IC 555 is most versatile linear integrated device introduced by signetics corporation in early 1970. It is basically a monolithic timer circuit which can be used in many applications such as monostable and Astable multivibrators, linear ramp generator, Pulse width modulators etc.

Basic Timing circuit:-

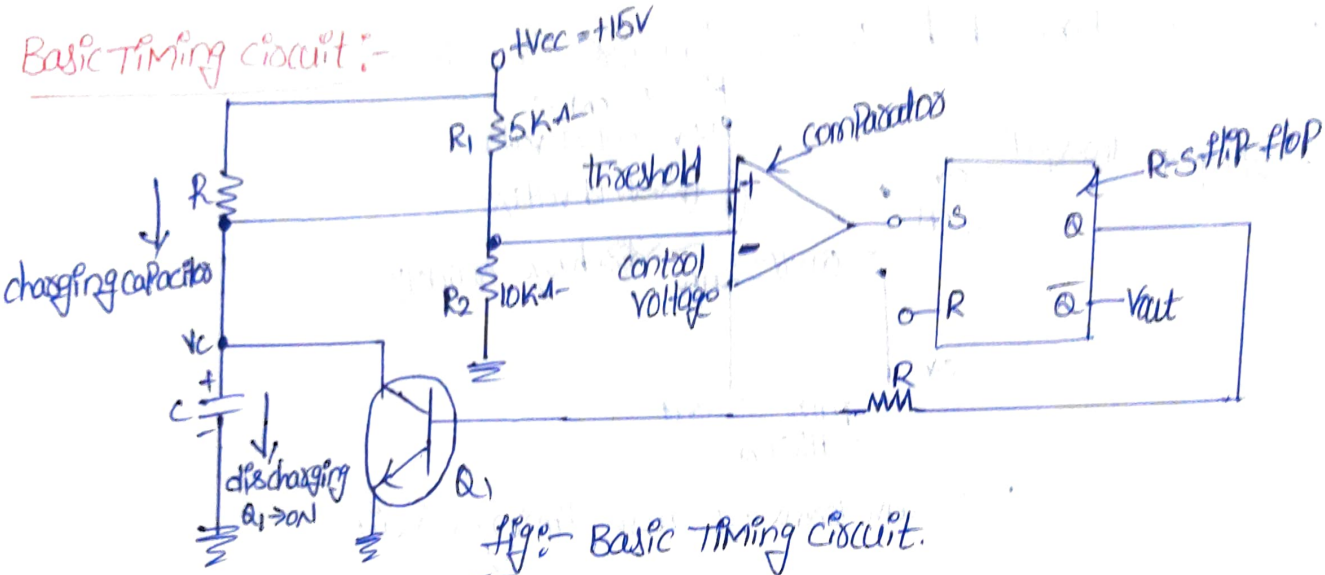


fig:- Basic Timing circuit.

→ consider that the output Q is high. this drives the base of Q_1 and as it is high it drives Q_1 into saturation. It makes the capacitor voltage zero and as other end of capacitor grounded, the capacitor is shorted. In this condition it can't be charged.

→ the circuit uses a comparator the non-inverting input of comparator is called threshold voltage. while it's inverting input is called "control voltage". the R_1 and R_2 forms a potential divider which maintains control voltage constant at +10V. As Q is high and transistor Q_1 is in saturation, the threshold voltage is zero. As $R_1 = 5K\Omega$ and $R_2 = 10K\Omega$

$$\text{control voltage} = \frac{R_2}{R_1+R_2} \times V_{cc} = \frac{10}{5+10} \times 15 = 10V$$

→ Now if high voltage is applied to the reset (R) input of flip-flop then it resets R-S flip-flop and output Q goes low. this drives the

transistor Q_1 in cutt-off. Now the capacitor is free to charge and starts charging through resistance R. the threshold voltage thus starts increasing. when it becomes just greater than +5V which is the control voltage, the comparator output goes high.

→ this high signal is driving the set(S) input of R-S flip-flop. this changes the state of output Q back to high. this drives transistor Q_1 into saturation which quickly discharge the capacitor C.

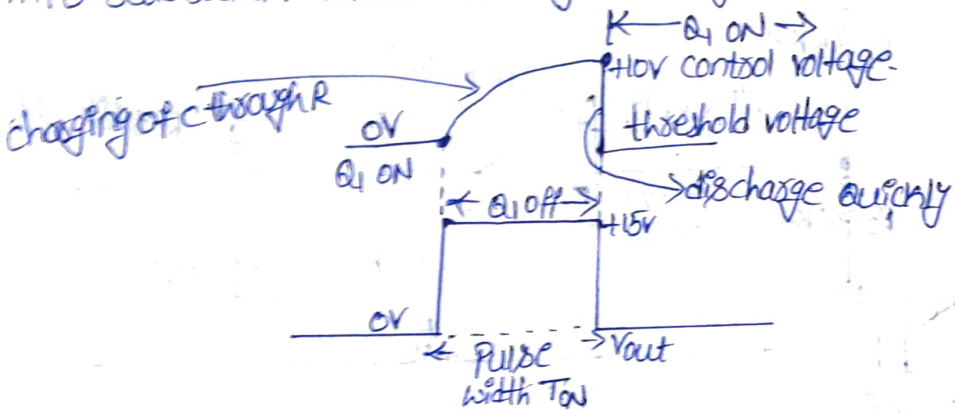


fig:- waveforms of basic timing circuit

=

→ the waveforms of threshold voltage and output voltage Vout. the charging of capacitor is exponential hence the threshold voltage is also exponential in nature. when Q goes low, the $\bar{Q}$ become high and positive going pulse appears at Vout. similarly. when capacitor voltages increases more than the control voltage, Q becomes high and $\bar{Q}$ become low. this brings Vout to zero instantly thus a rectangular output gets produced.

Block diagram of Ic 555:-

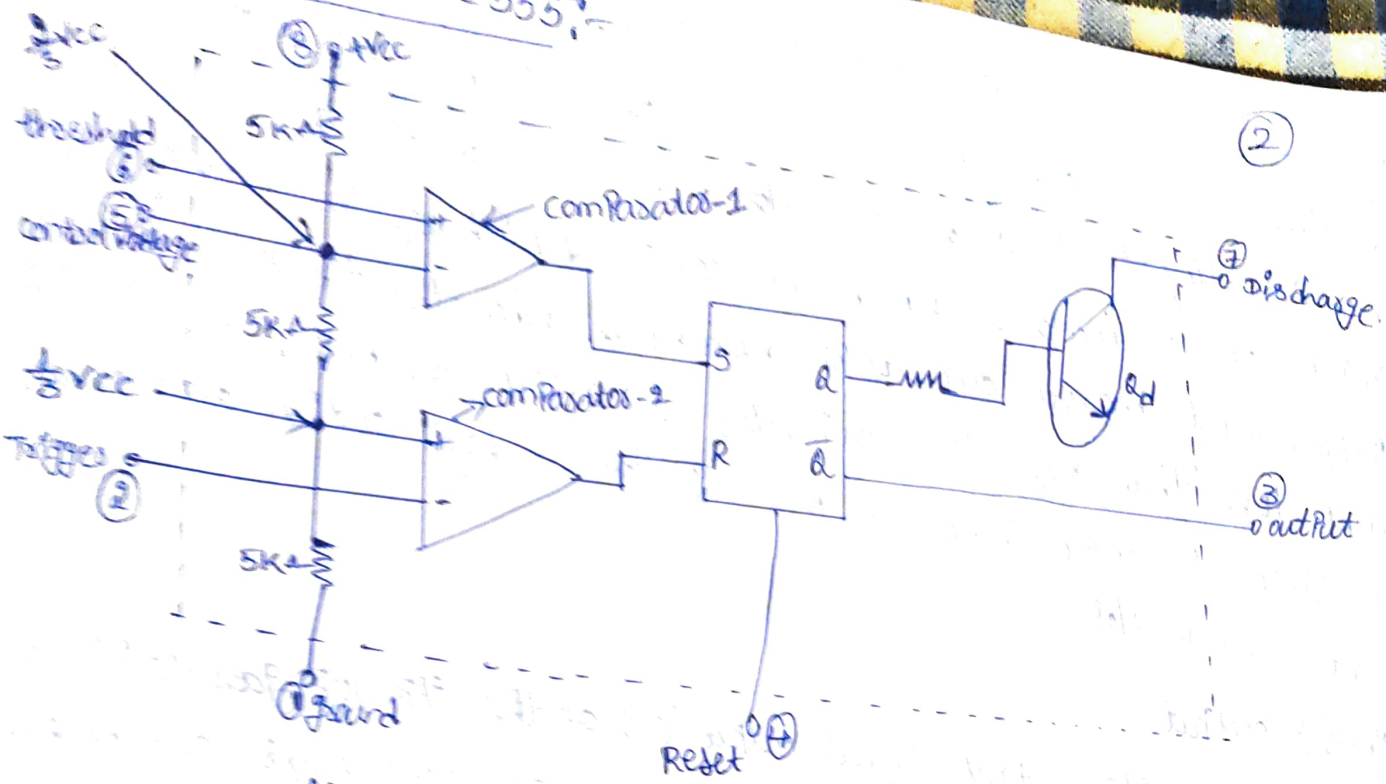


fig ⓐ:- Block diagram of Ic 555 timer.

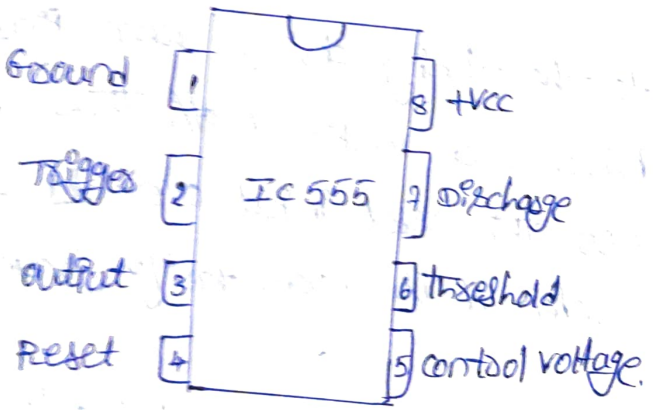


fig ⓑ:- Pin diagram Ic 555

Functions of Pins Ic 555 Timer:-

The Pin numbers of Ic 555 and thier functions are discussed below.

Pin ① :- All the voltages are measured with respect to this terminal.

Pin②:- the Ic 555 uses two comparators. the voltage divider consists of three equal resistances. Due to voltage divider, the voltage of non-inverting terminal of comparator-2 is fixed at $\frac{Vcc}{3}$. the inverting input of comparator-2 which is compared with $\frac{Vcc}{3}$ is nothing but triggers input brought out as pin number 2. when the triggers input is slight less than $\frac{Vcc}{3}$ the comparator-2 output goes high. this output is given to reset input of R-S flip-flop. So high output of comparator-2 reset the flip-flop.

Pin③:- output

the complementary signal output ($\bar{Q}$) of the flip-flop goes to Pin-3 which is the output. the load can be connected in two ways. one between pin 3 and ground which other b/w Pin③ and pin⑧

Pin④:- Reset.

this is an interrupt to the timing device. when Pin④ is grounded it stops the working of device and make it off. thus Pin-④ provides on/off feature to the Ic 555. this reset input overrides all other functions within the timer when it is momentarily grounded.

Pin⑤:- control voltage input.

In most of the applications, external control voltage input is not used. this pin is nothing but the inverting input terminal of comparator-1. the voltage divider holds the voltage of this input at $\frac{2}{3}$ Vcc. this is reference level for comparator-1 with which threshold is compared. If reference level required is other than $\frac{2}{3}$ Vcc for comparator 1 then external input is to be given to Pin⑤

If external input applied to Pin⑤ is alternating then the reference level for comparator-1 keeps on changing above and below $\frac{2}{3}$Vcc. Due to this, the variable Pulse width output is possible. this is called "Pulse width Modulation", which is possible due to Pin⑤.

Pin⑥:- threshold.

this is the noninverting input terminal of comparator-1. the external voltage is applied to this Pin⑥. when this voltage is more than $\frac{2}{3}$Vcc. comparator-1 output goes high. this is given to the set input of R-S flip flop this high output of comparator-1 sets the flip-flop. this makes 'Q' of flip-flop high and $\bar{Q}$ low. thus the output of Ic 555 at Pin③ goes low

Remember that output at Pin 3 is $\bar{Q}$ which is complementary output of flip-flop. In short.

for threshold $> \frac{2}{3}$Vcc, flip-flop → set, Q → high, output at Pin3 → low.

for trigger $< \frac{1}{3}$Vcc, flip-flop → reset, Q → low, output at Pin3 → high.

Pin⑦:- Discharge.

this Pin is connected to the collector of discharge transistor Qd. when the output is high then Q is low and transistor Qd off. It act as an open circuit to the external capacitor c to be connected across it, so capacitor 'c' can charge as described earlier. when output is low, Q is high which drives the base of Qd high, driving transistor Qd in saturation. It acts as short circuit, shorting the external capacitor c to be connected across it.

Pin⑧:- Supply +Vcc.

the Ic 555 timer can work with any supply voltage b/w 4.5V and 18V.

Monostable multivibrator using Ic 555 :-

the Ic 555 timer can be operated as a monostable multivibrator by connecting an external resistor and capacitor as shown in the below figure.

→ the circuit has only one stable state. when trigger is applied, it produces a pulse at the output and returns back to its stable state. the duration of the pulse depends on the value of R and C. As it has only one stable state. It is called one shot multivibrator.

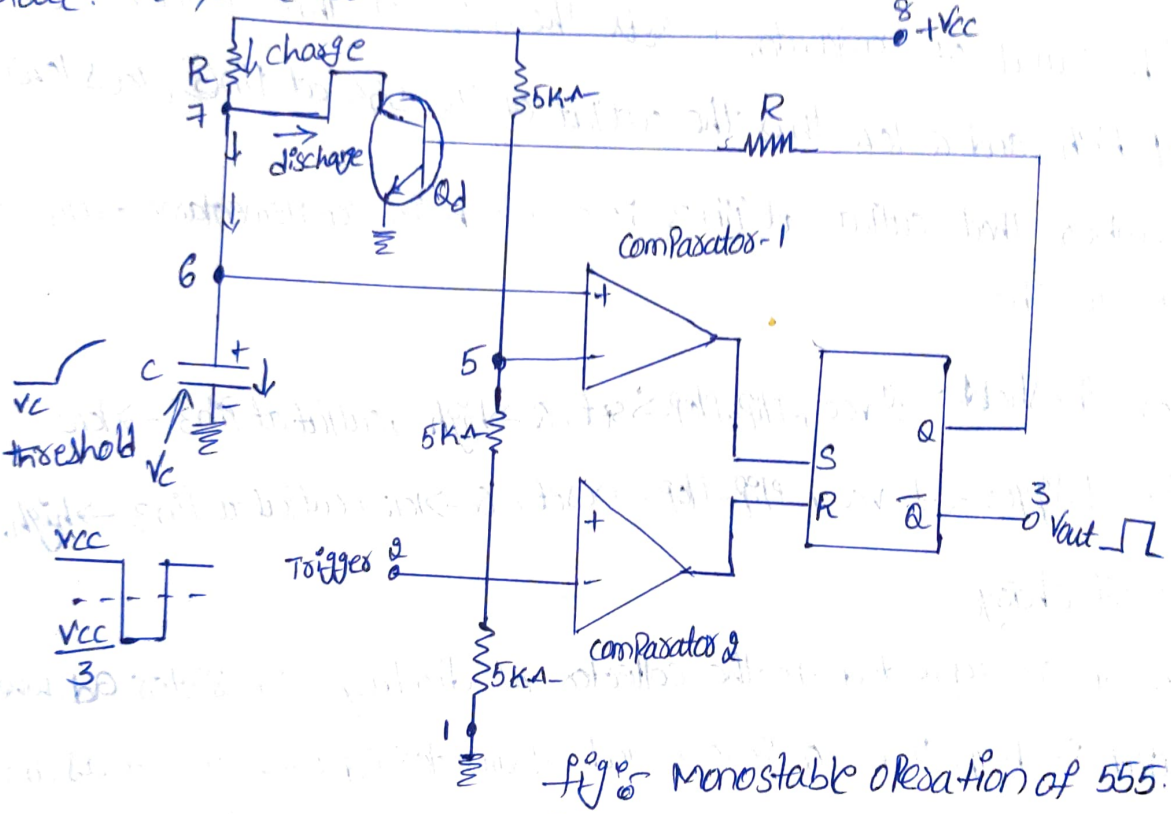


fig:- Monostable operation of 555

operation:-

→ the flip-flop is initially set i.e Q is high. this drives the transistor Qd in saturation. the capacitor discharges completely and voltage across it is nearly zero. the output at Pin3 is low.

→ when a trigger input, a low going pulse is applied, then circuit state remains unchanged till trigger voltage is greater than 1/3 Vcc. when it becomes less than 1/3 Vcc, then comparator 2 output goes high. this resets the flip-flop so 'Q goes low and Q̄ goes high.

low 'Q' makes the transistor Qd off. Hence capacitor starts charging through resistance R, as shown in above figure arrow. (4)

→ the voltage across capacitor increases exponentially. this voltage is nothing but the threshold voltage at Pin(6). when this voltage becomes more than $\frac{2}{3}$Vcc. then comparator-1 output goes high. this sets the flip-flop i.e. Q become high and $\bar{Q}$ low. this high Q drives the transistor Qd in saturation. thus capacitor quickly discharge through Qd as shown above figure

→ so it can be noted that Vout at Pin3 low at start, when trigger is less than $\frac{1}{3}$Vcc. it becomes high and when threshold is greater than $\frac{2}{3}$Vcc again becomes low, till next triggers Pulse occurs. so a rectangular wave is produced at the output. the Pulse width of this rectangular Pulse is controlled by the charging time of capacitor. this depends on the time constant RC. thus RC controls the Pulse width. shown in waveform below.

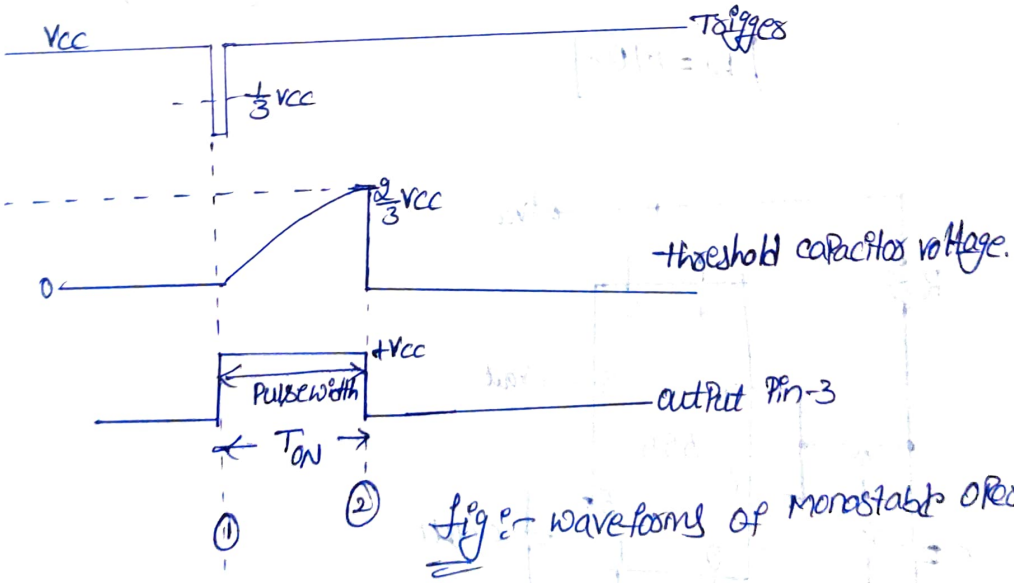


fig:- waveforms of Monostable operation.

Derivation of Pulse-width:-

The voltage across capacitor increases exponentially and is given by

$$V_c = V(1 - e^{-t/CR})$$

If $V_c = \frac{2}{3}V_{cc}$

then $\frac{2}{3}V_{cc} = V_{cc}(1 - e^{-t/CR})$

$$\frac{2}{3} - 1 = -e^{-t/CR}$$

$$\frac{1}{3} = -e^{-t/CR}$$

$$\frac{-t}{CR} = -1.0986$$

$$t = +1.0986CR$$

$$t \approx 1.1CR$$

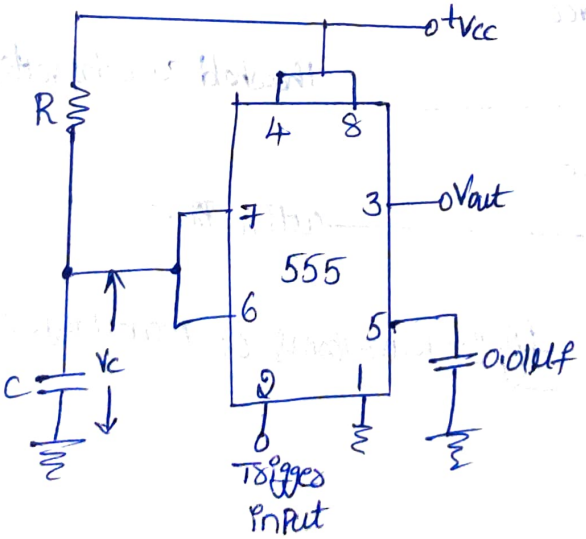
where C → farads, R (Ω), t (sec)

Thus we can say that voltage across capacitor will reach $\frac{2}{3}V_{cc}$ in approximately 1.1 times, time constant i.e $1.1RC$.

Thus the Pulse width denoted as 'w' is given by

$$\boxed{w = 1.1RC}$$

Schematic symbol:-



Applications of Multivibrator (Monostable):-

→ Frequency divider
→ Pulse width Modulation
→ Linear ramp generator
→ Pulse Position Modulation.

Astable Multivibrator using IC 555:-

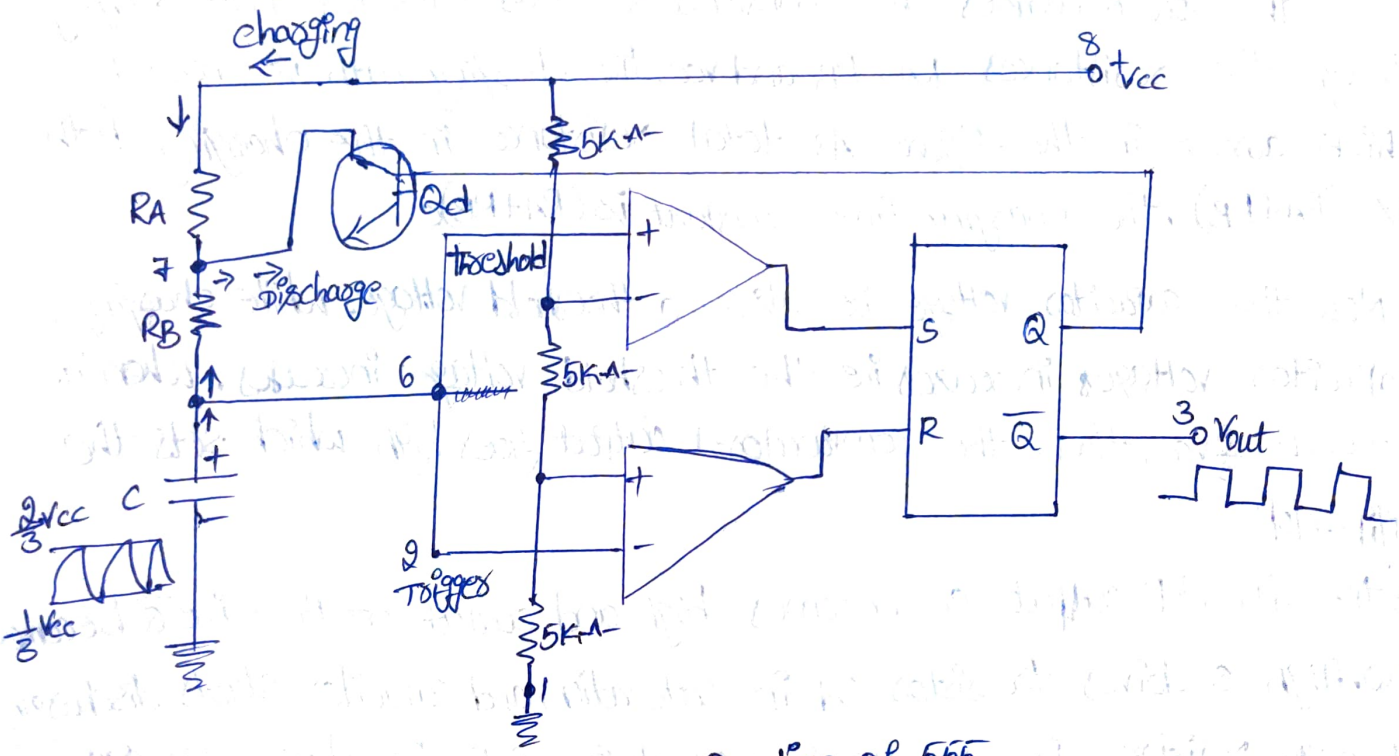


fig:- Astable operation of 555

The above figure shows the IC 555 connected as an Astable multivibrator. The threshold input is connected to the trigger input. Two external resistances RA, RB and capacitor 'C' used in the circuit.

→ this circuit has no stable state. the circuits change its state alternately. hence the operation is called free running non-sinusoidal oscillator.

Opesation:-

when the flip-flop is set, Q is high which drives the transistor Qd in saturation and the capacitor gets discharged. Now the capacitor voltage is nothing but the trigger voltage. so while discharging, when it becomes less than $\frac{1}{3}V_{cc}$, comparator-2 output goes high. this resets the flip-flop hence Q goes low and $\bar{Q}$ goes high.

The low 'Q' makes the transistor off. thus capacitor starts charging through the resistances R_A, R_B and V_{cc}. the charging path is shown by thick arrows in the figure As total resistance in the charging path is (R_A+R_B), the charging time constant is $(R_A+R_B)C$

→Now the capacitor voltage is also a threshold voltage. while charging, capacitor voltage increases ie the threshold voltage increases. when it exceeds $\frac{2}{3}V_{cc}$, then the comparator-1 output goes high which sets the flip-flop.

→the flip-flop output Q becomes high and output at Pin 3 i.e $\bar{Q}$ becomes low. high Q drives transistor Qd in saturation and capacitor starts discharging through resistance R_B and transistor Qd. this path is shown by ~~dotted~~ arrows in the arrow.

→thus the discharging time constant is R_BC. when capacitor voltage becomes less than $\frac{1}{3}V_{cc}$, comparator-2 output goes high, resetting the flip-flop this cycle repeats.

→thus when capacitor is charging, output is high while when it is discharging the output is low. the output is a rectangular wave. the capacitor voltage is exponentially rising and falling. the waveforms are shown below.

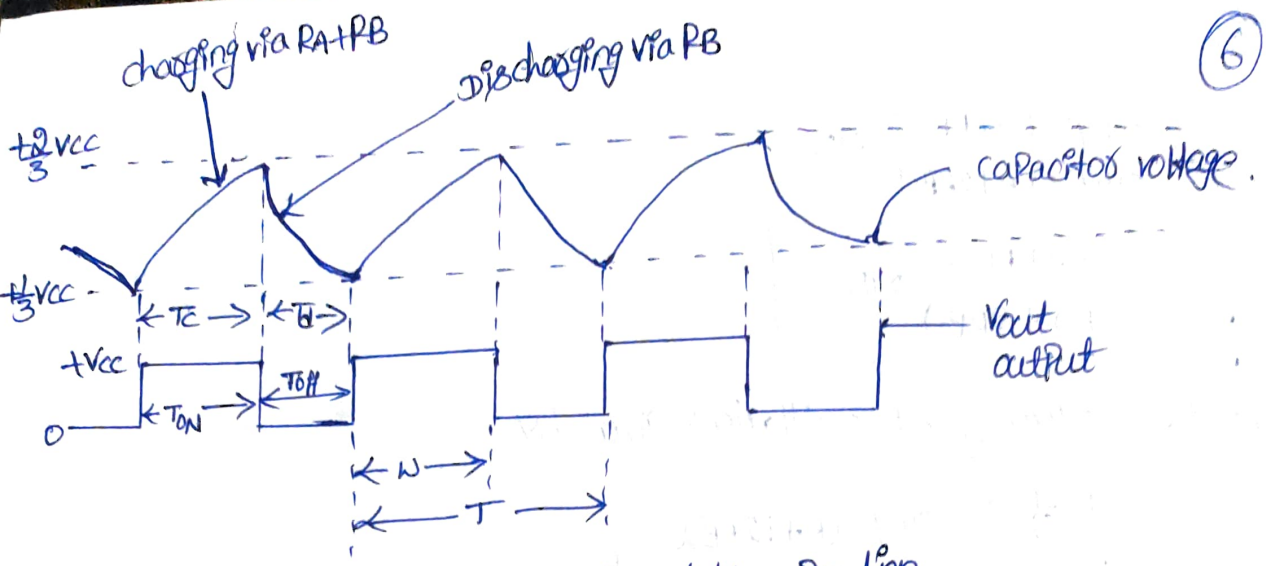


fig:- waveforms of astable operation.

Duty cycle:-

Generally the charging time constant is greater than the discharging time constant. Hence at the output, the waveforms is not symmetric. The high output remains for longer period than low output. The ratio of high output period & low output period is given by mathamatical parameter called duty cycle. It is defined as the ration of 'on' time i.e high output to the total time of one cycle.

W = time for output is high = T_{ON}

T = time of one cycle.

D = duty cycle = $\frac{W}{T}$

$$\%D = \frac{W}{T} \times 100\%$$

The charging time for the capacitor is given by

T_C = charging time = $0.693(R_A+R_B)C$

while discharging time given by

T_d = Discharge time = $0.693R_BC$.

Hence time for one cycle is

$$T = T_C + T_d = 0.693(R_A+R_B)C + 0.693R_BC.$$

While $W = T_C = 0.693(R_A+R_B)C$

$$\%D = \frac{t_2}{T} \times 100$$

$$= \frac{0.693(R_A+R_B)C}{0.693(R_A+2R_B)C} \times 100$$

$$\boxed{\%D = \frac{(R_A+R_B)}{(R_A+2R_B)} \times 100}$$

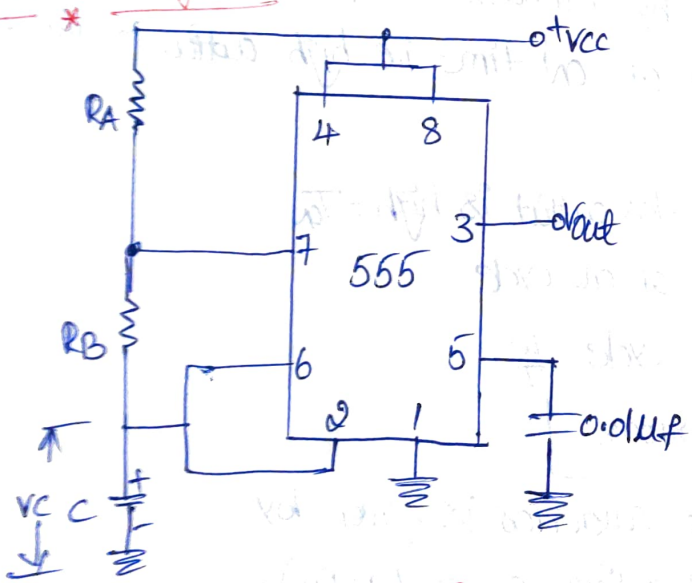
While the frequency of oscillations given by

$$f = \frac{1}{T} = \frac{1}{0.693(R_A+2R_B)C}$$

$$\boxed{f = \frac{1.44}{(R_A+2R_B)C} \text{ Hz}}$$

If R_B is much smaller than R_B, duty cycle approaches to 50% and output waveform approaches to square wave.

Schematic Diagram :-



Applications of Astable multivibrator :-

1) Square wave generator
2) voltage controlled oscillator (VCO)
3) FSK generator

8.5 SCHMITT TRIGGER

The use of 555 timer as a Schmitt Trigger is shown in Fig. 8.24. Here the two internal comparators are tied together and externally biased at $V_{CC}/2$ through R_1 and R_2. Since the upper comparator will trip at (2/3) V_{CC} and lower comparator at (1/3) V_{CC}, the bias provided by R_1 and R_2 is centered within these two thresholds.

Thus, a sine wave of sufficient amplitude ($> V_{CC}/6 = 2/3\ V_{CC} - V_{CC}/2$) to exceed the reference levels causes the internal flip-flop to alternately set and reset, providing a square wave output as shown in Fig. 8.25.

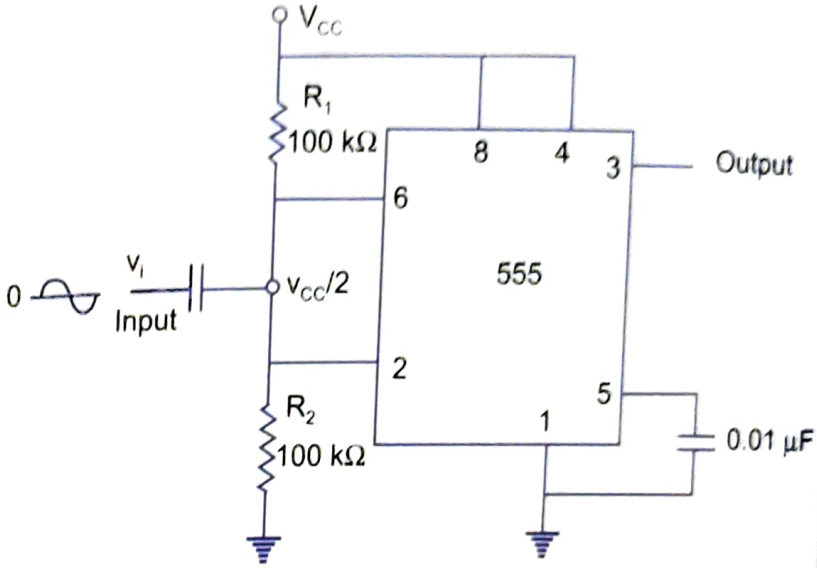


Fig. 8.24 Timer in Schmitt Trigger Operation

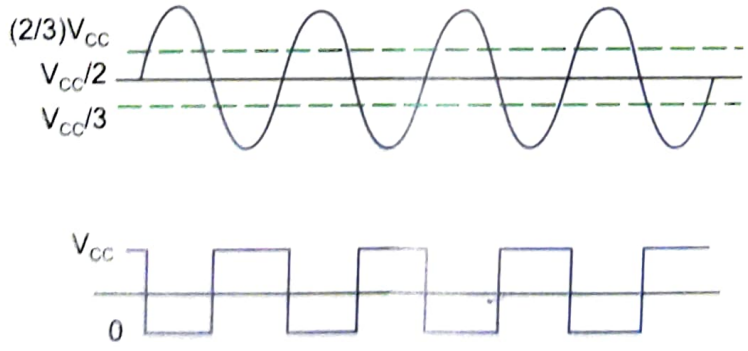


Fig. 8.25 Input output waveforms of Schmitt Trigger

It may be noted that unlike conventional multivibrator, no frequency division is taking place and frequency of square wave remains the same as that of input signal.

9.4 VOLTAGE CONTROLLED OSCILLATOR (VCO)

A common type of VCO available in IC form is Signetics NE/SE566. The pin configuration and basic block diagram of 566 VCO are shown in Fig. 9.7 (a, b). Referring to Fig. 9.7 (b), a timing capacitor C_T is linearly charged or discharged by a constant current source/sink. The amount of current can be controlled by changing the voltage v_c applied at the modulating input (pin 5) or by changing the timing resistor R_T external to IC chip. The voltage at pin 6 is held at the same voltage as pin 5. Thus, if the modulating voltage at pin 5 is increased, the voltage at pin 6 also increases, resulting in less voltage across R_T and thereby decreasing the charging current.

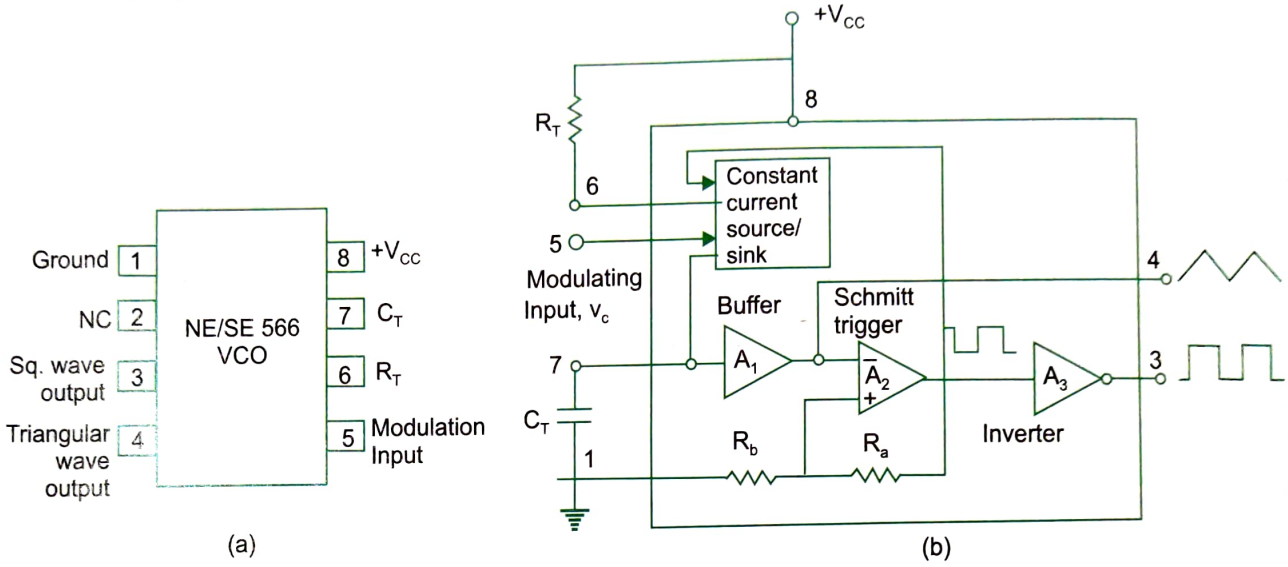
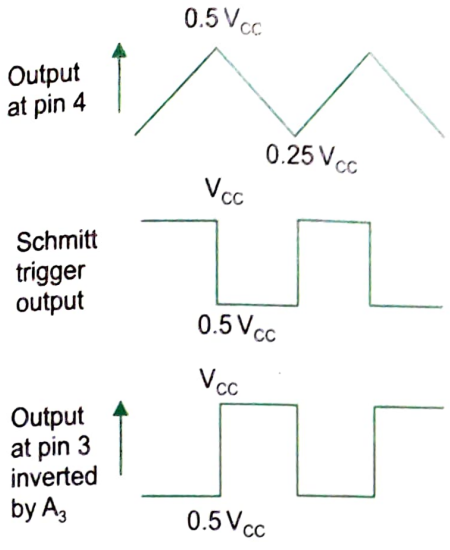


Fig. 9.7 Voltage controlled oscillator (a) Pin configuration (b) Block diagram

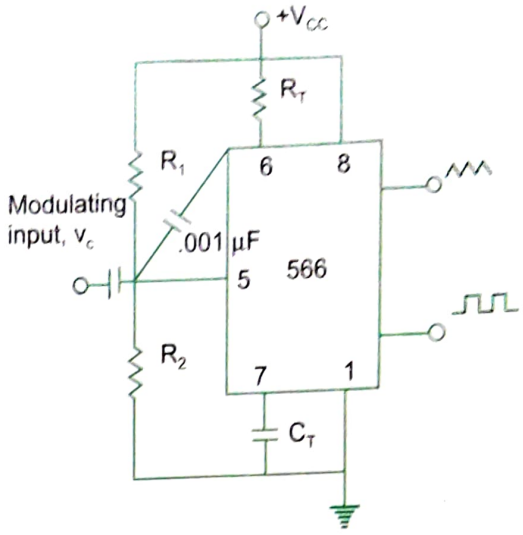
A small capacitor of .001 μF should be connected between pin 5 and 6 to eliminate possible oscillations. A VCO is commonly used in converting low frequency signals such as EEGs, EKG into an audio frequency range. These audio signals can be transmitted over telephone lines or a two way radio communication systems for diagnostic purposes or can be recorded on a magnetic tape for further reference.

The voltage across the capacitor C_T is applied to the inverting input terminal of Schmitt trigger A_2 via buffer amplifier A_1. The output voltage swing of the Schmitt trigger is designed to V_{CC} and 0.5 V_{CC}. If $R_a = R_b$ in the positive feedback loop, the voltage at the non-inverting input terminal of A_2 swings from 0.5 V_{CC} to 0.25 V_{CC}. In Fig. 9.7 (c), when the voltage on the capacitor C_T exceeds 0.5 V_{CC} during charging, the output of the Schmitt trigger goes LOW (0.5 V_{CC}). The capacitor now discharges and when it is at 0.25 V_{CC}, the output of Schmitt trigger goes HIGH (V_{CC}). Since the source and sink currents are equal, capacitor charges and discharges for the same amount of time. This gives a triangular voltage waveform across C_T which is also available at pin 4. The square wave output of the Schmitt trigger is inverted* by inverter A_3 and is available at pin 3. The inverter A_3 is basically a current amplifier used to drive the load. The output waveforms are shown in Fig. 9.7 (c).

The output frequency of the VCO can be calculated as follows:



(c)



(d)

Fig. 9.7 (c) Output waveform (d) Typical connection diagram

The total voltage on the capacitor changes from 0.25 V_{CC} to 0.5 V_{CC}. Thus $\Delta v = 0.25\ V_{CC}$. The capacitor chargers with a constant current source.

So
$$\frac{\Delta v}{\Delta t} = \frac{i}{C_T}$$

or,
$$\frac{0.25\ V_{CC}}{\Delta t} = \frac{i}{C_T}$$

or,
$$\Delta t = \frac{0.25\ V_{CC} C_T}{i} \qquad (9.8)$$

The time period T of the triangular waveform = $2\Delta t$. The frequency of oscillator f_o is,

$$f_o = \frac{1}{T} = \frac{1}{2\,\Delta t} = \frac{i}{0.5\ V_{CC} C_T}$$

But,
$$i = \frac{V_{CC} - v_c}{R_T} \qquad (9.9)$$

where, v_c is the voltage at pin 5. Therefore,

$$f_o = \frac{2(V_{CC} - v_c)}{C_T R_T V_{CC}} \qquad (9.10)$$

The output frequency of the VCO can be changed either by (i) R_T, (ii) C_T or (iii) the voltage v_c at the modulating input terminal pin 5. The voltage v_c can be varied by connecting a R_1R_2 circuit as shown in Fig. 9.7 (d). The components R_T and C_T are first selected so that VCO output frequency lies in the centre of the operating frequency range. Now the modulating input voltage is usually varied from 0.75 V_{CC} to V_{CC} which can produce a frequency variation of about 10 to 1. With no modulating input signal, if the voltage at pin 5 is biased† at (7/8) V_{CC}, Eq. (9.10) gives the VCO output frequency as,

† The expression of f_o depends upon the initial choice of the voltage v_c. If the value of v_c is taken as 0.85 V_{CC} then f_o comes out to be $0.3/R_TC_T$.

$$f_o = \frac{2(V_{CC} - (7/8)\, V_{CC})}{C_T\, R_T\, V_{CC}} = \frac{1}{4R_T\, C_T} = \frac{0.25}{R_T\, C_T} \tag{9.11}$$

Voltage to Frequency Conversion Factor

A parameter of importance for VCO is voltage to frequency conversion factor K_v and is defined as

$$K_v = \frac{\Delta f_o}{\Delta v_c}$$

Here Δv_c is the modulation voltage required to produce the frequency shift Δf_o for a VCO. If we assume that the original frequency is f_o and the new frequency is f_1, then

$$\Delta f_o = f_1 - f_o = \frac{2(V_{CC} - v_c + \Delta v_c)}{C_T\, R_T V_{CC}} - \frac{2(V_{CC} - v_c)}{C_T R_T V_{CC}} = \frac{2\,\Delta v_c}{C_T R_T V_{CC}} \tag{9.12}$$

or,
$$\Delta v_c = \frac{\Delta f_o\, C_T R_T V_{CC}}{2} \tag{9.13}$$

Putting the value of $C_T R_T$ from Eq. (9.11)

$$\Delta v_c = \Delta f_o\, V_{CC}/8 f_o \tag{9.14}$$

or,
$$K_v = \frac{\Delta f_o}{\Delta v_c} = \frac{8\, f_o}{V_{CC}} \tag{9.15}$$

9.5 LOW PASS FILTER

UNIT - III

Filters

Active filters:

A filter is a circuit that is designed to pass a specific band of frequencies while attenuating all the signals outside the band. It is a frequency selective circuit.

The filters are basically classified as active & passive filters. The "passive filter" networks use only passive elements such as resistors, inductors & capacitors while "Active filter" circuit use the active elements such as op-amps, transistors along with resistors, inductors & capacitors. Modern active filters donot use inductors as the inductors are bulky, heavy & non-linear.

First Order Low pass butterworth filter:-

The first order low pass butterworth filter is realised by R-C circuit used along with an op-amp, used in non-inverting configuration.

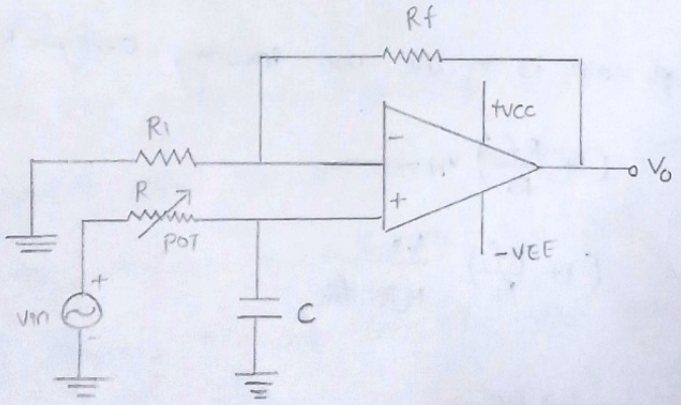


Fig: First order low pass butterworth filter

This filter is also called "one pole low pass butterworth filter".

Analysis :-

The impedence of the Capacitor C is $-jX_C$ where X_C is the Capacitive reactance given by $X_C = \frac{1}{2\pi fC}$.

By the potential divider rule, the voltage at the non inverting input terminal A which is the voltage across Capacitor C is given by

$$V_A = \frac{-jX_C}{R - jX_C} V_{in} \longrightarrow (1)$$

$$V_A = -j\left(\frac{1}{2\pi fC}\right) \cdot V_{in}$$

$$V_A = \frac{-j}{2\pi fRC - j} \cdot V_{in}$$

$$V_A = \frac{V_{in}}{1 - \frac{2\pi fRC}{j}}$$

$$\therefore V_A = \frac{V_{in}}{1 + j2\pi fRC} \longrightarrow (2) \qquad \left(-j = \frac{1}{j} \text{ & } \frac{-1}{j} = j\right)$$

As the op-amp is in the non-inverting configuration

$$V_o = \left(1 + \frac{Rf}{R_1}\right) V_A$$

$$V_o = \left(1 + \frac{Rf}{R_1}\right) \frac{V_{in}}{1 + j2\pi fRC}$$

$$\therefore \frac{V_o}{V_{in}} = \frac{A_F}{1 + j\left(\frac{f}{f_H}\right)} \longrightarrow (3)$$

where

$A_F = \left(1 + \frac{Rf}{R_1}\right)$ = Gain of filter in pass band

$f_H = \frac{1}{2\pi RC}$ = high cutoff frequency of filter

f = operating frequency

The $\frac{V_o}{V_{in}}$ is the transfer function of the filter & can be expressed in the polar form as

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+\left(\frac{f}{f_H}\right)^2}} \rightarrow (4)$$

$$\phi = -\tan^{-1}\left(\frac{f}{f_H}\right) \rightarrow (5)$$

1. At very low frequencies, $f < f_H$

$$\left|\frac{V_o}{V_{in}}\right| \cong A_F \text{ i.e constant}$$

2. At $f = f_H$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{2}} = 0.707\ A_F \text{ i.e } 3\,dB \text{ down to level of } A_F$$

3. At $f > f_H$

$$\left|\frac{V_o}{V_{in}}\right| < A_F$$

Thus, for the range of frequencies, $0 < f < f_H$, the gain is almost constant equal to f_H which is high cutoff frequency. At $f = f_H$ gain reduces to $0.707\ A_F$ i.e 3dB down from A_F & as the frequency increases than f_H, the gain decreases at a rate of 20dB / decade. The rate 20dB / decade means decrease of 20dB in gain per 10 times change in frequency. The frequency f_H is called "cutoff frequency", "break frequency", "-3 dB frequency", "or" corner frequency.

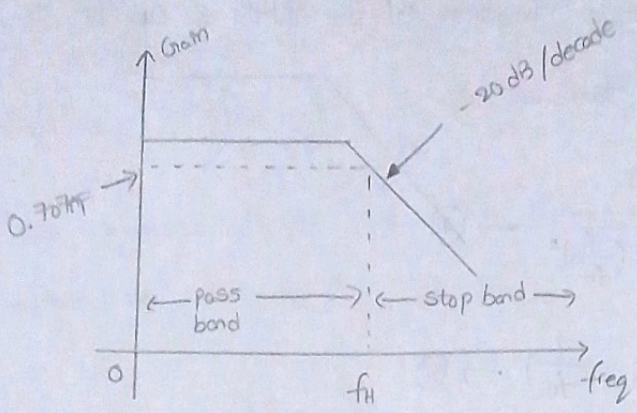


fig: Frequency response

Design Steps :-

1. Choose the cutoff frequency, f_H.
2. Choose the capacitance C usually between 0.001 and 1μF. Generally it is selected as 1μF or less than that.
3. Now for RC circuit $f_H = \frac{1}{2\pi RC}$
4. Select R_F & R_1 to get the desired gain $A_F = 1 + \frac{R_F}{R_1}$

Frequency Scaling :-

Once the filter is designed sometimes, it is necessary to change the value of cut-off frequency f_H. The method used to change the cut-off frequency f_H to a new cut-off frequency f_{H1} is called "frequency scaling".

To achieve such a frequency scaling, the standard value capacitor C is selected first. The required cut-off frequency

Can be achieved by calculating corresponding value of resistance R. But to achieve frequency scaling a potentiometer. Thus, the resistance R is generally a potentiometer with which required cut off frequency f_H can be adjusted & changed later on if required.

First order High pass Butterworth filter :-

A high pass filter is a circuit that attenuates all the signals below specific cut off frequency denoted as f_L. The high pass filter circuit can be obtained by interchanging frequency determining resistance & capacitors in low pass filter circuit.

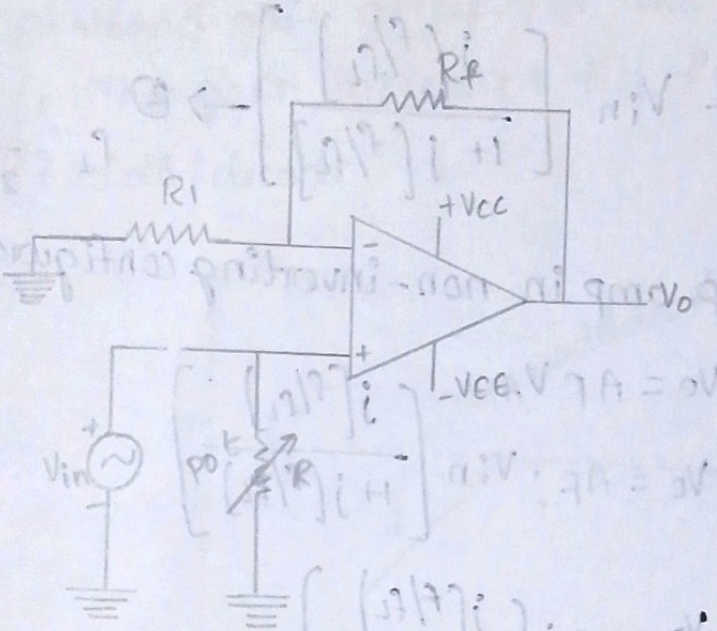


Fig: First order high pass Butterworth filter

Analysis :

By voltage divider rule, the potential of the non inverting terminal of op-amp is

$$V_A = \left[\frac{R}{R - jX_C}\right] V_{in} \longrightarrow (1)$$

$$V_A = \frac{R}{-jX_C\left[\frac{R}{-jX_C} + 1\right]} \cdot V_{in} \qquad -\frac{1}{j} = j$$

$$\therefore \frac{-1}{jX_C} = \frac{j}{X_C} = \frac{j}{\frac{1}{2\pi fC}} = j2\pi fC$$

$$V_A = V_{in}\left[\frac{\left[\frac{-R}{jX_C}\right]}{1+\left[\frac{-R}{jX_C}\right]}\right]$$

$$= V_{in}\left[\frac{j2\pi fRC}{1+j2\pi fRC}\right]$$

$$V_A = V_{in}\left[\frac{j\left[f/f_L\right]}{1+j\left[f/f_L\right]}\right] \longrightarrow (2) \qquad f_L = \frac{1}{2\pi RC}$$

Now, for op-amp in non-inverting configuration

$$V_o = A_F V_A$$

$$V_o = A_F \cdot V_{in}\left[\frac{j\left[f/f_L\right]}{1+j\left(f/f_L\right)}\right]$$

$$\frac{V_o}{V_{in}} = A_F\left[\frac{j\left[f/f_L\right]}{1+j\left[f/f_L\right]}\right] \longrightarrow (3)$$

The magnitude of transfer function, which is given by $\left|\frac{V_o}{V_{in}}\right| = \frac{A_F\left[f/f_L\right]}{\sqrt{1+\left[f/f_L\right]^2}} \longrightarrow (4)$

1. At low frequencies, $f < f_L$

$$\therefore \left|\frac{V_o}{V_{in}}\right| < A_F$$

2. At $f = f_L$

$$\left|\frac{V_o}{V_{in}}\right| = 0.707 A_F$$

3. At $f > f_L$ i.e high frequencies, 1 can be neglected as compared to $[f/f_2]$ from denominator

$$\left|\frac{V_o}{V_{in}}\right| \cong A_F$$

Thus, the circuit acts as high pass filter with a passband gain as A_F For the frequencies, $f < f_L$, the gain increases till $f = f_L$ at a rate of +20 dB/decade.

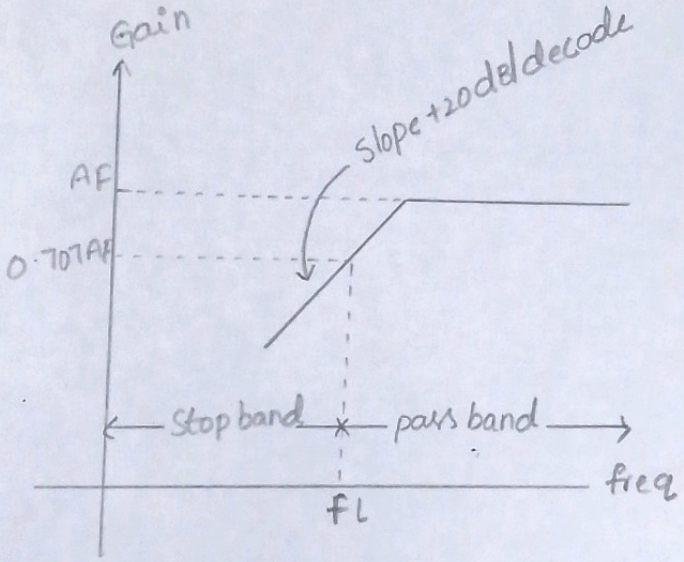
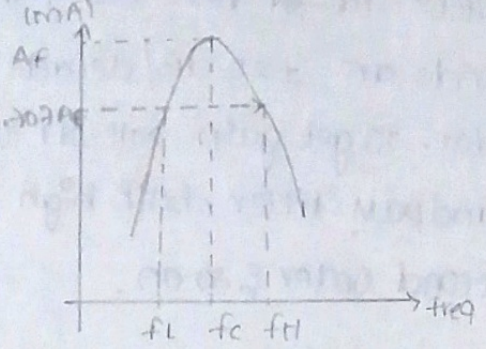


Fig: Frequency response

Band Pass filters:

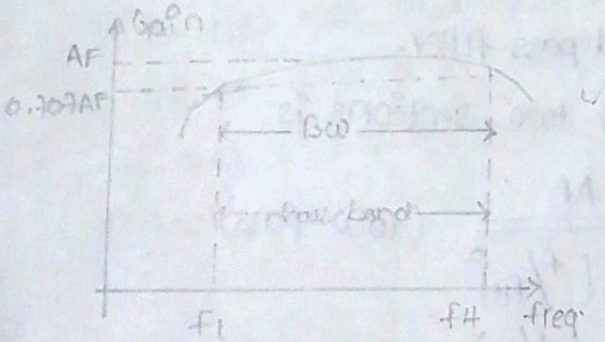
A band pass filter is basically a frequency selectors. It allows one particular band of frequencies to pass. Thus, the pass band is between the two cut-off frequencies f_H & f_L, ($f_H > f_L$)

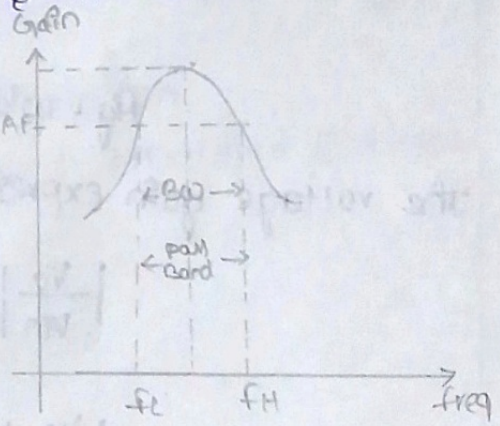


There are two types of band pass filter which are classified based on "figure of merit" or "quality factor (Q)"

(i) for Q<10, the bandpass filter is called wide bandpass filter. In this, the bandpass is wide & we get large band width.

(ii) for Q>10, the bandpass filter is called narrow bandpass filter. The bandpass is very narrow & band width is very small. Higher the value of Q, narrower is pass band & more selective is filter.





The gain roll off for $f < f_L$ is +20 dB/decade while $f > f_H$ is -20 dB/decade

for wide bandpass filter, the centre frequency is given by.

$$f_c = \sqrt{f_L f_H}$$

The relationship between Q & 3dB bandwidth with f_c is given by

$$Q = \frac{f_c}{BW} = \frac{f_c}{f_H - f_L}$$

Wide bandPass filter :-

The wide bandpass filter can be realised by simply cascading a high pass filter & low pass filter. If both high pass & low pass filters are of first order, the gain roll off in both the stop bands are ±20 dB/decade & wide bandpass filter is of first order. To get gain call off ±40 dB/decade & second order wide bandpass filter, both high pass & low pass filters must be of second order & so on.

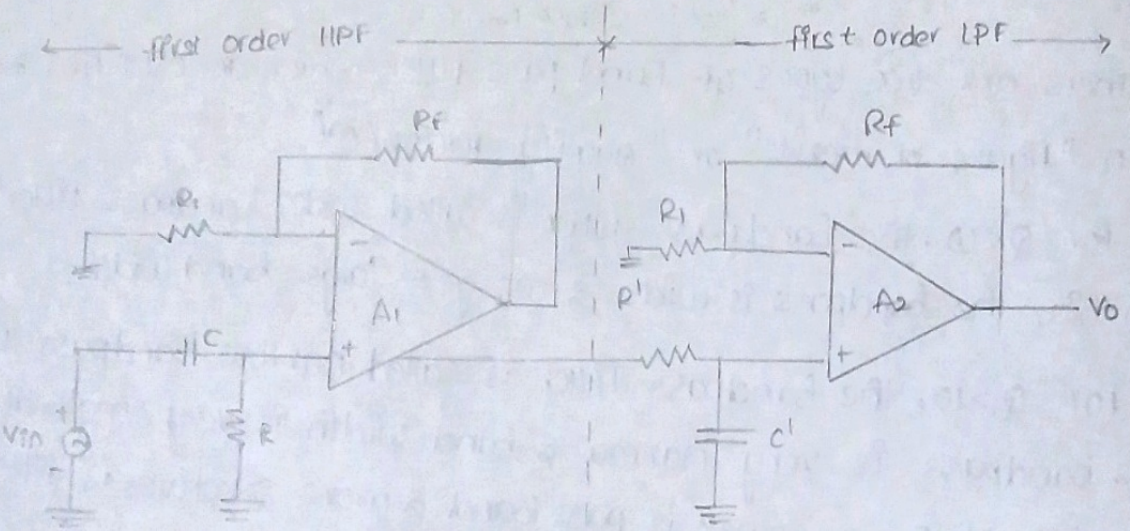


fig: wide band pass filter.

The voltage gain expression for two sections is

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_f}{\sqrt{1+\left[f/f_H\right]^2}} \quad \text{(low pass)}$$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_f\,(f/f_L)}{\sqrt{1+\left(\frac{f}{f_L}\right)^2}} \quad \text{(High pass)}$$

As the two circuits are in cascade, the overall gain of wide band pass filter is the product of two gains.

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_{FT}\,(f/f_L)}{\left[\sqrt{1+(f/f_L)^2}\right]\left[\sqrt{1+(f/f_H)^2}\right]}$$

where, $A_{FT} = A_1 A_2$ = Total pass band gain.

A_1 = Gain of HPF

A_2 = Gain of LPF

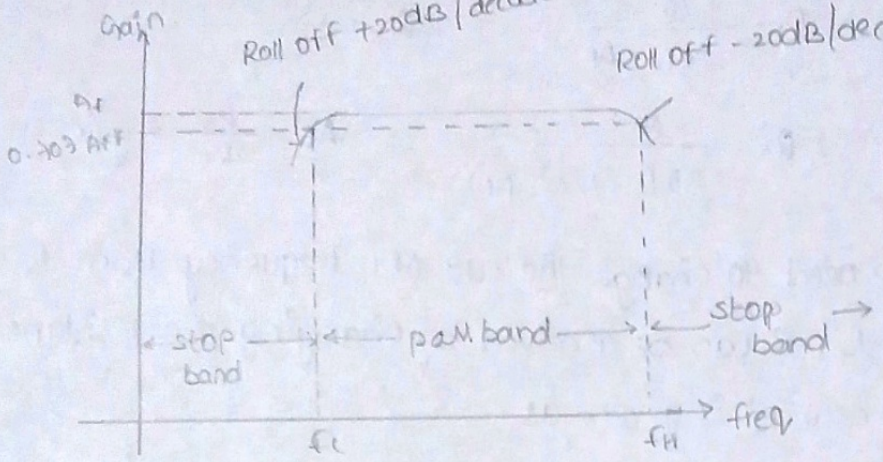


fig: frequency response.

Narrow bandpass filter :-

The narrow bandpass filters uses only one op-amp as against two by wide bandpass filter. It has following features.

(i) It has two feed back paths

(ii) the op-amp is in inverting configuration.

Due to two feed back paths, it is called "multiple feedback filter".

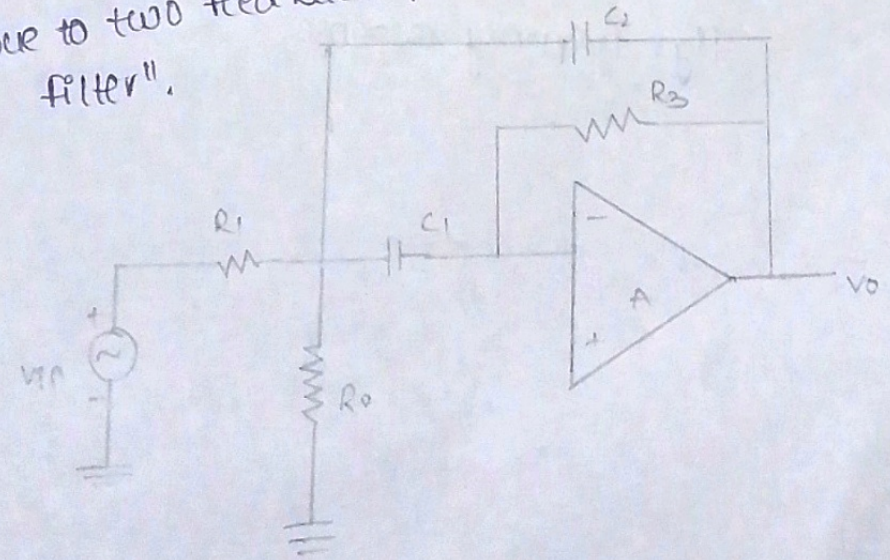


fig: Narrow bandpass filter.

The important parameters of narrow bandpass filters are f_L, f_H, f_c, gain at center frequency (A_f) & Quality factor Q. The relationship of components with the various parameters are,

$$R_1 = \frac{Q}{2\pi f_c C A_f} \qquad R_3 = \frac{Q}{\pi f_c C}$$

$$R_2 = \frac{Q}{2\pi f_c (2Q^2 - A_f)} \qquad A_f = \frac{R_3}{2R_1} = \text{gain at } f_c$$

If we need to change the cut off frequency from f_c to a new value f_c', it can be acheived by changing the resistance R_2.

The new R_2' is given as,

$$R_2' = R_c \left(\frac{f_c}{f_c'}\right)^2$$

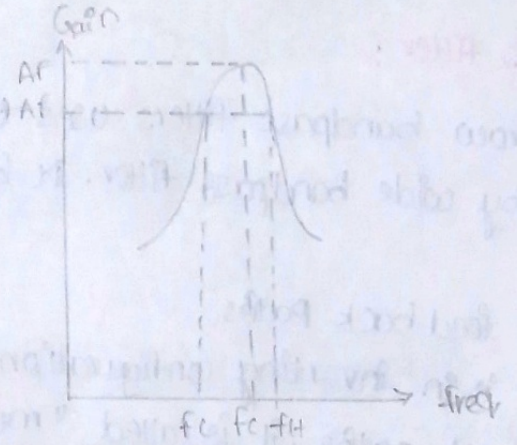


fig: frequency response.

Band Elimination Filter :

A filter which rejects a specific band of frequencies is known as band stop filter or band filter. This filter has two pass bands and one stop band. A band of frequencies is attenuated by this filter, hence the name elimination filter. This filter is classified as

(i) Wide band reject filter ($Q<10$)

(ii) Narrow band reject filter ($Q>10$)

Wide band Reject filter :

Similar to wide band pass filter, this filter also consists of high pass & low pass filter sections, with a summing amplifier.

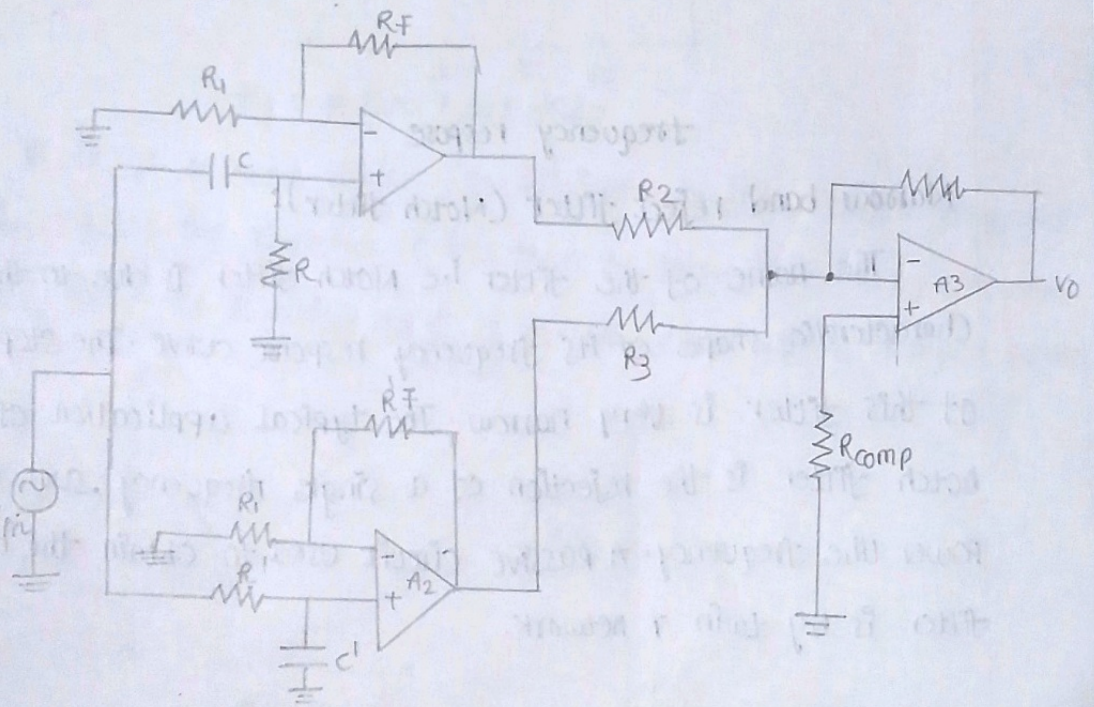


fig : Wide band reject filter

To have a satisfactory operation of this filter it has to satisfy

(i) The low cutoff frequency, ~~f_H of high low pass filter~~ f_L of high pass filter must be greater than the high cutoff frequency, f_H of low pass filter.

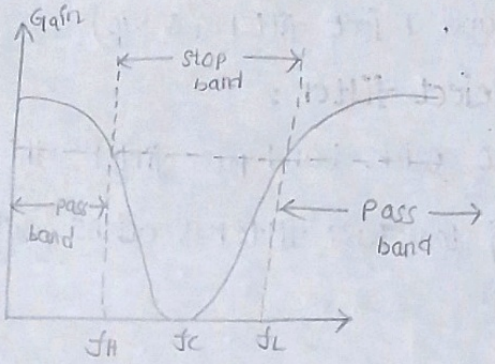
(iv) The pass band gain of LPF and HPF must be equal. The gain of the summing amplifier should be set to unity

$$R_2 = R_3 = R_4 = R$$

$$R_{comp} = R_2 \| R_3 \| R_4 = \frac{R}{3}$$

Both high pass & low pass sections provide attenuation in the stop band between f_H & f_L. for $f < f_H$, the transmission is due to low pass section while for $f > f_L$, the transmission is due to high pass section. The centre frequency, f_c is given by

$$f_c = \sqrt{f_H f_L}$$



frequency respose

Narrow band reject filter (Notch filter):

The name of the filter i.e Notch filter is due to the characteristic shape of its frequency response curve. The stop band of this filter is very narrow. The typical application of the notch filter is the rejection of a single frequency, such as 50 Hz power line frequency. A passive circuit used to obtain the notch filter is by twin T network.

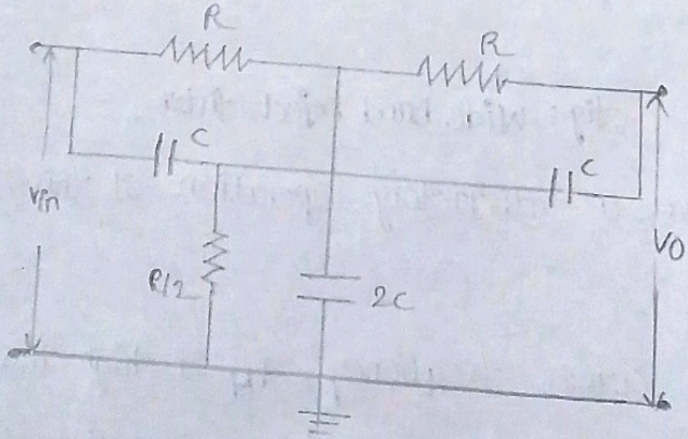


fig: Twin T- network

It consists of two T networks. one consists of two resistors & a capacitor while other consists of two capacitors & one resistor. The notch out frequency is the frequency at which the maximum attenuation occur is given by

$$f_N = \frac{1}{2\pi RC} \rightarrow (1)$$

The value of Q i.e figure of merit for passive network is very low, hence an active notch filter which uses twin T network is prepared.

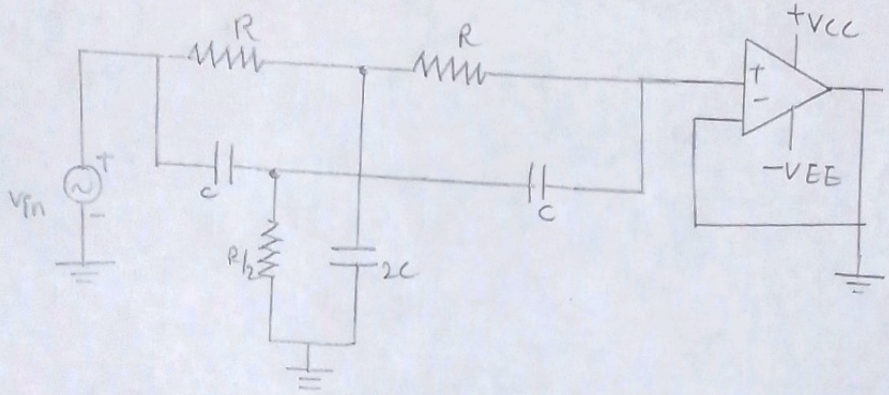
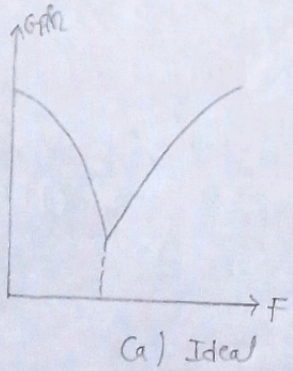
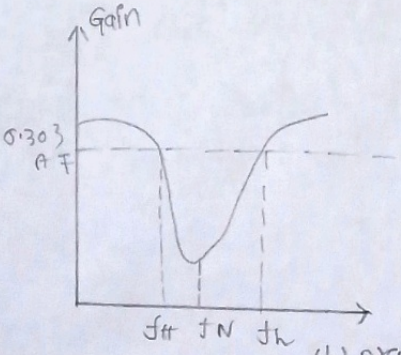


fig : Active notch filter

To design a notch filter, to eliminate specific notch frequency f_N, choose the capacitor C less than or equal to 1 μF, calculate the value of R using eq (1) & set the circuit with precise values.



(a) Ideal



(b) practical

All pass filter

The filters which are discused uptill now are used to adjust the magnitude of the transfer function of the circuit. But, this also alters the phase angle characteristics of the circuit. It is many times required to control the phase response of the filter. The filter which is used to control the phase response by adding a phase shift between input and output signals is called as all the pass filter. Its gain is one for all the frequenices. Thus, as name suggests, it passes all the frequencies of the input signal. It does not produce any attenuation but provides the required phase shift for the different frequencies of the input signal.

for example, when signals are transmitted over the transmission lines, there is change in their phase. To compensate for such phase change, all pass filters are used. Hence, all pass filters are used. Hence, all pass filters are called as delay equalizers or phase correctors.

The fig 6.37 shows the simple first order all pass filter

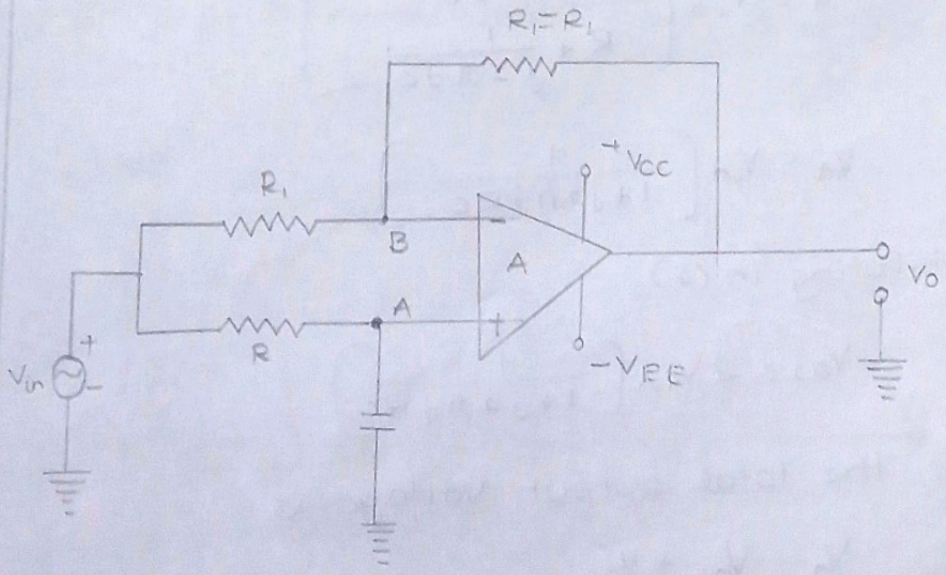


fig. 6.37 All pass filter

6.11.1 Analysis of the circuit

Let us use the superposition principle to obtain the expression for the output voltage V_o

Assume input to the non-inverting terminal zero. The circuit acts as an inverting amplifier

$$V_{o1} = -\frac{R_f}{R_1} V_{in}$$

$$V_{o1} = -V_{in} \quad \text{as} \quad R_f = R_1$$

Now, assume input to the inverting terminal zero. The circuit acts as a non-inverting amplifier

$$V_{o2} = \left(1 + \frac{R_f}{R_1}\right) V_A$$

$$V_{o2} = 2V_A \quad \text{as} \quad R_f = R_1$$

V_A = voltage at node A

By the potential divider rule, the voltage V_A can be obtained as

$$V_A = V_m \left[\frac{-jX_c}{R - jX_c}\right]$$

where $-jX_c = -j\left(\frac{1}{2\pi fc}\right)$

$$= \left(\frac{1}{j2\pi fc}\right) \text{as} -j = \frac{1}{j}$$

$$V_A = V_{in}\left[\frac{\frac{1}{j2\pi fc}}{R + \frac{1}{j2\pi fc}}\right]$$

$$V_A = V_{in}\left[\frac{1}{1 + j2\pi fRC}\right]$$

Substituting in (2),

$$V_{o2} = 2V_{in}\left[\frac{1}{1 + j2\pi fRC}\right]$$

Hence, the total output voltage is

$$V_o = V_{o1} + V_{o2}$$

$$= -V_{in} + 2V_{in}\left(\frac{1}{1 + j2\pi fRC}\right)$$

$$V_o = V_{in}\left[-1 + \frac{2}{1+j2\pi fRC}\right]$$

$$\frac{V_o}{V_{in}} = \frac{1-j2\pi fRC}{1+j2\pi fRC}$$

The magnitude of the transfer function is

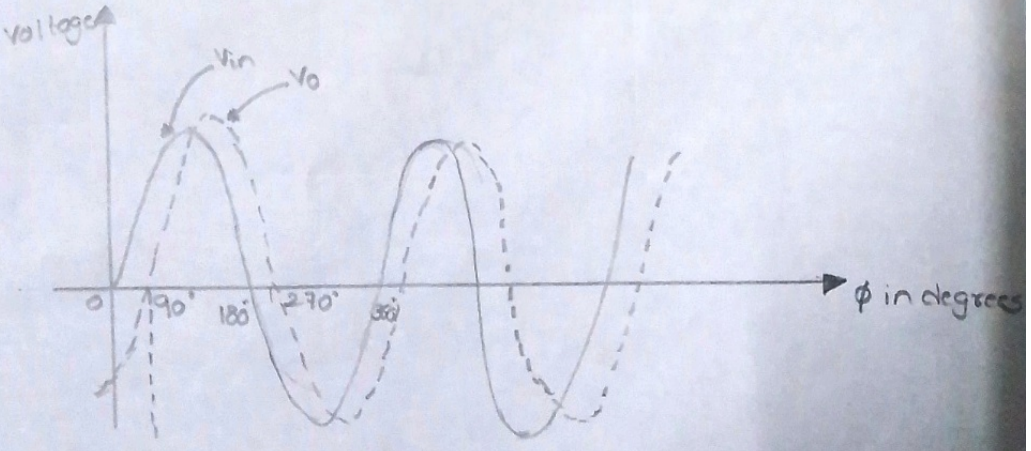
$$\left|\frac{V_o}{V_{in}}\right| = \frac{\sqrt{1+(2\pi fRC)^2}}{\sqrt{1+(2\pi fRC)^2}} = 1$$

It is mentioned earlier that the magnitude is always 1 for all pass filter and it can pass the entire range of frequency. But the phase angle is given by

$$\boxed{\phi = -2\tan^{-1}\left(\frac{2\pi fRC}{1}\right)}$$

This is the phase angle in degrees which indicates that there is a phase shift of ϕ degrees between input and output signal. If the positions of R and C are interchanged, we get the positive phase shift. The negative phase shift indicates that the output V_o lags input V_{in} by angle ϕ, while positive phase shift indicates that V_o leads input V_{in} by angle ϕ

The fig 6.38 shows the phase shift produced by all pass filter between input and output.



Example 6.10: For the all pass filters, the values of R and C are 7.95 kΩ and 0.02μF respectively. If the input frequency is 1.5 kHz, calculate the phase shift.

$R = 7.95\ k\Omega \qquad C = 0.02\mu F$

$f = 1.5\ kHz$

$$\phi = 0^\circ - 2\tan^{-1}\left(\frac{2\pi fRC}{1}\right)$$

$$= -2\tan^{-1}\left(\frac{2\pi \times 1.5\times10^{3}\times 7.95\times10^{3}\times0.02\times10^{-6}}{1}\right)$$

$$= -112.56^\circ$$

The output voltage lags input voltage by 112.56°, but the amplitude and frequency of output will be same as that of input.

Unit-3

DATA * CONVERTER's

Digital to Analog Converters:- (DAC)

*

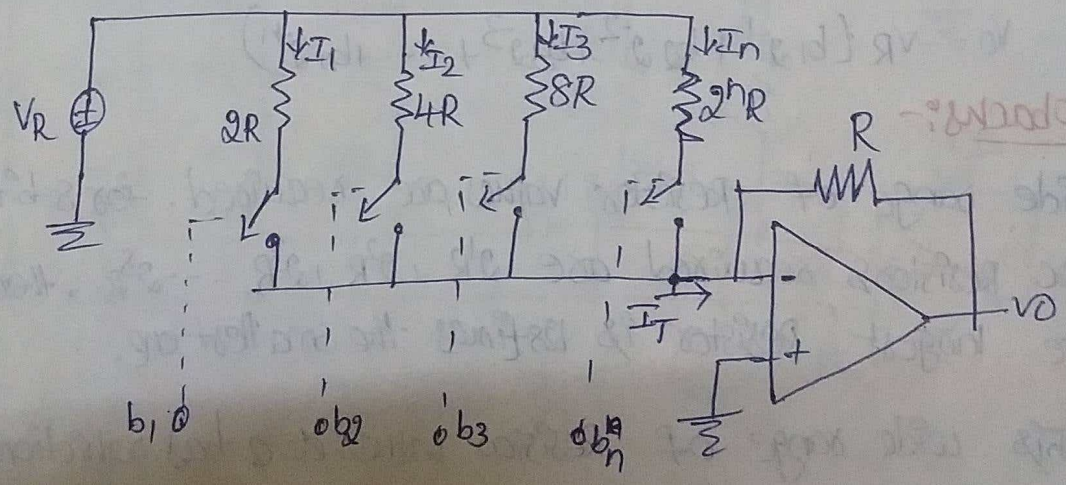
There are mainly two techniques used for analog output from an digital input.

→ Binary weighted Resistor D/A converter

→ R/2R ladder D/A converter

In these techniques, the shunt resistors are used to generate 'n' binary weighted currents. these currents are added according to switch positions controlled by the digital input and then converted into voltage to give analog voltage equivalent of digital input. so such converters are called current driven DAC's.

Binary weighted Resistor D/A converter:-



The binary weighted Resistor DAC uses op-amp to sum of binary weighted currents derived from a reference voltage 'VR'. current scaling resistors 2R, 4R, 8R ---- 2ⁿR. the switch positions are controlled by the digital inputs.

→ when digital input is logic 1, it connects the switching Resistance to the reference voltage V_R, otherwise it leaves Resistor open therefore.

- for on-switch, $I = \frac{V_R}{R}$
- for off-switch (ZERO) $I = 0$

these operational amplifier is used as summing amplifier. Due to high input impedance of opamp, summing current will flow through Rf. hence the total current through Rf can be given as

$$I_T = I_1 + I_2 + I_3 + \cdots + I_n.$$

the output voltage is the voltage across Rf and it is given as

$$V_0 = -I_T R_f = -R_f (I_1 + I_2 + I_3 + \cdots + I_n)$$

$$= -R_f \left(b_1 \frac{V_R}{2R} + b_2 \frac{V_R}{4R} + b_3 \frac{V_R}{8R} + \cdots + b_n \frac{V_R}{2^n R} \right)$$

$$= \frac{-V_R}{R} R_f \left(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_n 2^{-n} \right)$$

when $R_f = R$, V_0 given as

$$V_0 = -V_R \left(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_n 2^{-n} \right)$$

Drawbacks:-

1. wide range of Resistor values are required. for 8-bit DAC Resistors required are $2^1R, 2^2R, 2^3R \cdots 2^8R$. therefore the largest Resistor is 128 times the smallest one.

2. this wide range of Resistor values also has restrictions on both higher, lower ends. it is impracticable to fabricate large values of Resistor in IC. the voltage drop across a large Resistor due to the bias current also affects the accuracy.

3. The finite Resistance of the switches disturbs the binary-weighted relationship among the various currents, particularly in the most significant bit positions where the current setting Resistances are smaller.

2) Inverted R-2R ladder (current mode R-2R ladder DAC :-

R-2R ladder DAC uses only two resistor values. This avoids Resistances spread drawback of binary weighted DAC like binary weighted Resistor DAC, it also uses shunt Resistors to generate 'n' binary weighted currents ; however it uses voltage scaling & Identical Resistors instead of Resistor scaling & common voltage reference used in binary weighted Resistor DAC. voltage scaling requires an additional set of voltage dropping series Resistances b/w adjacent nodes.

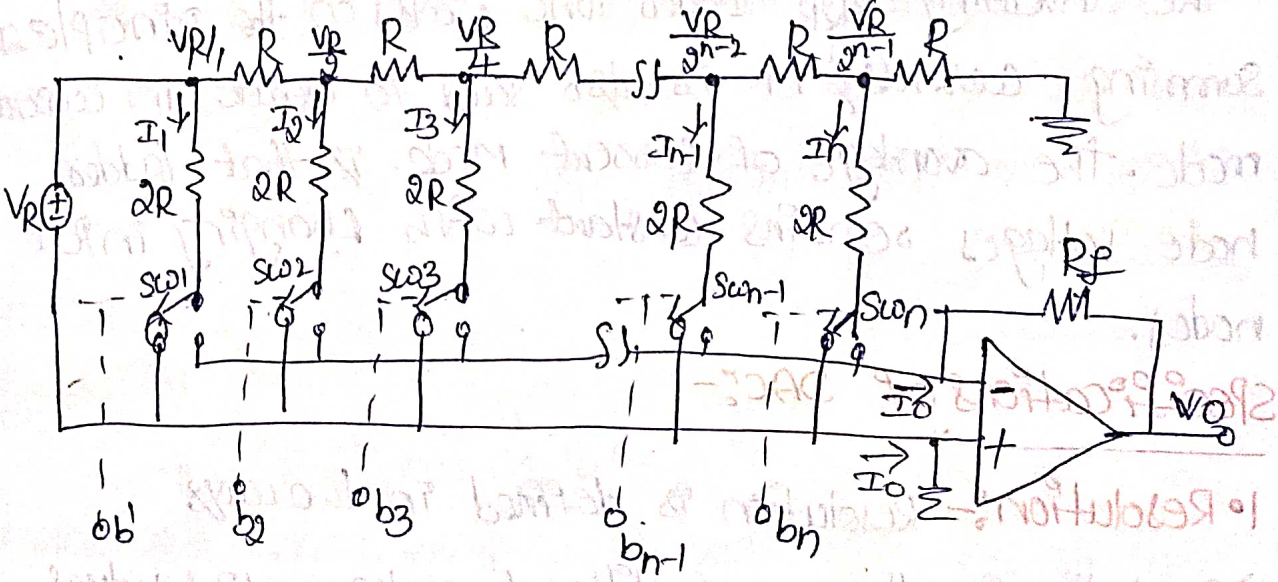


fig :- Inverted R-2R ladder DAC.

Here each bit of the binary word controls the corresponding switch either to ground (or) to inverting input terminal of the opamp which is at virtual ground. since both the positions of switches are at ground Potential,

the current flowing through resistances is constant & it is independent of switch position. these currents can be given as

$$I_1 = \frac{V_R}{2R}$$

$$I_2 = \frac{V_R/2}{2R} = \frac{V_R}{4R}$$

$$I_3 = \frac{V_R/4}{2R} = \frac{V_R}{8R}$$

$$I_n = \frac{V_R/2^{n-1}}{2R} = \frac{I_1}{2^{n-1}}$$

$$V_0 = -I_T R_f$$

$$= -R_f (I_1 + I_2 + I_3 + \cdots + I_n)$$

$$= -R_f \left(b_1 \frac{V_R}{2R} + b_2 \frac{V_R}{4R} + b_3 \frac{V_R}{8R} + \cdots + b_n \frac{V_R}{2^n R} \right)$$

$$= -\frac{V_R}{R} R_f \left(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_n 2^{-n} \right)$$

when $R_f = R$, $V_0 = -V_R (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_n 2^{-n})$

the Inverting R/2R ladder DAC works on the principle of summing currents & it is also said to operate in current mode. the advantage of current mode is that ladder node voltages remains constant with changing in bit nodes.

Specifications of DAC:-

1. **Resolution:-** Resolution is defined in two ways

→ Resolution is the no. of different analog output values that can be provided by a DAC for an n-bit DAC.

$$\text{Resolution} = 2^n$$

→ Resolution is also defined as the ratio of a change in output voltage resulting from a change

of 1LSB at the digital inputs.

$$\text{resolution} = \frac{V_{OFS}}{2^n - 1}$$

where V_{OFS} = Full-scale output voltage

2. **Accuracy**:- It is a comparision of actual output voltage with expected output. it is expressed in %.

$$\text{Accuracy} = \frac{V_{OFS}}{(2^n - 1)^2}$$

3) **monotonicity**:- A converter is said to have good monotonicity if it does not miss step backward when stepping through it's entire range by a counter.

4) **conversion time**:- It is a time required for conversion of analog signal into it's digital equivalent. It is also called as setting time. It depends on the response time of switches & the output of the amplifier.

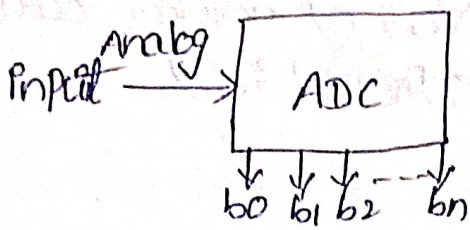
5) **Setting Time**:- this is the time required for the output of the DAC to settle to within ± ½ LSB of the final value for a given digital input i.e zero to fullscale.

6) **stability**:-

the Performance of converter changes with temperature, age & power supply variations. So all the relavant parameters such as offset, gain, linearity error & monotonicity must be specified over the full temperature & Power supply range. these parameters represent the stability of the converters.

Analog to Digital Converter:-

The A/D conversion is a quantizing process whereby an analog signal is converted into equivalent binary word.



Analog to digital converters are classified into two general groups based on the conversion techniques. one technique involves comparing a given analog signal with the internally generated reference voltages. this group includes successive approximation, flash, delta modulation, adaptive delta modulation converters. the another techniques involves changing an analog signal into time (or) frequency & comparing these new parameters against known values. this group includes integrator, voltage-to-frequency converters.

1) Dual-Slope-ADC:-

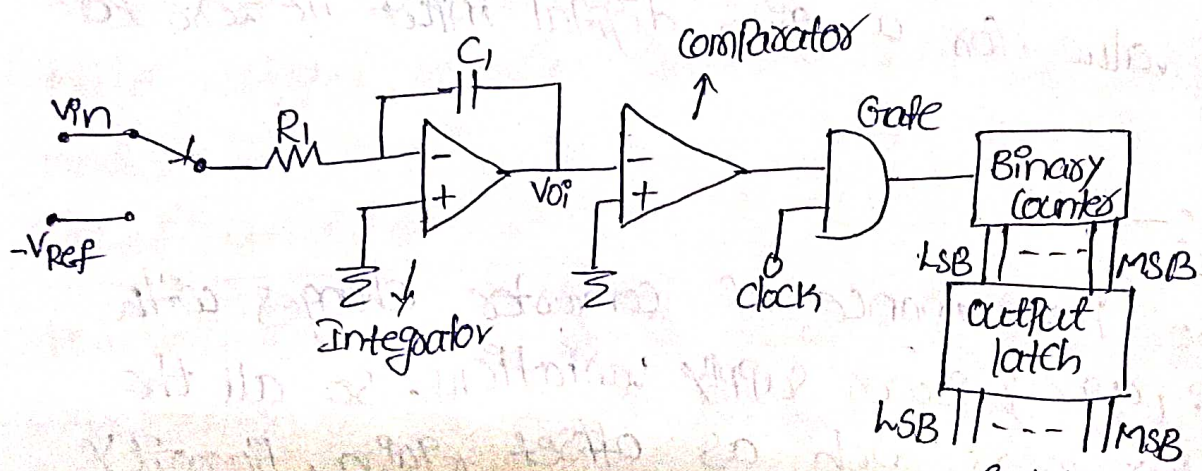
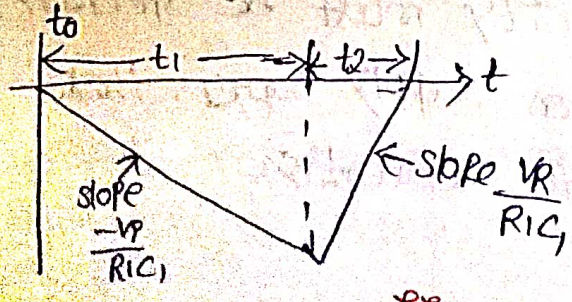


fig:- Dual slope ADC



→ Dual slope conversion is an indirect methode of A/D conversion where an analog voltage & a reference voltage are converted into time periods by an integrator & then measured by a counter. the speed of this conversion is slow but the accuracy is high.

→ the dual-slope ADC consists of an integrator (ramp generator) comparator, binary counter, output latch & reference voltage. the ramp generator input is switched b/w the analog input voltage V_i & a -ve reference voltage $-V_{ref}$. the analog switch is controlled by the MSB of the counter. when the MSB is a logic 0, the voltage being measured is connected to the ramp generator input. when MSB is logic 1, the -ve reference voltage is connected to the ramp generator.

At time t=0, analog switch 'S' is connected to the analog input voltage v_i, so that the analog input voltage integration begins the output voltage of the integrator can be given as $V_{o1} = \frac{-1}{R_1C_1}\int_0^t v_i dt$

$$V_{o1} = \frac{-V_i t}{R_1 C_1}$$

At the end of clock periods MSB of the counter goes high
→ At a result the output of the flip-flop goes high, which causes switch S to be switched from V_P to $-V_R$. At this very same time the binary counter which has gone through its entire count sequence is Reset.

The negative reference voltage connected to the input of integrator causes the integrator output to ramp positive when integrator output reaches zero, the comparator output voltage goes low, which disables the clock & and gate this stops the clock pulses reaching the counter, so that the counter will be stopped at a count corresponding to the no. of clock pulses in time t.

The integrator output ramp down to a voltage V_z & get back upto '0'. Therefore, the charge voltage is equal to discharge voltage & can be written as.

$$\frac{V_i t_1}{R_1 C_1} = \frac{V_R t_2}{R_1 C_1}$$

$$V_i t_1 = V_R t_2$$

$$t_2 = \frac{V_i t_1}{V_R}$$

→ the above equation shows that t_2 is directly proportional only to the V_i. since V_R & t_1 are constants. the binary digital o/p of the counter gives corresponding digital value.. for time period t_2 & hence it is also directly proportional to input signal V_i

→ the actual conversion of analog voltage V_{in} into a digital count occurs during t_2. the control circuit connects the clock to the counter at the beginning of t_2. the clock is disconnected at the of t_2. Thus the counter contents is digital output.

$$\text{Digital output} = \left(\frac{\text{counts}}{\text{second}}\right) t_2$$

$$= \left(\frac{\text{counts}}{\text{second}}\right)\left(\frac{V_i}{V_R}\right) t_1$$

the counter output can then be connected to an appropriate digital display.

Advantages:-

1. It is highly accurate.
2. It's cost is low.
3. It is immune to temperature variations in R_1 & C_1.

* the only disadvantage is it's speed which is low.

Parallel Comparator (or) flash type ADC:-

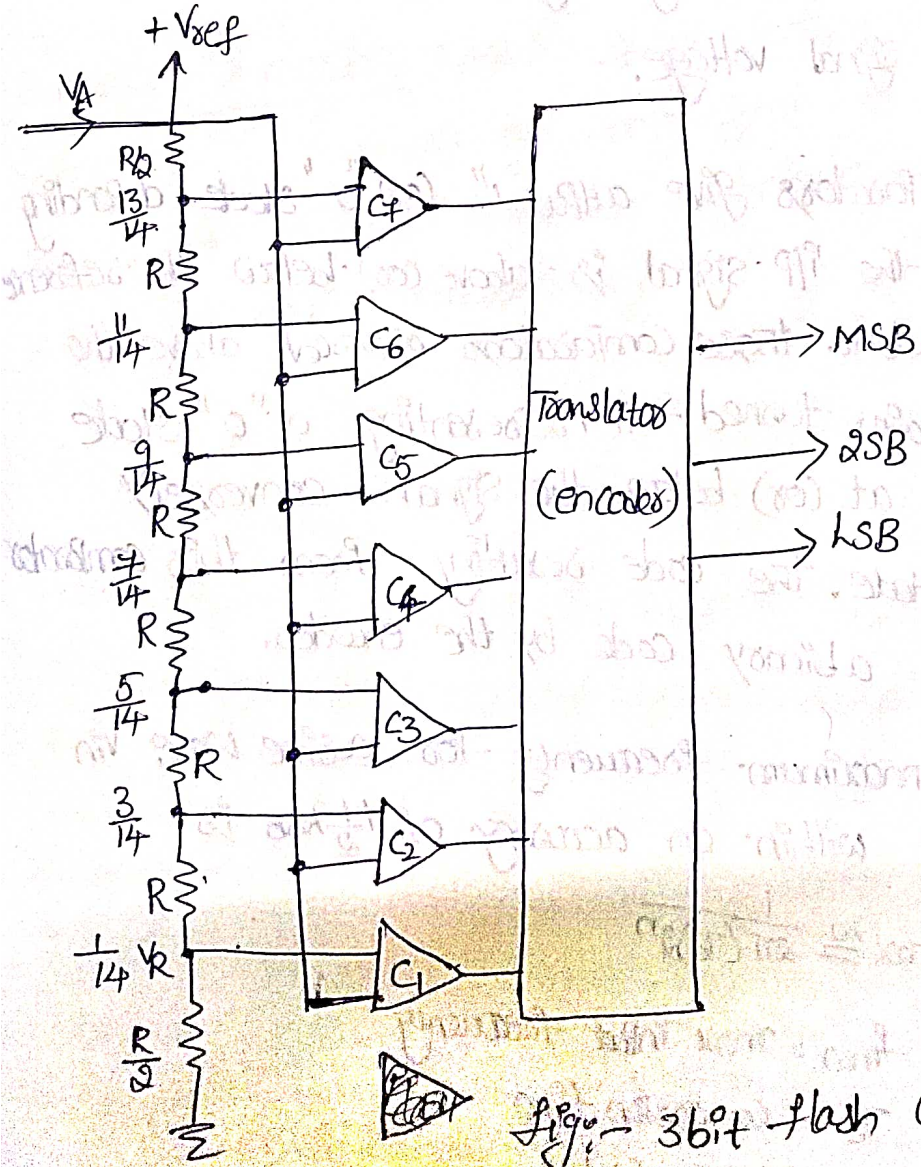


fig:- 3bit flash Converter

When system design call for the highest speed available, flash-type ADC's are the right choice. they get their names from their ability to do the conversion very rapidly. flash ADC, also known as a simultaneous (or) Parallel comparator ADC, because the fast conversion speed is accomplished by providing $2^n - 1$ comparators and simultaneously comparing the input signal with unique reference levels spaced 1LSB apart.

The figure shows 3-bit flash ADC. for this ADC, seven ($2^3 - 1$) comparators are required. one input of the each comparator is connected to the input signal & other i/p to the reference voltage level generated by the reference voltage divider. the reference voltage signal is equal to the full scale input signal voltage.

the comparators give output "1" (or) "0" state depending on whether the i/p signal is above (or) below the reference level at that instant. those comparators reffered above the input signal remains turned-off, representing a "0" state. the comparators at (or) below the signal conversely become a '1' state. the code resulting from this comparator is converted to a binary code by the encoder.

so the maximum frequency for a sine wave Vin to be digitised within an accuracy of $\pm\frac{1}{2}$ LSB is

$$f_{max} \cong \frac{1}{2\pi (T_c) 2^n}$$

where f_{max} = max input frequency

T_c = conversion time

n = no. of bits.

of functional value D, so that

$$D = d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n} \qquad (10.3)$$

where d_1 is the most significant bit and d_n is the least significant bit. An ADC usually has two additional control lines; the START input to tell the ADC when to start the conversion and the EOC (end of conversion) output to announce when the conversion is complete. Depending upon the type of application, ADCs are designed for microprocessor interfacing or to directly drive LCD or LED displays.

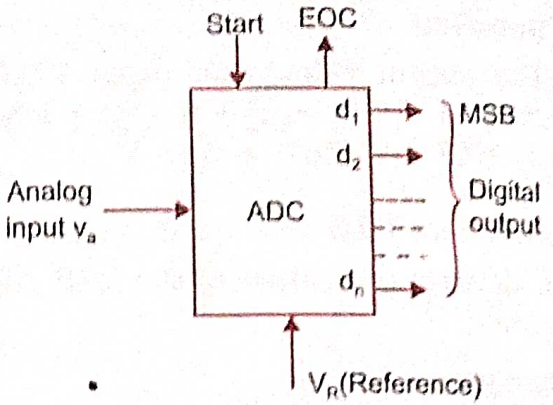


Fig. 10.9 Functional diagram of ADC

ADCs are classified broadly into two groups according to their conversion technique. Direct type ADCs and Integrating type ADCs. Direct type ADCs compare a given analog signal with the internally generated equivalent signal. This group includes

Flash (comparator) type converter
Counter type converter
Tracking or servo converter
Successive approximation type converter

Integrating type ADCs perform conversion in an indirect manner by first changing the analog input signal to a linear function of time or frequency and then to a digital code. The two most widely used integrating type converters are:

(i) Charge balancing ADC
(ii) Dual slope ADC

The most commonly used ADCs are successive approximation and the integrator type. The successive approximation ADCs are used in applications such as data loggers and instrumentation where conversion speed is important. The successive approximation and comparator type are faster but generally less accurate than integrating type converters. The flash (comparator) type is expensive for high degree of accuracy. The integrating type converter is used in applications such as digital meter, panel meter and monitoring systems where the conversion accuracy is critical.

DIRECT TYPE ADCs

10.3.1 The Parallel Comparator (Flash) A/D Converter

This is the simplest possible A/D converter. It is at the same time, the fastest and most expensive technique. Figure 10.10 (a) shows a 3-bit A/D converter. The circuit consists of a resistive divider network, 8 op-amp comparators and a 8-line to 3-line encoder (3-bit priority encoder). The comparator and its truth table is shown in Fig. 10.10 (b). A small amount of hysteresis is built into the comparator to resolve any problems that might occur if both inputs were of equal voltage as shown in the truth table. Coming back to Fig. 10.10 (a), at each node of the resistive divider, a comparison voltage is available. Since all the resistors are of equal value, the voltage levels available at the nodes are equally divided between the reference voltage V_R and the ground. The purpose of the circuit is to compare the analog input voltage V_a with each of the node voltages. The truth table for the flash type AD converter is shown in Fig. 10.10 (c). The circuit has the advantage of high speed as the

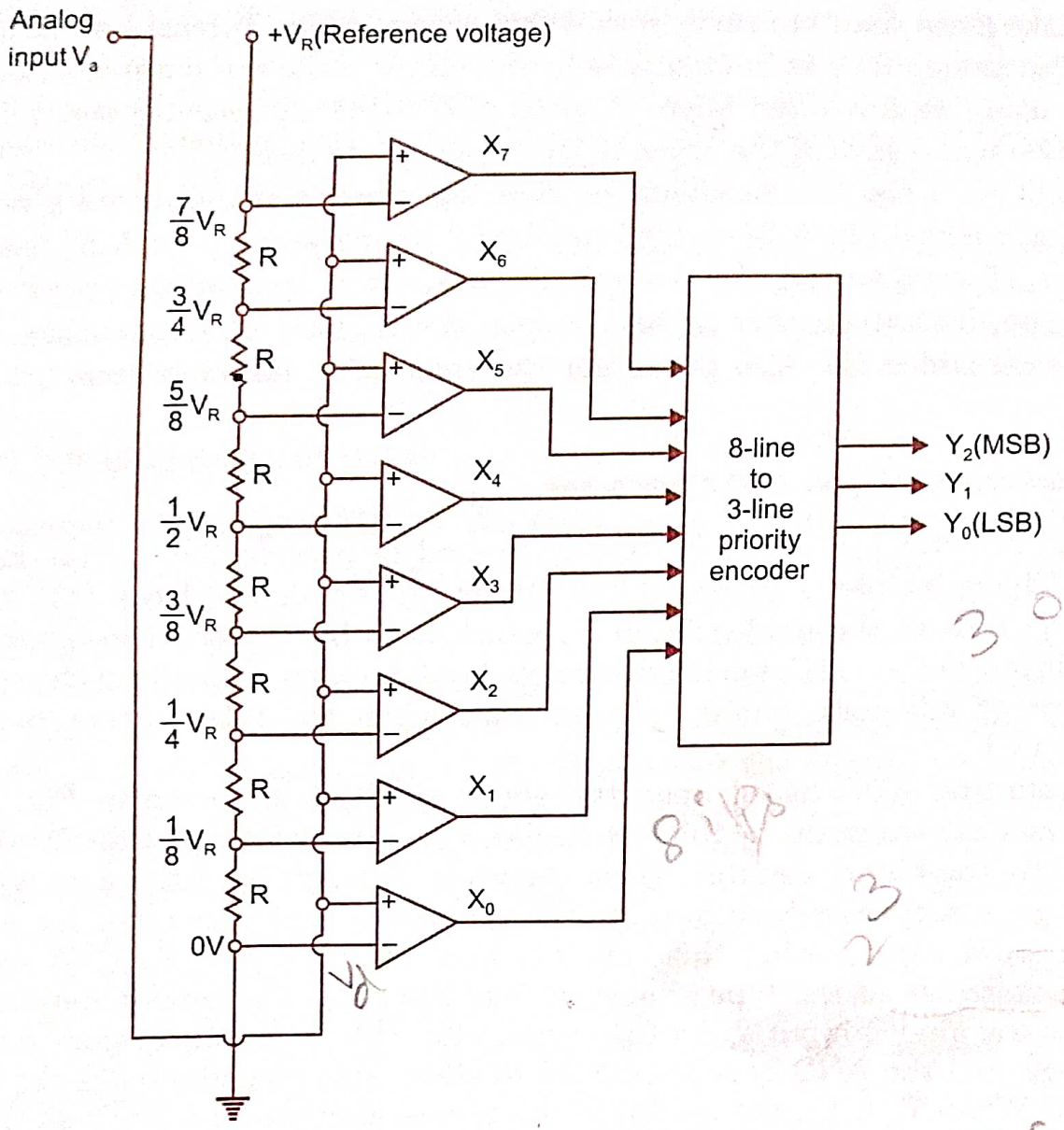


Fig. 10.10 (a) Basic circuit of a flash type A/D converter

Voltage input	*Logic output X*
$V_a > V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	Previous value

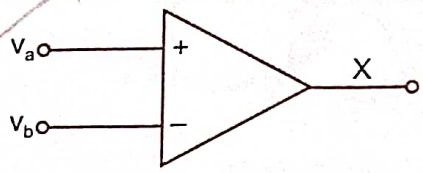


Fig. 10.10 (b) Comparator and its truth table

Input voltage V_a	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4$ to 3 $V_R/8$	0	0	0	0	0	1	1	1	0	1	0
3 $V_R/8$ to $V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2$ to 5 $V_R/8$	0	0	0	1	1	1	1	1	1	0	0
5 $V_R/8$ to 3 $V_R/4$	0	0	1	1	1	1	1	1	1	0	1
3 $V_R/4$ to 7 $V_R/8$	0	1	1	1	1	1	1	1	1	1	0
7 $V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

Fig. 10.10 (c) Truth table for a flash type A/D converter

conversion take place simultaneously rather than sequentially. Typical conversion time is 100 ns or less. Conversion time is limited only by the speed of the comparator and of the priority encoder. By using an Advanced Micro Devices AMD 686A comparator and a T1147 priority encoder, conversion delays of the order of 20 ns can be obtained.

This type of ADC has the disadvantage that the number of comparators required almost doubles for each added bit. A 2-bit ADC requires 3 comparators, 3-bit ADC needs 7, whereas 4-bit requires 15 comparators. In general, the number of comparators required are $2^n - 1$ where n is the desired number of bits. Hence the number of comparators approximately doubles for each added bit. Also the larger the value of n, the more complex is the priority encoder.

10.3.2 The Counter Type A/D Converter

The D to A converter can easily be turned around

owly, the tracking A/D will be within one LSB of the change and
nalog input changes rapidly, the tracking A/D cannot keep up with the
curs as shown in Fig. 10.12 (b).

The tracking ADC has the advantage of being simple. The disadvantage, however, is the
me needed to stabilize as a new conversion value is directly proportional to the rate at
hich the analog signal changes.

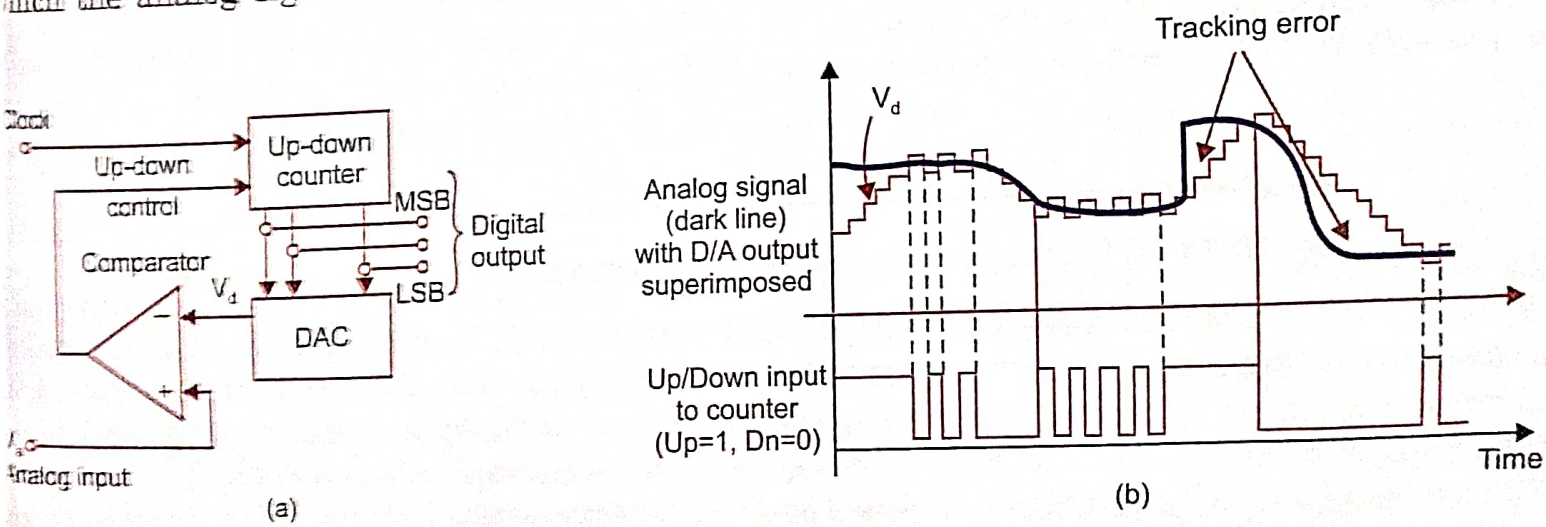


Fig. 10.12 (a) A tracking A/D converter (b) Waveforms associated with a tracking A/D converter

10.3.4 Successive Approximation Converter

The successive approximation technique uses a very efficient code search strategy to complete
n-bit conversion in just n-clock periods. An eight bit converter would require eight clock pulses
o obtain a digital output. Figure 10.13 shows an eight bit converter. The circuit uses a

successive approximation register (SAR) to find the required value of each bit by trial and error. The circuit operates as follows. With the arrival of the START command, the SAR sets the MSB $d_1 = 1$ with all other bits to zero so that the trial code is 10000000. The output V_d of the DAC is now compared with analog input V_a. If V_a is greater than the DAC output V_d then 10000000 is less than the correct digital representation. The MSB is left at '1' and the next lower significant bit is made '1' and further tested.

However, if V_a is less than the DAC output, then 10000000 is greater than the correct digital representation. So reset MSB to '0' and go on to the next lower significant bit. This procedure is repeated for all subsequent bits, one at a time, until all bit positions have been tested. Whenever the DAC output crosses V_a, the comparator changes state and this can be taken as the end of conversion (EOC) command. Figure 10.14 (a) shows a typical conversion sequence and Fig. 10.14 (b)

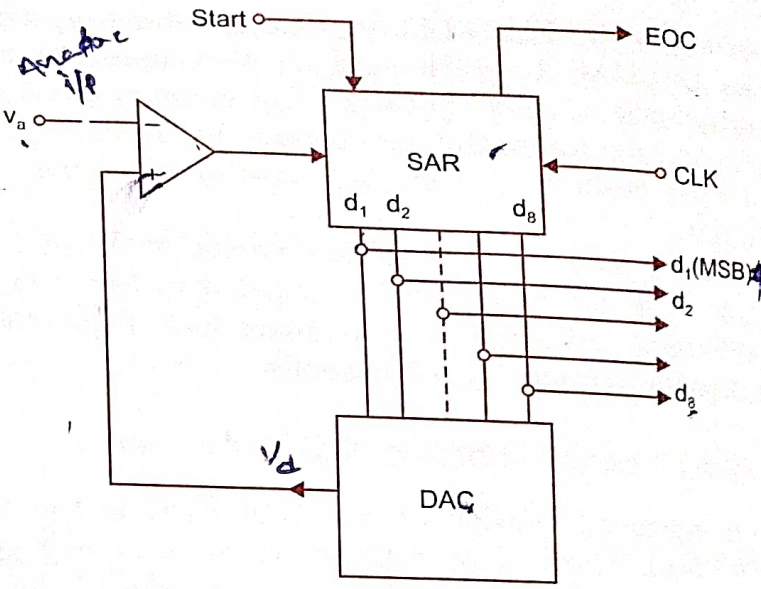


Fig. 10.13 Functional diagram of the successive approximation ADC

Correct digital representation	*Successive approximation register output V_d at different stages in conversion*	*Comparator output*
11010100	10000000	1 (initial output)
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

Fig. 10.14 (a) Successive approximation conversion sequence for a typical analog input

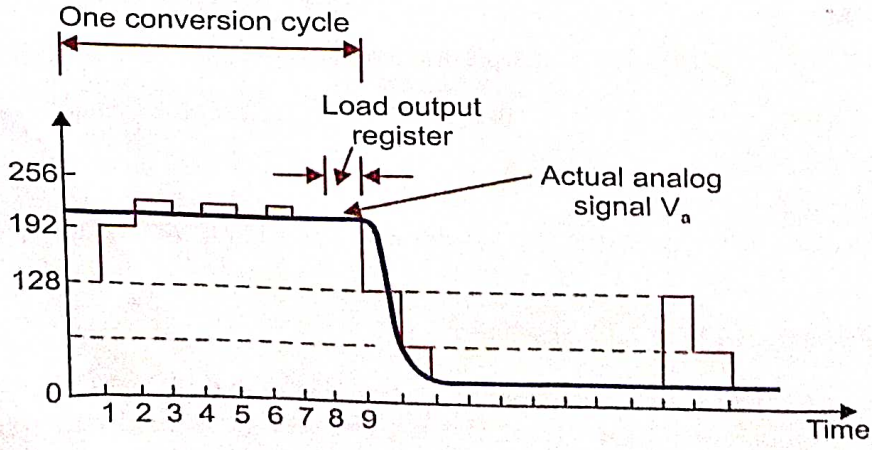


Fig. 10.14 (b) The D/A output voltage is seen to become successively closer to the actual analog input voltage

shows the associated wave forms. It can be seen that the D/A output voltage becomes successively closer to the actual analog input voltage. It requires eight pulses to establish the accurate output regardless of the value of the analog input. However, one additional clock pulse is used to load the output register and reinitialize the circuit.

A comparison of the speed of an eight bit tracking ADC and an eight bit successive approximation ADC is made in Fig. 10.15. Given the same clock frequency, we see that the tracking circuit is faster only for small changes in the input. In general, the successive approximation technique is more versatile and superior to all other circuits discussed so far.

Successive approximation ADCs are available as self contained ICs. The AD7592 (Analog Devices Co.) a 28-pin dual-in-line CMOS package is a 12-bit A/D converter using successive approximation technique.

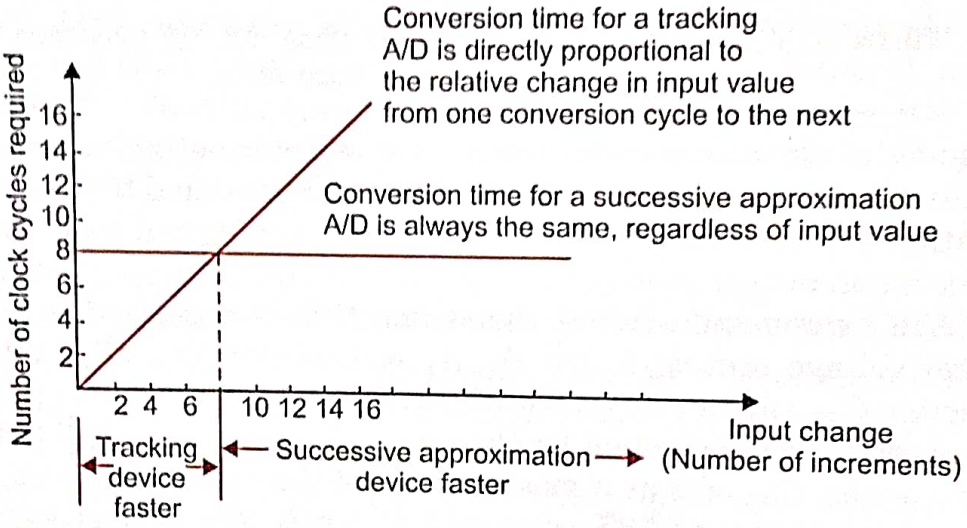


Fig. 10.15 Comparison of conversion times for tracking and successive approximation A/D devices

Integrating Type of ADCs

The integrating type of ADCs do not require a S/H circuit at the input. If the

Specifications of ADC:-

1. **Resolution:-**

Resolution is the no. of different digital output values that can be produced by an ADC.

$$\text{resolution} = 2^n$$

It is defined as the ratio of change in value of input voltage, V_i needed to change the digital output by 1 LSB.

$$\text{Resolution} = \frac{V_{FS}}{2^n - 1}$$

2. **Quantization Error:-** the uncertainity in producing an exact value is known as quantization error.

$$Q_E = \frac{V_{FS}}{(2^n - 1)2}$$

3. **Analog conversion TIME:-** It is defined as the total time required to convert an analog signal into it's digital output. It depends on the conversion technique used, the propagation delay of circuit components. //

Complex programmable logic devices :-

→ PLA's and PAL's are useful for implementing a wide variety of small digital circuits. This chips are limited to fairly medium sizes, typically it supporting a combined number of inputs and outputs is not more than 32.

→ for Implementation of complex circuits which requires more inputs and outputs, either multiple PLA's (or) PAL's can be combined together to implement the complex design. A more sphisticated type of chip is formed is called "CPLD".

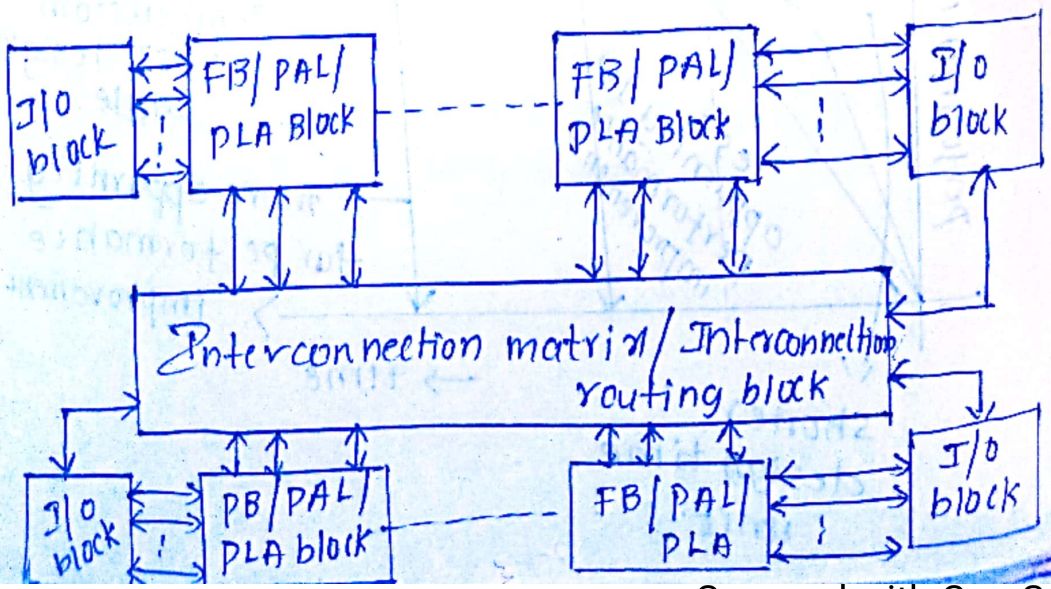
→ A CPLD having three blocks,

(1). PAL / PLA / functional Block

(2). I/O block.

(3). Interconnection matrix / Interconnection Routing.

Architecture of CPLD :-



→ Each functional block is similar to PAL (or) PLA, if internal wiring structure to connect circuit blocks as shown in fig above. So, a CPLD has two levels of programmability.

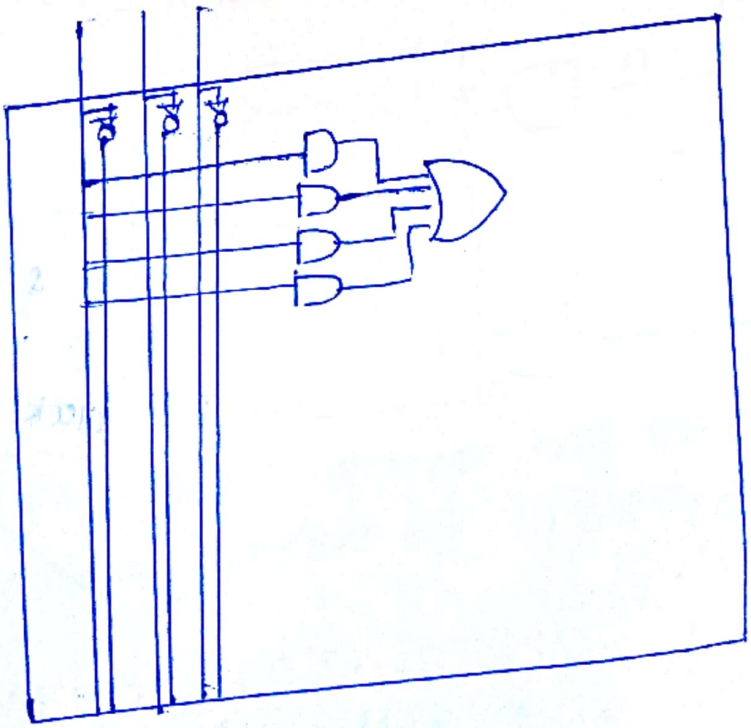
(i). Each functional block i.e., PLA (or) PAL is programmable.

(ii). The Interconnection b/w the PLD's is programmable.

→ The CPLD structure consists of PAL like functional block that are connected to a Interconnection matrix and also connected to a I/O block.

Functional Block and I/O block :-

The wiring structure and connections of a PAL in a CPLD is shown in figure below.



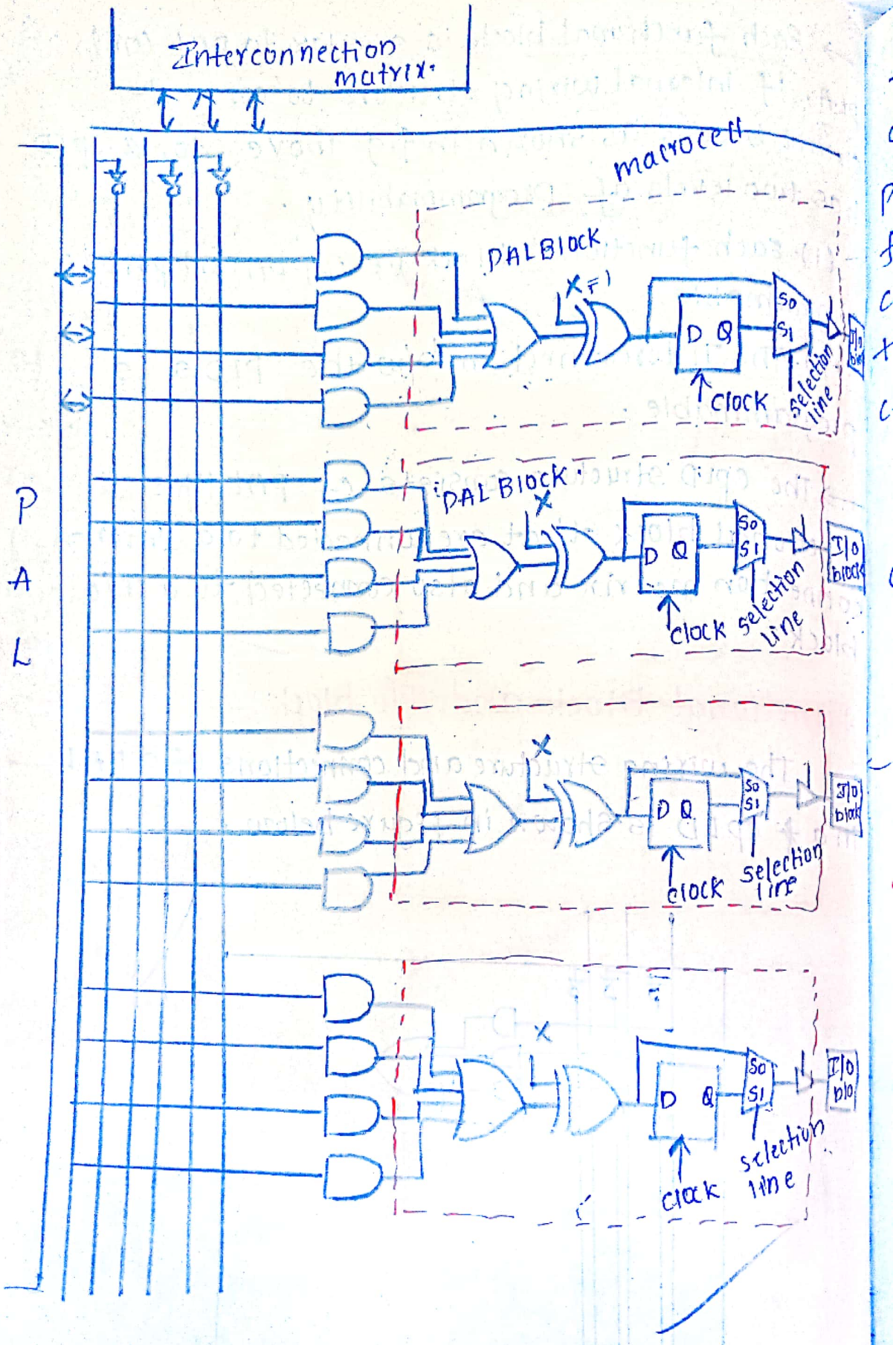


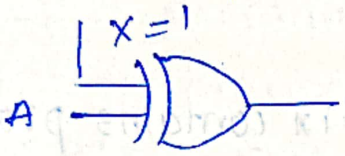
fig: A selection of CPLD.

→ The PAL Block includes three macrocells (the CPLD's having typically 4 to 20 macrocells in a PAL block). Each macrocell consisting of a four input OR Gate and the OR Gate output is connected to Exclusive OR Gate. And antoher i/p to the exclusive OR Gate can be programmably connected to one (or) zero.

case(1) :-

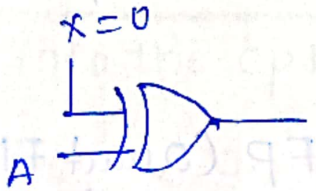
If X = 1, the XOR Gate complements the OR Gate output

Let us assume o/p of OR Gate is 'A',



$$y = A x' + A' x$$
$$= A\,1 + A'\,1$$
$$= A(0) + A'(1)$$
$$= A'$$

case 2 :-



$$y = A x' + A' x$$
$$= A \cdot 0 + A' \cdot 0$$
$$= A \cdot 1 + A' \cdot 0$$
$$= A + 0$$
$$= A$$

If X=0; then XOR gate has no effect on the output. Assum o/p of OR gate is A.

→ The macro cell also includes a flipflop, multiplexer and a tristate buffer. The flipflop is used to store the o/p value produced by XOR Gate.

→ multiplexer is used to retrive the data from present state and past state.

Tri state buffer:-

→ each tristate buffer allows each pin as an o/p from cpLD or as an i/p.

→ To use a pin as an o/p, the corresponding tri state buffer is enabled, acting as a switch it will establish, o/p path.

→ If the pin is used to be a Input, the tristate buffer is disabled, acting as a switch, it will establish i/p path.

Interconnection Matrix:-

→ The Interconnection matrix contains programmable switches that are used to connect PAL blocks. ***

→ The cPLD size range from two PAL blocks to 100 PAL blocks.

→ cPLD's are avilable in QFP (Quad Flat packaging).

Programming Technique used in cPLD:-

cPLD devices, usually support ISP (In system programming) technique.

Isp:-

The method of programming, while the chip is mounted on the circuit board with

other components is called "ISP".

Most Isp devices using SRAM, EEPROM (electrically erasable programmable Read only memory) or flash technology.

→ The PLA's and PAL's does not have Isp, but it is used only for high logic capacity devices like CPLD's.

→ A small connecter is included on the printed circuit board (pcb) of CPLD, and a caple is connected between the connector and a computer system.

→ A CPLD is programmed by transferring the program, information genelated by computer aided design tools (CAD), system through the cable (JTAG)

– Joint Text Action Group : from computer into the CPLD.

Examples of CPLD's families :-

Manufactures	CPLD product
1. ATMEL	1. ATF and ATV
2. ALTERA	2. MAX 5000, 7000 and 9000 Series.
3. cypriis	3. FLASH 370, 37000 Series.

Advantages :-

(1). Area is less. Because the functional blocks and Inter connection matrix arrangement in CPLD makes more efficient use of avilable Silicon Die area.

(2). High performance, when compared to simple programmable logic devices.

(3). CPLD uses Isp technique.

(4). Simple design, when compared to FPGA.

(5). Reduced cost.

(6). Turn around time is short compare to full custom design style.

Time taken from start to end position for an IC

(7). high density when compared to SPLD.

In small area implementing large no. of transistors.

(8). Security is more when compared to SPLD.

Disadvantages :-

(1). logic capacity of CPLD is low, compared to FPGA i.e., It can implement functions with less number of variables.

(2). flexibility is less compared to advanced programmable logic devices like FPGA.

(3). High static power dissipation, CPLD is battery operated equipment.

Applications :-

(1). for realizing large logic design.

(2). for designing data processing devices.

**** Imp.

FPGA (Field Programmable Gate Array) :-

field :- field means the processing to obtain a desired circuit will be done in lab (or) home etc.,.

Gatearray :- Gate array is used to indicate series of columns and rows of CLB (Configurable logic blocks) that can be programmed by end user. (or) customer.

→ The FPGA is an integrated circuit that contains many Identical logic cells called "configuration logic blocks".

→ The individual logic cells are interconnected by a matrix of wires and programmable switches.

→ A FPGA is a programmable logic device i.e., used to implement complex logic ckts.

→ FPGA's are different from CPLD, because FPGA's do not contain 'AND' and 'OR' gates are planes. Instead they have logic blocks for implementation of required function.

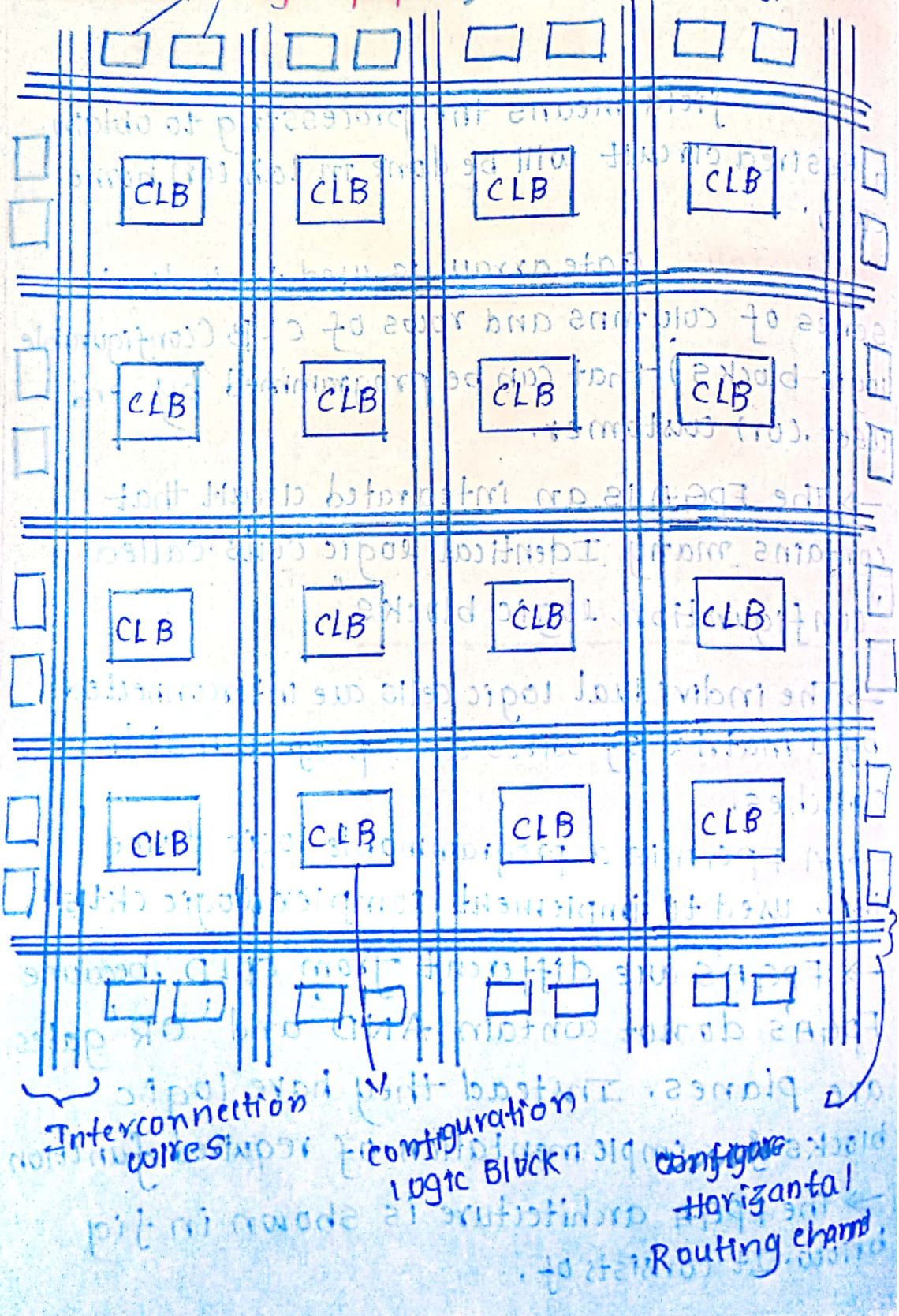
→ The FPGA architecture is shown in fig below. It consists of,

(1). configuration logic blocks.

(2). configurable I/O blocks for connecting to the pins of the package.

(3). programmable Interconnect wires and switches.

Architecture of FPGA :-



FPGA consists of an array of uncommitted circuit elements is called "configuration logic blocks" and "interconnect resources", but FPGA is configuration in general is performed to programming by end user.

→ It is the only time of field programmable logic devices that supports very high logic capacity.

→ The logic blocks are arranged in two dimensional array, the Interconnection wires are Organized as horizantal and vertical routing channels b/n rows & columns of logic blocks.

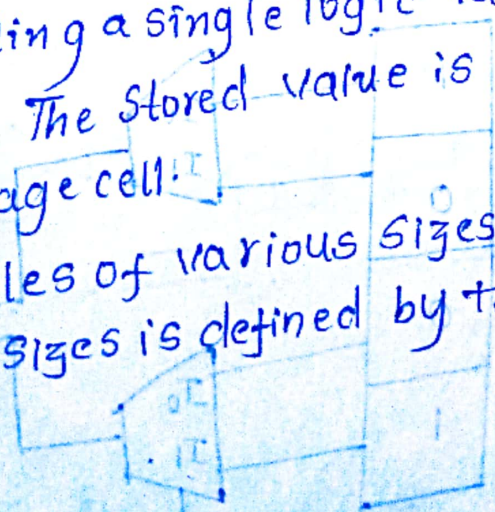
→ The routing channel contains wires and programmable Switches that allows the logic blocks to be Interconnected in many ways.

→ Each logic block in FPGA has a multiple number of inputs and one output.

→ The most commonly used logic block is a look up table (LUT) which contains storage cells that are used to implement a small logic function.

→ Each cell in a look up table logic block is capable of holding a single logic value, either 0 (or) 1. The stored value is produced as o/p of storage cell.

→ look up tables of various sizes may be created where sizes is defined by the no. of i/p's.



Look up table in CLB :- RAM-temporary.

→ A look up table basic logic block is a Segment of RAM, any function can be implemented by loading its LUT into the logic block at power up (ON)

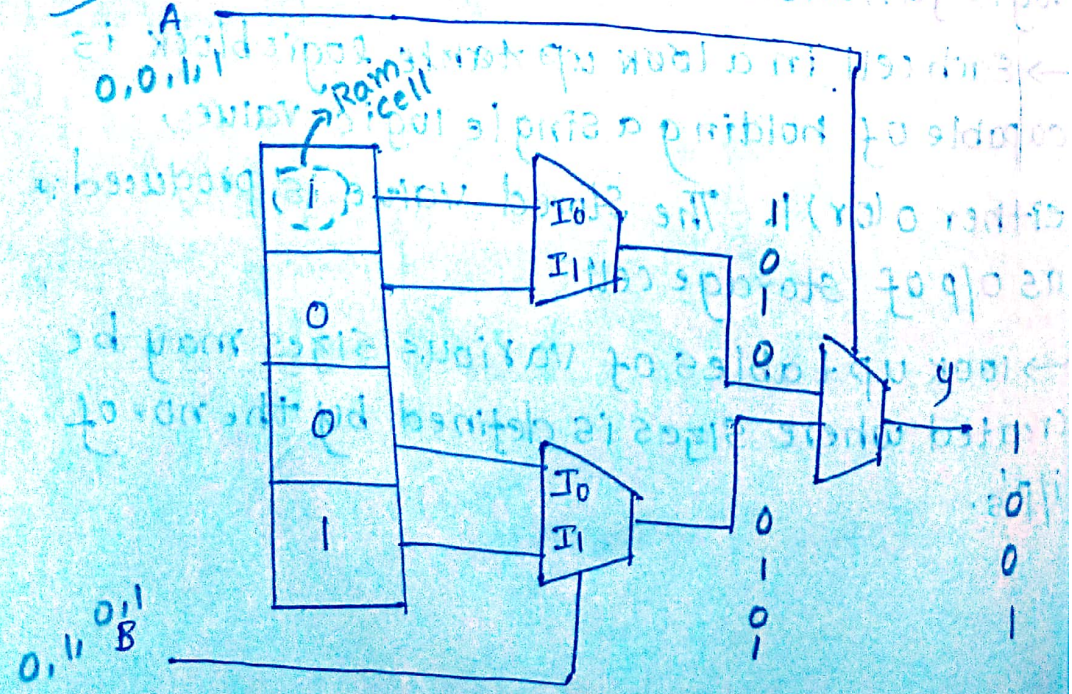
for ex :- 2^m

The function (f) = $\bar{A}\bar{B} + AB$ (XNOR function) is implemented and by loading the truth table into logic block as shown in below figure.

Truth table :-

A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

Circuit for two i/p look up table :-



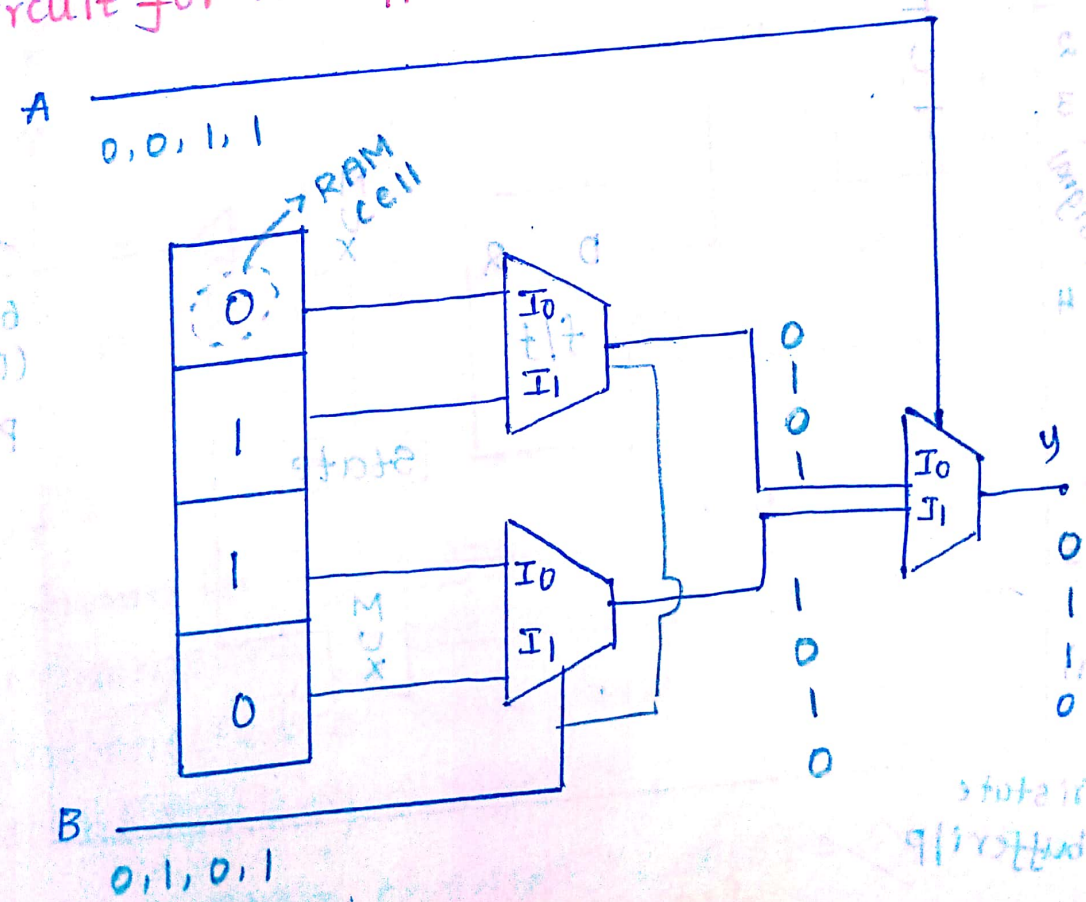
for Ex:- for (Exclusive OR Gate)

The function (f) = $A'B + AB'$ (X OR function). is implemented and by loading the truth able into logic block as shown in below igure.

Truth table :-

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

Circuit for two i/p look up table :-



Configuration logic Block:-

→ The configuration logic block has a total of 7 pins i.e., 0 to 6 as shown in below figure.

→ The no. of i/p pins is four.

→ The no. of o/p pins is one.

→ The no. of clock signals is one

→ The tristate buffer i/p is one

∴ The total no. of pins is 7

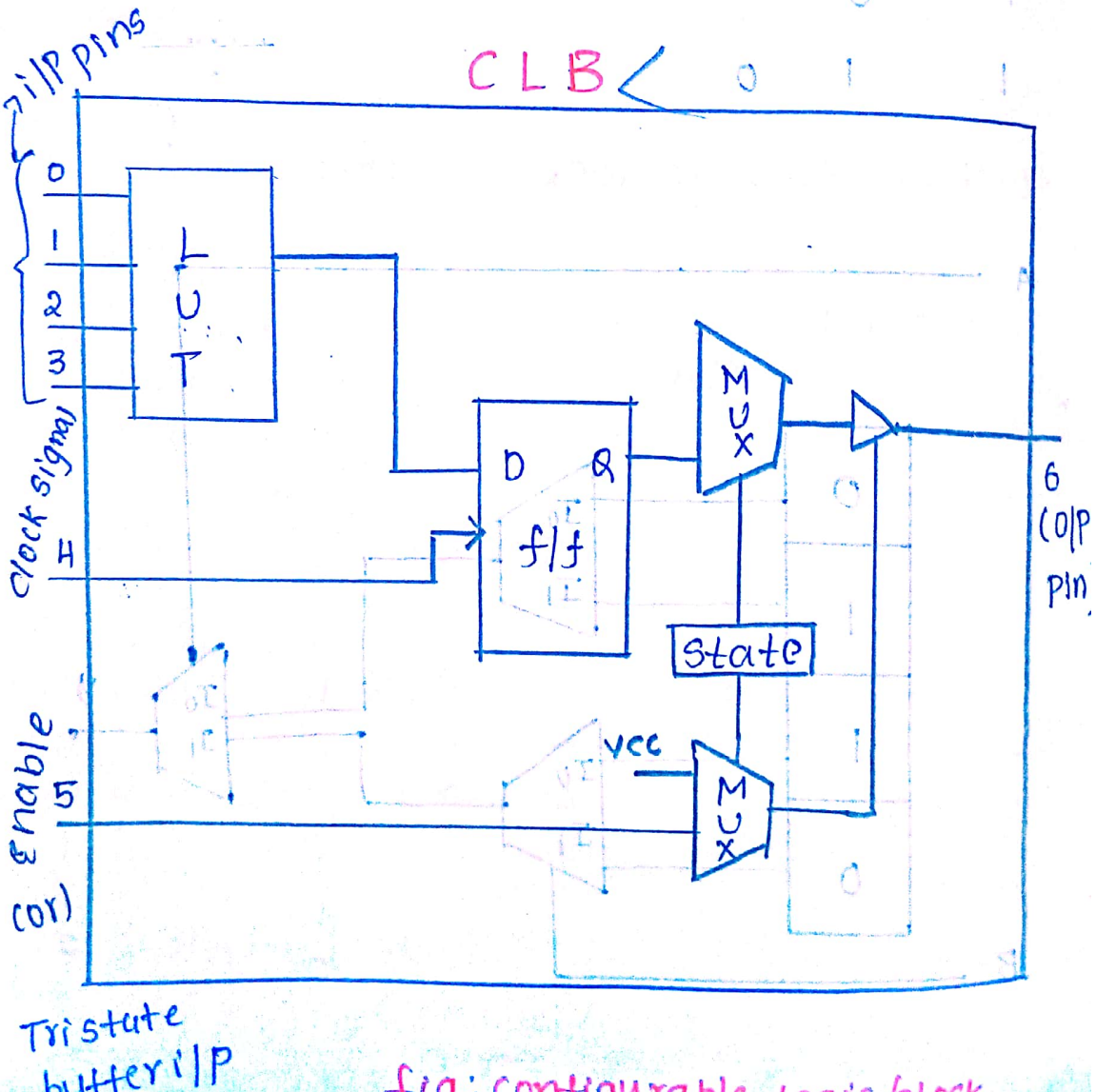


fig: configurable logic block

→ on receiving certain set of i/p's, the logic block simply "look up", the appropriate output and set the o/p line accordingly.

→ The three i/p look up has '8' storage cells, because a three variable truth table has '8' rows, the commercial FPGA chips, the LUT usually have either four (or) five i/p's, which require 16 (or) 32 storage cells.

→ FPGA's are configured by using ISP (In system programming) method, the storage cells in look up tables in FPGA are volatile, which means that they loose their temporary. stored element, whenever the power supply for the chip is turned off. so, a chip of PROM is inculded in circuit boaud of FPGA.

Routing for symmetrical FPGA's (or) Interconnections Wires and Switches in FPGA:

The basic structure of a symmetrical FPGA is shown in fig below. It consists of two dimensional array of logic block interconnected by both horizantal and vertical routing channel.

→ The routing channel consists of two kinds of blocks.

(i). connection block (c)

(2). switch block (s)

→ The connection block (C), holds routing switches i.e., used to connect the Logic block pins to the Wire Segment.

→ The Switch block Switches that allows one Wire Segment to be connected to an other wire Segment.

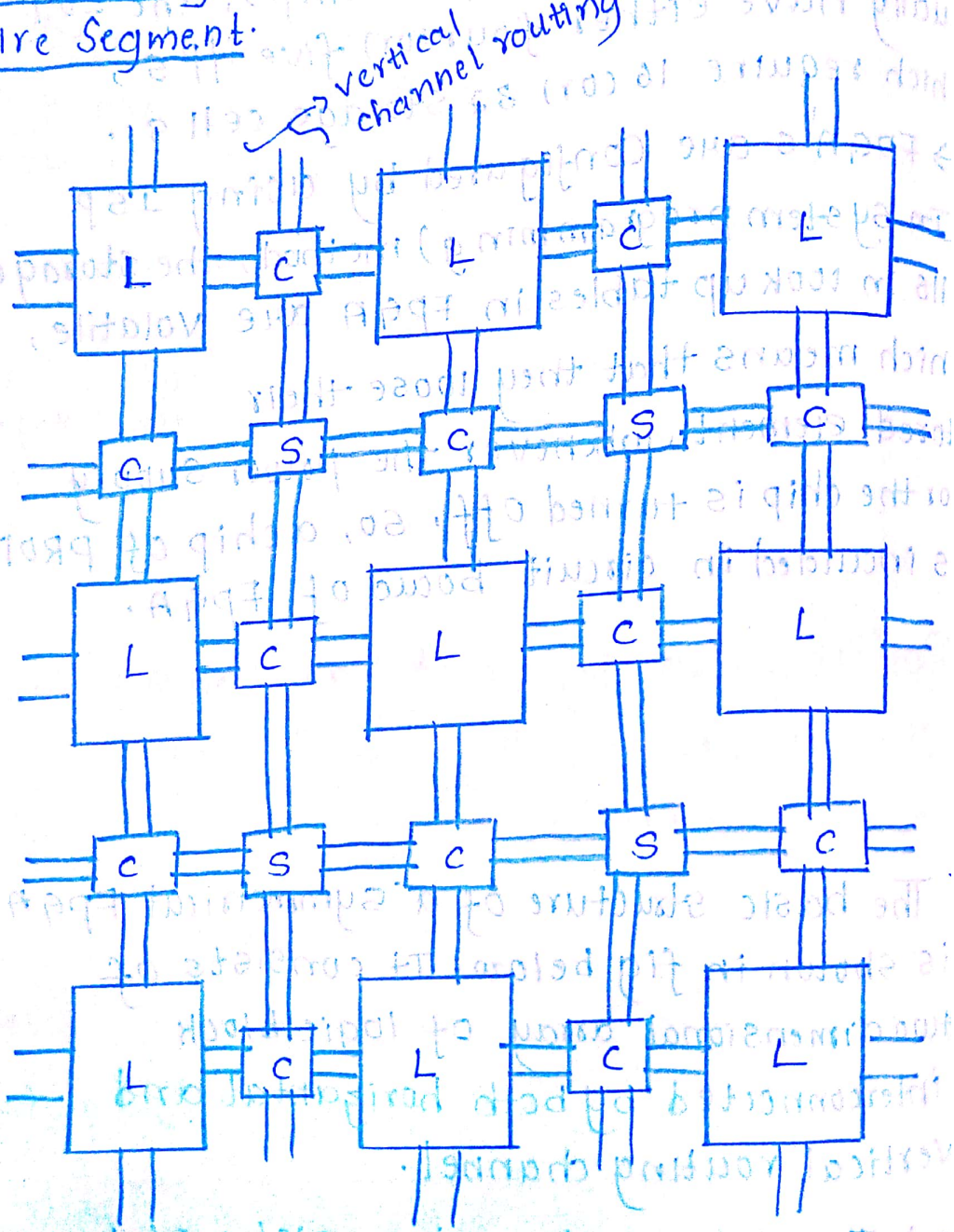


fig: structure of Symmetrical FPGA.

S → switch block

C → connection block

Advantages :-

→ very high logic capacity.
→ flexibility is more.
→ FPGA can operate on high speed
→ simple design cycle i.e., software handle routing placements and timing. so, manually assembled is less.
→ Reusability

— Reusability of FPGA is main advantage i.e., if design using FPGA was falsut, change HDL code, generate bit stream, program to FPGA and test again.
→ High density programmable logic devices.

disadvantages :-

→ power consumption in FPGA is more.
→ FPGA limits the design size.

Applications :-

→ Random logic can be implemented.
→ FPGA can be used to integrate multiple SPLD's
→ used to implement device controllers, communication encoding with SRAM.

Standard cell based design :-

(Applications, disadvantages).

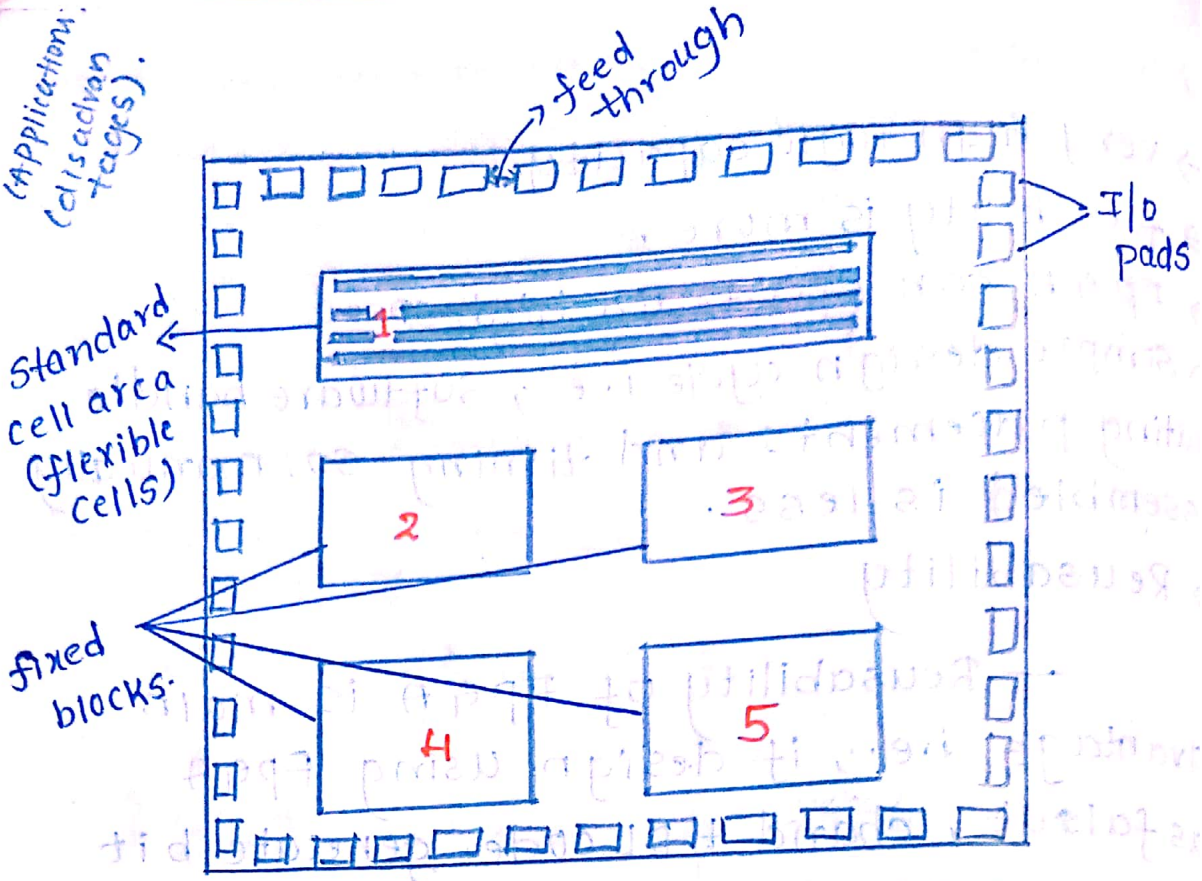


fig: Architecture standard cell based design.

→ The standard cell Architecture consists of rectangular cells of same height.

→ Initially large circuit is partitioned into several small blocks each of which is equivalent to some predefined sub-circuit is called "standard cells" and same user defined sub circuits are called "fixed blocks (or) cells".

→ The functionality and electrical characteristics of each predefined cells are tested, analyzed and collection of this cells is called "cell library".

→ usually a cell library consists of 500-1200 cells.

→ The cells are placed in a rows and spacing between each cell is called "feed through" is used for routing.

feed through :-

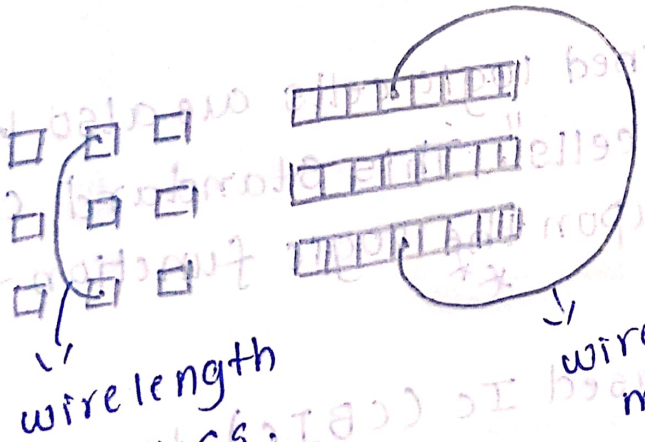
The empty space between cells is called "feed through".

→ The advantage of using feed through is, we need not go all around for routing purpose from one row to antoher.

→ Routing can be made easy in standard cells by making connections through "feed through".

→ Due to feed through, the wiring is reduced, the space between standard cells can be adjusted as per our requirements.

Note:-



→ A cell based ASIC (Application specific Integrated circuit), uses predefined logic cells. So, the design process in standard cell design stype is simpler than full custom design style.

→ The standard cell block consists of predesigned and pre-tested logic cells like AND Gates, OR Gates, Multiplexers and flipflop's etc.,

→ The standard cell area is also called "flexible cells (or) blocks". in a CBIC (cell based Ic) are built of rows of standard cells like a wall built of bricks.

→ The predesigned logic cells are similar to an existing cell library in a high level language (or) computer system language.

→ The predesigned logic cells can be used directly in the design without any modification.

→ The standard cell may be used in combination with larger predesigned cells is called "Megacells".

→ The predefined logic cells are also known as "standard cells". This standard cells size depends upon the logic function to be implemented.

→ the cell based Ic (CBIC) die (or) chip constitutes a single standard cell area, together with four other fixed blocks. The small squares around the edge of the die (or) bonding pads that are connected to the pins of ASIC package.

Advantages of CBIC:-

→ Designers save type.
→ cost is less.
→ High packing density.
→ The designer reduce the risk, by using predefined and pretested standard cell library.
→ To acheive maximum speed and minimum area.

Features of CBIC (or) standard cell based design:-

→ manufacturing lead time (or) Turn around time is above 6 to 8 weeks.
→ custom blocks can be Combined together.
→ All mask layers are customiged transistors and Interconnections.

Gate Array:-

→ Gate array is an Ic where identical cells called "Base Cells". i.e., (Transistors either NMOS (or) PMOS (or) CMOS Transistors, logic gates, NAND, NOR Gates etc.,) can be placed in a matrix form without connections is called a "Gate array", as shown in below figure.