Clamper:-

Clamper circuits are circuits which are used to clamp or fix the extrimity of periodic wave-form to some constant reference level.

→ Clamping means fixing (or) shifting.

Need for clamper:

→ The capacitor blocks the passage of direct current. when a signal is transmiting through a capacitive coupling circuit, it loses DC component.

→ It is necessary to restore the signal at later stage, the signal needs to be passed through a clamping circuit.

→ Since the clamping circuit restore or re-insert the lost DC component, it is called as DC restorer or DC re-inserter.

→ This also used when the DC value of signal is to be shifted from one level to another.

→ The clamping circuit changes only the DC level of input, but doesnot affect its shape.

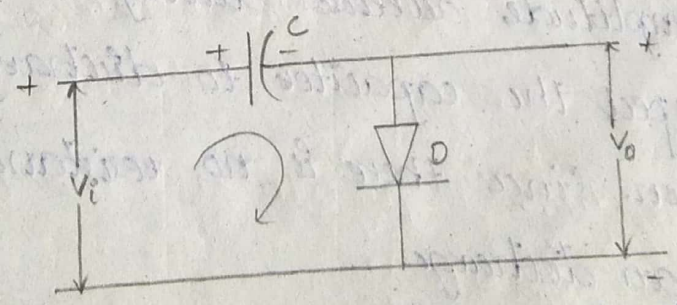
Classification of clamper

→ Positive clamper (or) negative peak clamper.

→ Negative clamper (or) positive peak clamper.

Negative clamper / Positive peak clamper

Operation:



Capacitor charges upto V_m

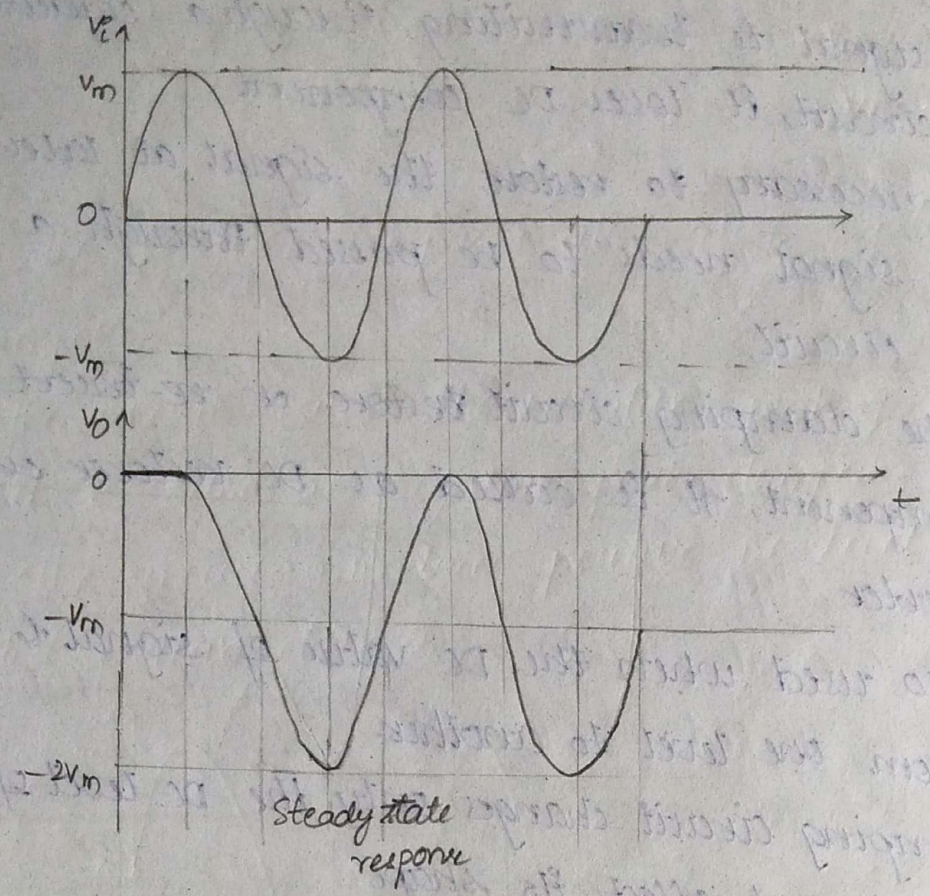
$\therefore V_c = V_m$

→ The circuit clamps the positive peak of the signal to the zero level is positive peak clamper.

The circuit introduces a negative dc level, so it is called negative clamper.

Let the input to the circuit is sinusoidal

i.e $\boxed{V_i = V_m \sin \omega t}$



→ During 1st quarter cycle of the input wave form V_i goes to positive then the diode gets forward biased conducts and the capacitor 'C' gets charged.

→ At the end of quarter cycle, the capacitor charges to $+V_m$ volts and the output voltage $V_o = 0$

→ As the amplitude decreases during second quarter cycle, we expect the capacitor to discharge, but this can't happen. Since there is no resistance through which it can discharge.

→ The voltage across capacitor 'C' remains constant (V_m volts) and it acts as a voltage source.

It follows KVL as $V_i = V_o + V_m$ and $\boxed{V_o = V_i - V_m}$

$V_c = V_m$

If $V_i = 0$

then, $V_o = 0 - V_m$

$$\boxed{V_o = -V_m}$$

If $V_i = V_m$

then, $V_o = V_m - V_m$

$$\boxed{V_o = 0}$$

If $V_i = -V_m$

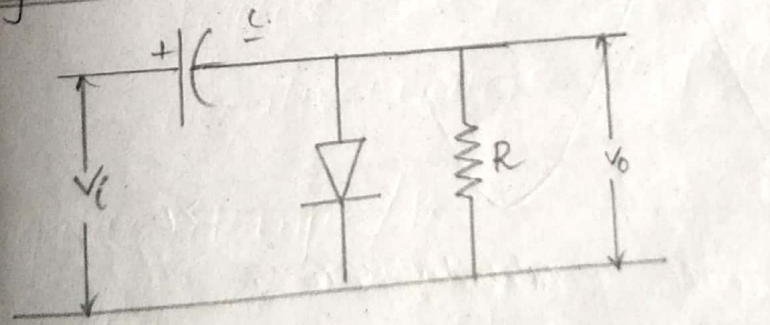
then, $V_o = -V_m - V_m$

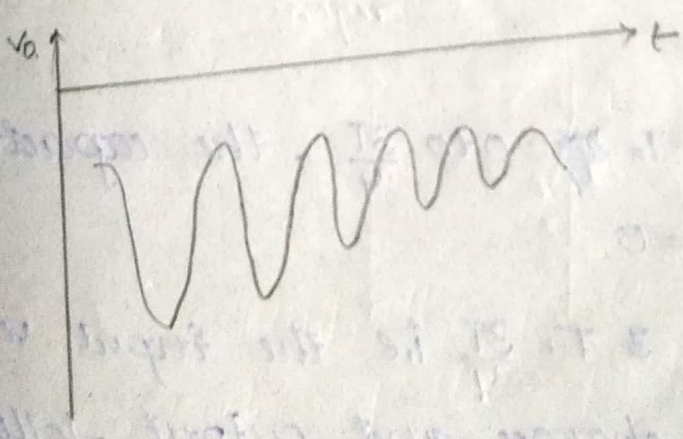
$$\boxed{V_o = -2V_m}$$

Hence peak to peak input voltage ($2V_m$) and peak to peak output voltage is equal

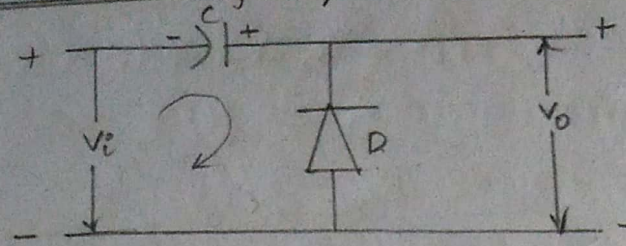
Note:-

Negative clamper with Resistor.





2. Positive clamper / Negative peak clamper



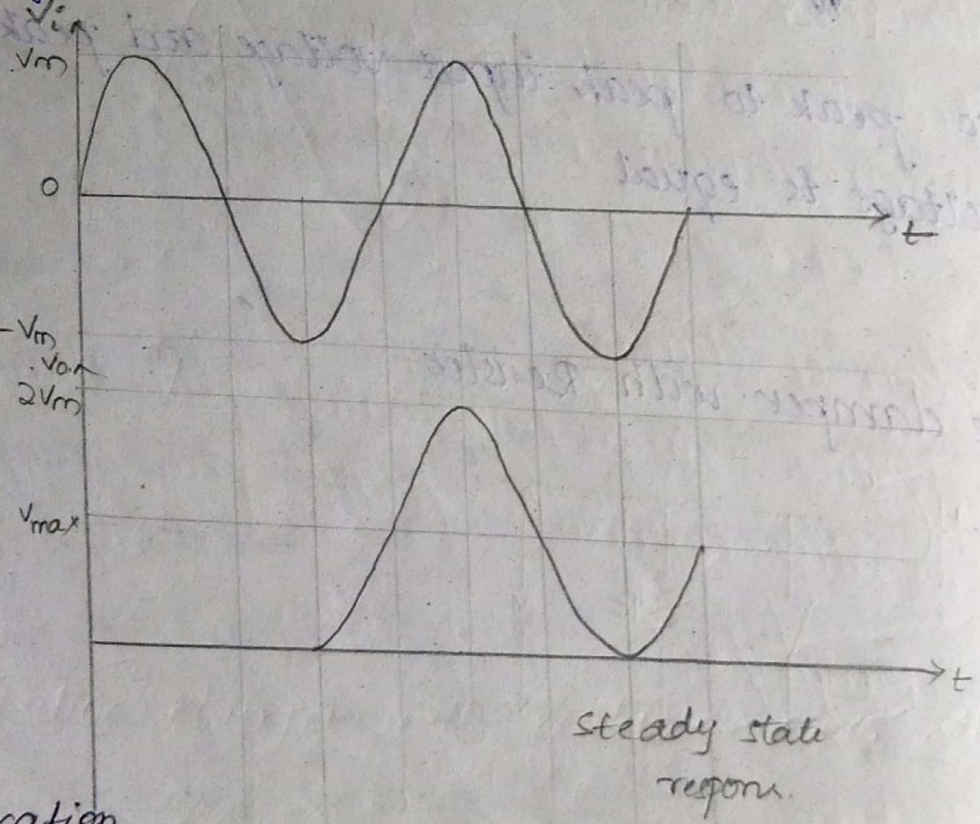
Capacitor charges upto $-V_m$

$\therefore V_C = -V_m$

The positive clamper is also called negative peak clamper.

→ The circuit clamps the negative peak of the signal from zero level so, it is called as negative peak clamper

→ The circuit introduces positive DC Level. so, it is called positive clamper.



Steady state response

Operation

→ During the time T= 0 to $\frac{3T}{4}$, the capacitor will not operate. So O/p = 0

→ when it reaches T = $\frac{3T}{4}$ i.e the input voltage is $-V_m$, the capacitor charges and output follows the input

∴ The minimum voltage required to charge the capacitor is $-V_m$

By applying KVL,

$$V_i = -V_m + V_o$$

then

$$V_o = V_i + V_m$$

If $V_i = 0$,

$$V_o = V_m$$

If $V_i = V_m$

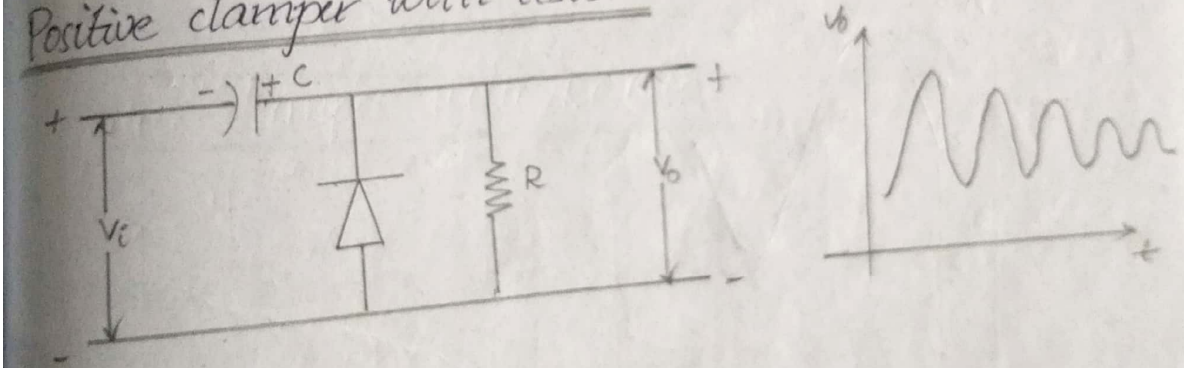
$$V_o = 2V_m$$

If $V_i = -V_m$

$$V_o = 0$$

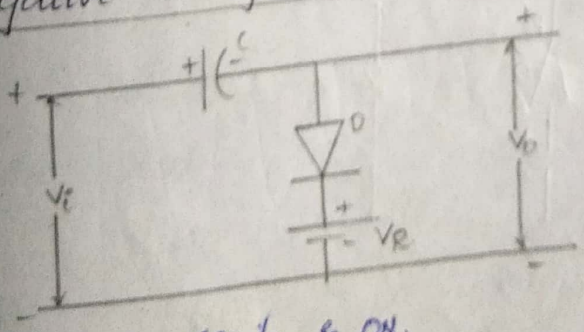
∴ Peak to peak input voltage is same as peak to peak output voltage.

Positive clamper with resistor



Biased clamper

(i) Negative clamper with +ve reference.



when diode is ON,

$$V_i - V_c - V_R = 0$$

$$V_c = V_i - V_R$$

$V_c = V_m - 2$

when the diode is OFF,

$V_i - V_c - V_o = 0$

$V_o = V_i - V_c$

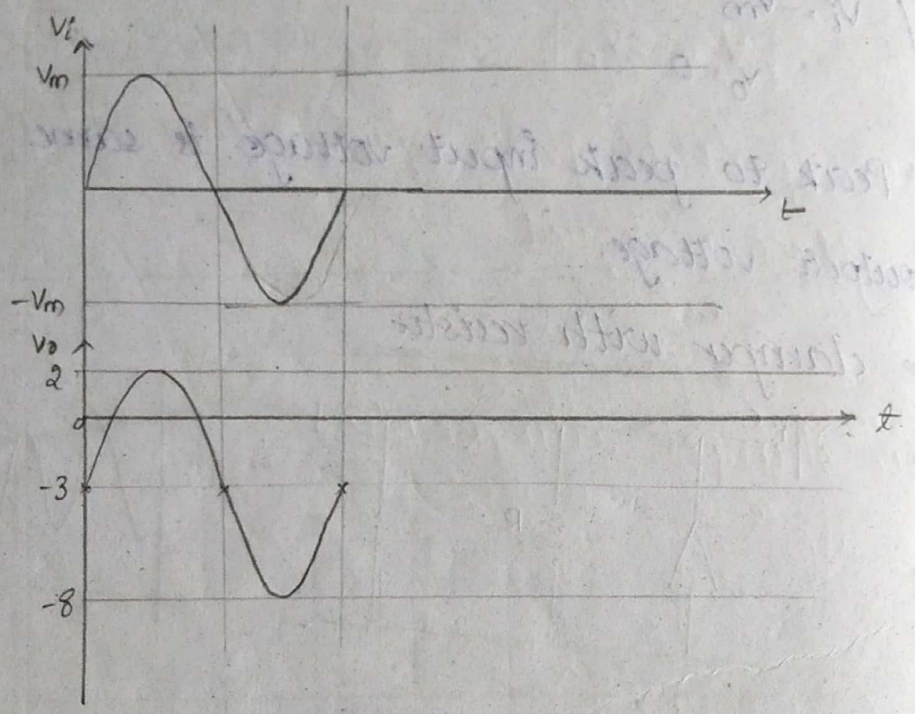
$= V_i - (V_m - 2)$

If $V_m = 5$ $\quad V_o = V_i - 3$

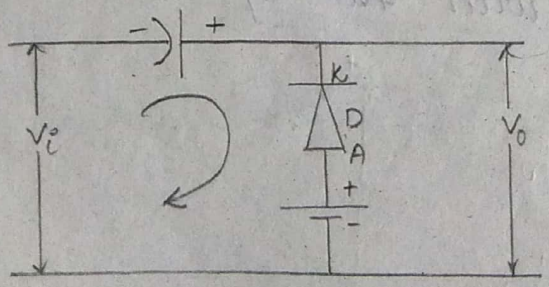
If $V_i = 0$, $V_o = -3$

$V_i = V_m$, $V_o = 2$

$V_i = -V_m$, $V_o = -8$



ii Positive clamper with positive reference voltage



When D is ON,

$V_i + V_c - V_R = 0$

$V_c = V_R - V_i$

$= V_R - (-V_m)$

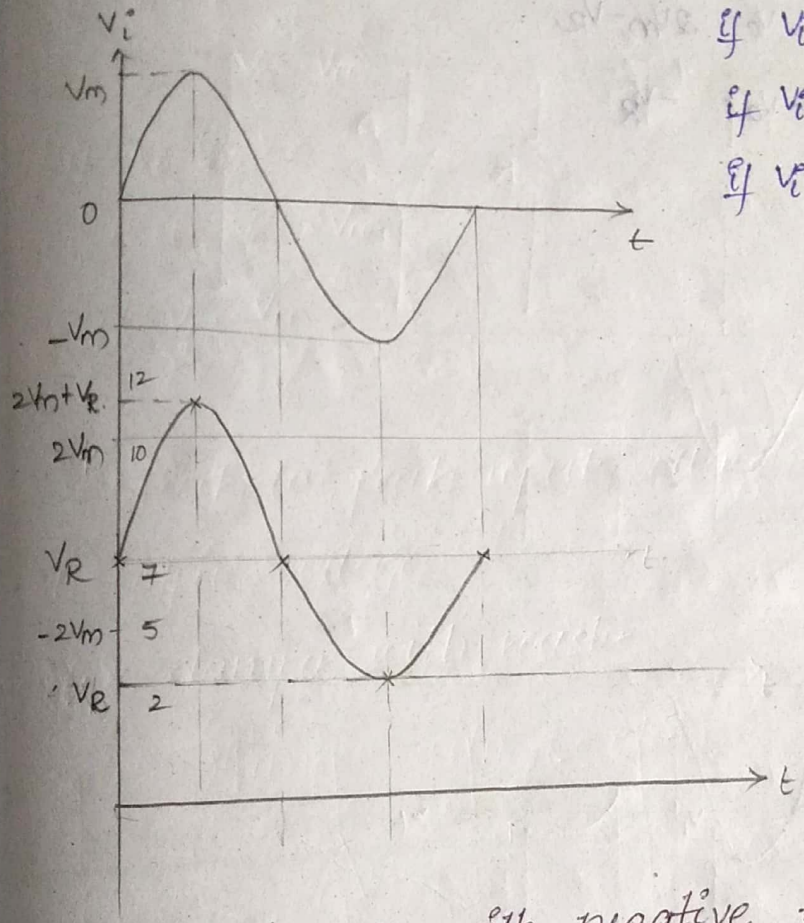
$$V_c = V_m + V_R$$

When Diode is OFF,

$$V_i + V_c - V_o = 0$$

$$V_o = V_i + V_c$$

$$V_o = V_i + V_m + V_R$$



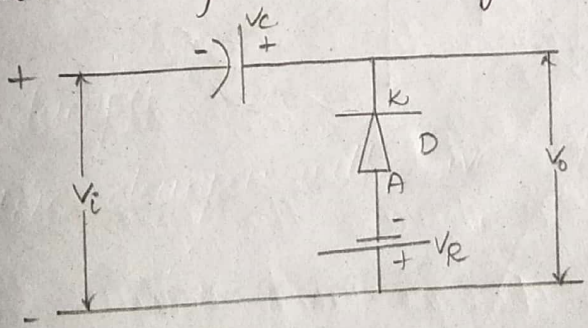
If $V_i = 0 \Rightarrow V_o = V_m + V_R$

If $V_i = V_m \Rightarrow V_o = 2V_m + V_R$

If $V_i = -V_m \Rightarrow V_o = V_R$.

If $V_m = 5$, $V_R = 2$

(iii) Positive clamper with negative reference voltage.



When Diode is ON,

$$V_i + V_c + V_R = 0$$

$$V_c = -V_R - V_i$$

$$= -V_R - (-V_m)$$

$$V_c = V_m - V_R$$

When Diode is OFF,

$$V_i + V_c - V_o = 0$$

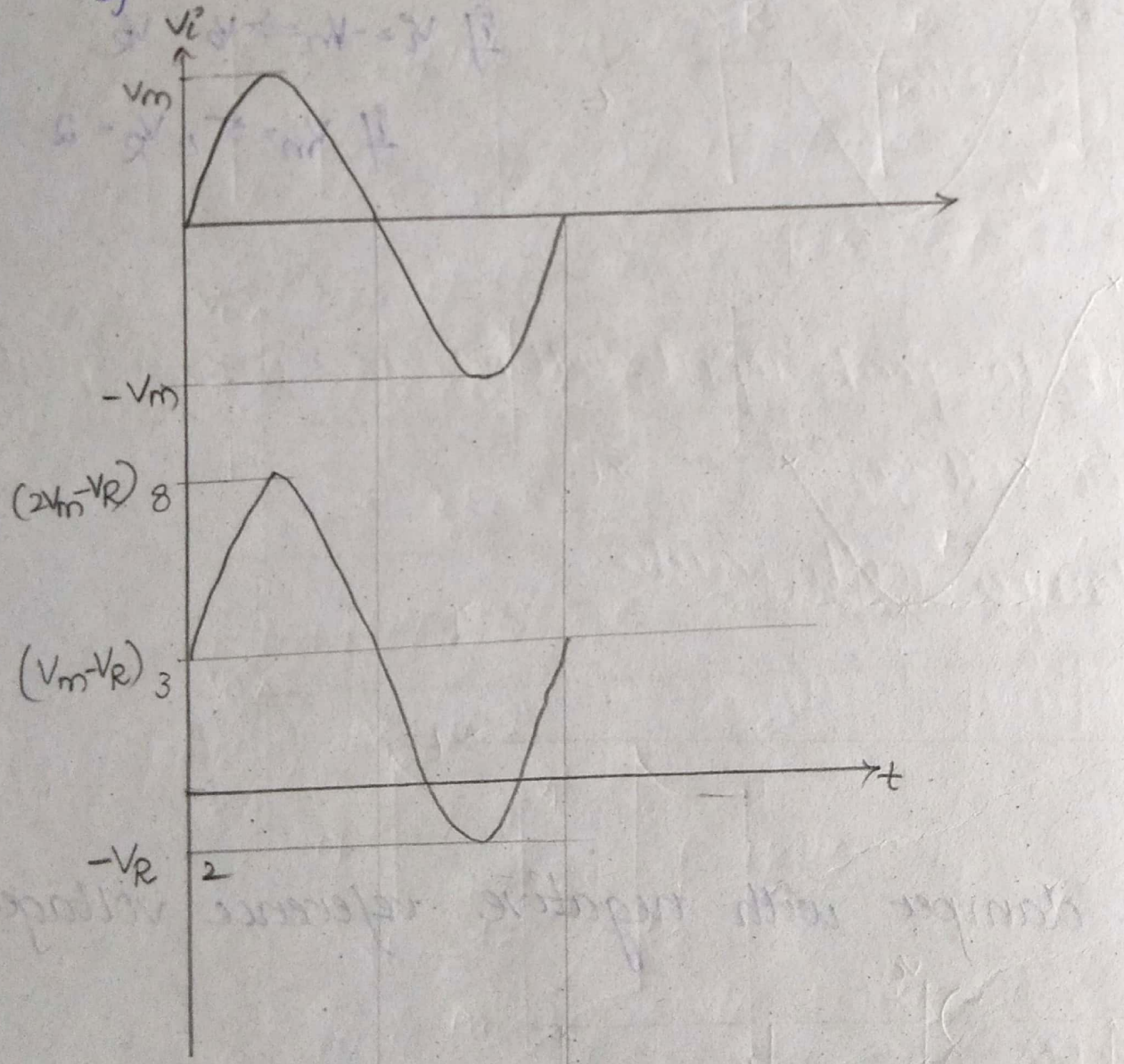
$$V_o = V_i + V_c$$

$$\boxed{V_o = V_i + V_m - V_R}$$

If $V_i = 0 \Rightarrow V_o = V_m - V_R$

If $V_i = V_m \Rightarrow V_o = 2V_m - V_R$

If $V_i = -V_m \Rightarrow V_o = -V_R$



** Clamping Circuit theorem

Statement:

Under steady state condition, the ratio of area(A_f) under the output curve in forward direction (when the diode conducts) to the area(A_r) under the output curve in reverse direction (when the diode doesn't conduct) is given by $\frac{A_f}{A_r} = \frac{R_f}{R}$

where A_f - area under the output curve in forward direction (diode is ON)

A_r - area under the output curve in reverse

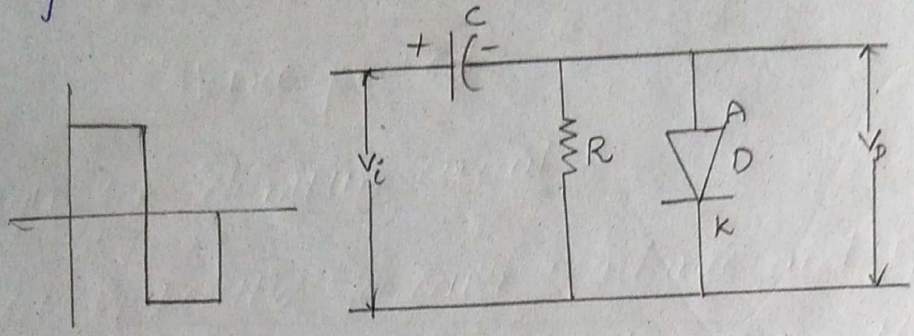
direction (diode is off)

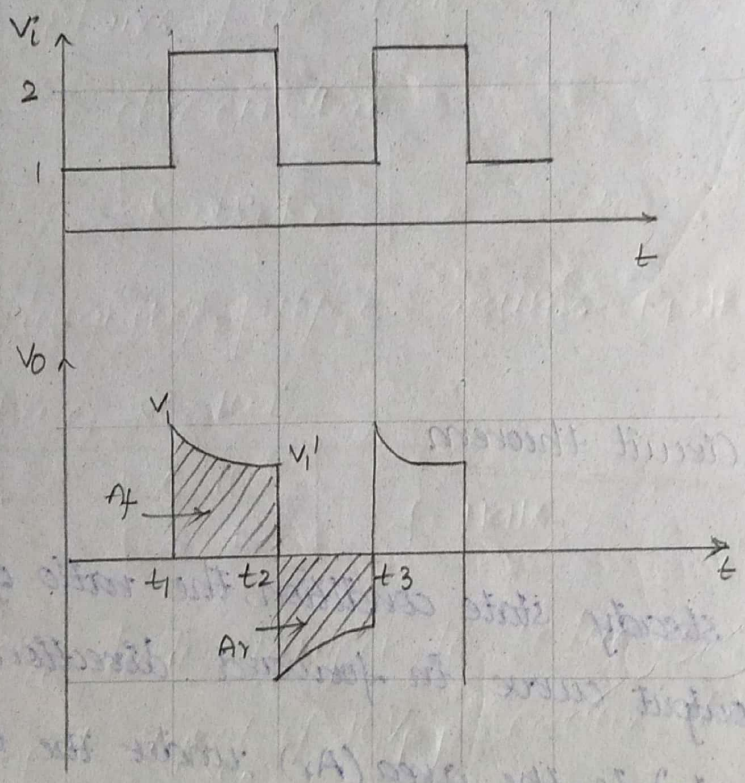
R_f - forward resistance of diode / shunt resistance

R - shunt resistance of circuit

Proof:

Let us consider a sample negative clamper and let the input be a square wave.





The diode 'D' is ON during the time interval t_1 to t_2. Hence the capacitor C charges and regains the last charge.

∴ The regained charge, q is

$$q = \int_{t_1}^{t_2} I_f \, dt$$

where I_f - forward charge of current

$$I_f = \frac{V_f}{R_f}$$

V_f - forward voltage

R_f - forward resistance

$$q = \int_{t_1}^{t_2} \frac{V_f}{R_f} dt$$

$$= \frac{1}{R_f} \int_{t_1}^{t_2} V_f dt$$

$$q = \frac{A_f}{R_f}$$

The diode 'D' is OFF during the time interval $(t_2 - t_3)$ hence the capacitor 'C' discharges and looses the gained charges. Therefore the lost charge q' is given by

$$q' = \int_{t_2}^{t_3} I_r dt$$

where I_r = Reverse current / discharging current

$$I_r = \frac{V_r}{R}$$

$$q' = \int_{t_2}^{t_3} \frac{V_r}{R} dt$$

$$q' = \frac{1}{R} \int_{t_2}^{t_3} V_r dt$$

$$q' = \frac{A_r}{R}$$

Under steady state condition, the regained charge

is equivalent to the charge lost.

$$q = q'$$

$$\frac{A_f}{R_f} = \frac{A_r}{R}$$

$$\boxed{\frac{A_f}{A_r} = \frac{R_f}{R}}$$

Hence proved.

Design for clamping circuit.

Let R_f be the forward resistance and R_r be the reverse resistance of the diode then the external shunt resistance is chosen that

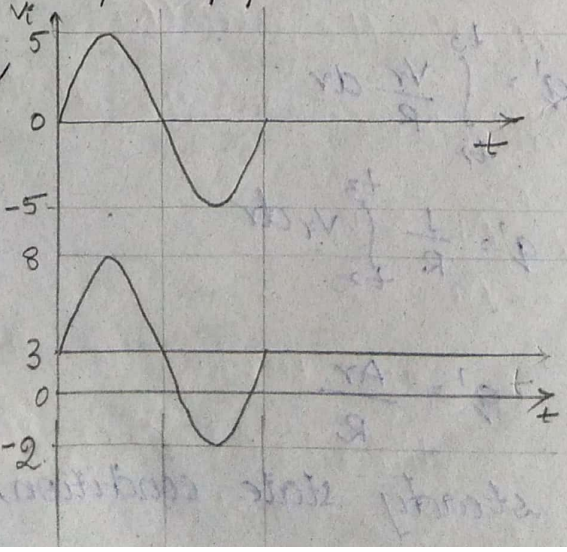
$$\boxed{R = \sqrt{R_f R_r}}$$

for designing purpose assume $R_f = 1k\Omega$, $R_r = 100k\Omega$

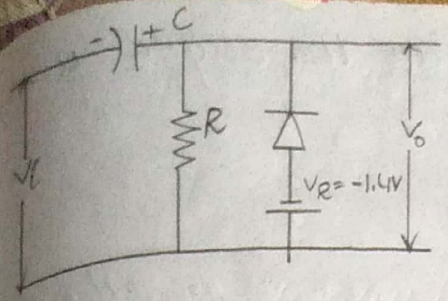
we choose $RC = 10T$

$$\boxed{C = \frac{10T}{R}}, \quad f = 1kHz$$

1. Design a diode clamper to restore a dc level of 3V to an input signal of $10V_{p-p}$. Assume the drop across the diode is 0.6V



It is positive clamper. Since the dc level is shifted above reference line



$V_R - 0.6 = -2$

In positive clamper V_R = minimum value

$V_R = -1.4V$

$R = \sqrt{R_f R_r}$

$R = 10k\Omega$

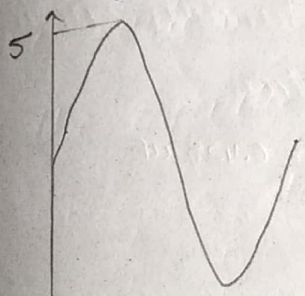
$R_f = 1k\Omega$

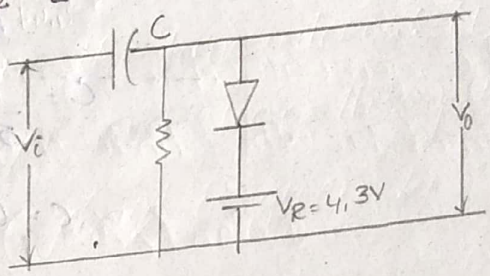
$R_r = 100k\Omega$

$C = \frac{10T}{R}$

$C = 1\mu F$

2. Design a diode clamper to store the positive peak of 1KHz input signal to the voltage level of 5V. Assume the voltage drop across the diode is 0.7V





Clamping level = $V_R + V_\gamma$

$5 = V_R + V_\gamma$

$V_R = 4.3V$

$R = \sqrt{R_f R_r}$

$R = 10k\Omega$

$R_f = 1k\Omega$

$R_r = 100k\Omega$

$C = \frac{10T}{R}$ $\quad C = \frac{10}{R_f}$ $\quad C = \frac{10}{10 \times 10^3 \times 1 \times 10^3}$

$C = 1\mu F$

3. Design a diode clamper to store the bottom peaks (negative peaks) of input signal to zero level. use a silicon diode with $R_f = 50\Omega$, $R_r = 400k\Omega$, The frequency of

the input voltage is 5 KHz. Draw the output waveform and calculate.

Unbiased clipper clamper

$V_R = V_\gamma$

$V_R = 0.7$

$R = \sqrt{R_f R_\gamma}$

$R = 10\ k\Omega$

$R_f = 1k\Omega\ 50\Omega$

$R_\gamma = 400k\Omega$

$R = \sqrt{50 \times 400 \times 10^3}$

$R = 4.47\ k\Omega$

$C = \frac{10T}{R}$

$C = 1\mu F$

$C = \frac{10}{R_f}$

$C = \frac{10}{4.47 \times 5 \times 10^3 \times 10^3}$

$C = \frac{10}{5 \times 4.47} \times 10^{-6}$

$C = 0.2 \times 10^{-6}$

$C = 0.428\ \mu F$

అమ్మ | Unit-8 | నాన్న.

Realization of Logic gates using Diodes & Transistors.

Syllabus:

AND, OR and NOT gates using diodes and Transistors. DCTL, RTL, DTL, TTL and CMOS Logic families and Comparision between the logic families.

Logic gate: Logic gates are the fundamental building block of digital system.

* A logic gate is a digital ckt with one or more inputs and only one output. Input and output of logic gates can occur in two levels. These two levels are termed High and Low or True and False or ON and OFF or simply '1' and '0'.
* The interconnection of gates to perform a variety of logical Operations is called Logic design.
* A table which lists all possible combinations of input variables & and the corresponding outputs is called a truth table.
* Logic can be either pulse logic or level logic. In pulse logic the presence of a pulse represents logic 1 and no pulse represents logic '0'. Level logic may be Positive logic or Negative logic.
* A positive logic system is the one in which the higher level represents logic 1 and the lower level represents logic '0'. → V(1) logic 1, V(0) logic 0
* A negative logic system is the one in which the higher level represents logic '0' and the lower level represents logic 1. V(0) logic 0, V(1) logic 1

Boolean algebraic expressions are only logical addition and, negation, logical multiplication no substraction, no division and no fraction.

→ In logical addition

0+0	= 0
0+1	= 1
1+0	= 1
1+1	= 1

(OR operation)

→ In multiplication.

0·0	= 0
0·1	= 0
1·0	= 0
1·1	= 1

(AND operation)

→ In negation.

$\bar{0}$	= 1
$\bar{1}$	= 0

(NOT operation)

Classifications of Logic gates:

1. OR gate
2. AND gate
3. NOT gate

} Basic gates : Any digital ckt of any complexity can be built by using only these three gates.

4. NAND gates
5. NOR gate

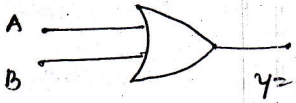
} Universal gates : By using only NAND or only NOR we can implement the basic gates.

6. XOR gate
7. XNOR gate

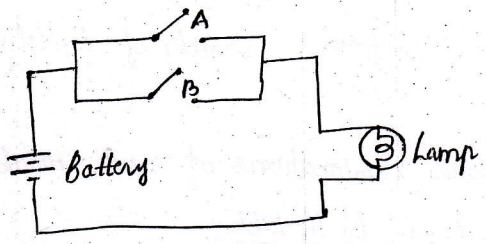
} Derived gates

Basic Gates:

OR gate:

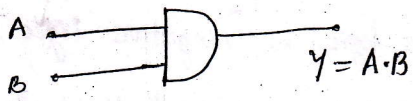


A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

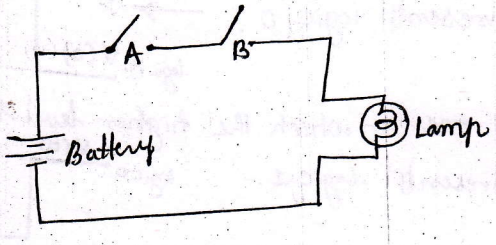


Switches		Lamp	
A	B		
Open	Open	Dark	0
Open	closed	bright	1
closed	open	bright	1
closed	closed	bright	1

AND gate:

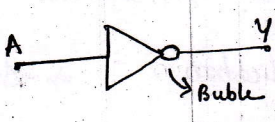


A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



Switches		Lamp	
A	B		
Open	Open	dark	0
Open	closed	dark	0
Closeit	open	dark	0
closed	closed	Bright	1

NOT gate:



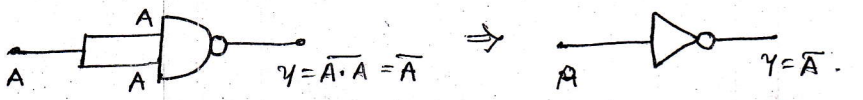
A	Y
0	1
1	0

A Not gate is also called an inverter.
It has only one input and only one output.
ie It is a device or ckt whose output is always the complement of its input.

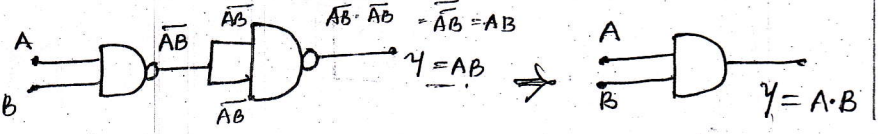
Universal gates :

(1) NAND gate as universal gate :

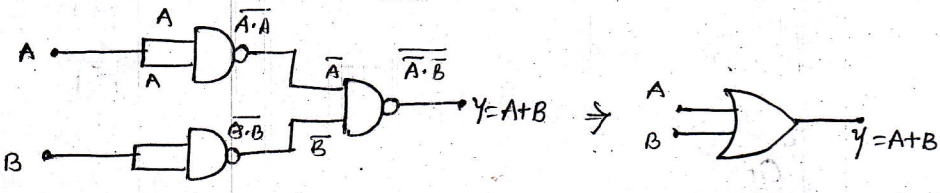
a) NOT gate :



b) AND gate :



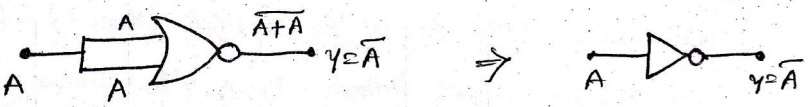
c) OR gate :



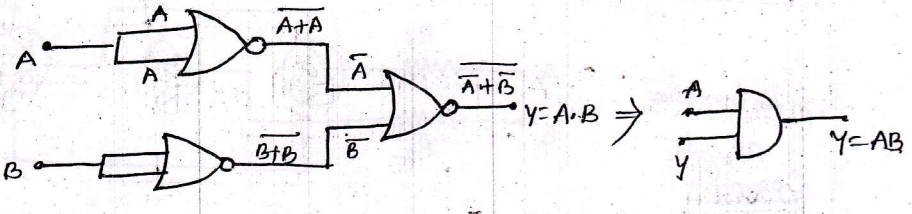
Thus the three basic gates NOT, AND, OR gates can be formed from combinations of several NAND gates only. Hence the name universal gate for the NAND gate.

(2) NOR gate as universal gate :

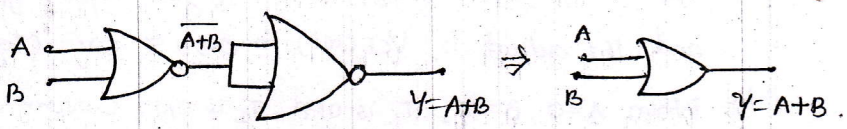
a) NOT gate :



b) AND gate :



c) OR gate :



$$\overline{\overline{A+B} + \overline{A+B}} = \overline{\overline{A+B}} = A+B.$$

Thus, the three basic gates NOT, AND, OR gates can be formed from combinations of several NOR gates only. Hence the name universal gate for the NOR gate.

—.

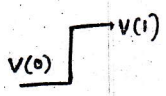
Realization of OR gate: (DL OR gate) & (RTL OR gate):

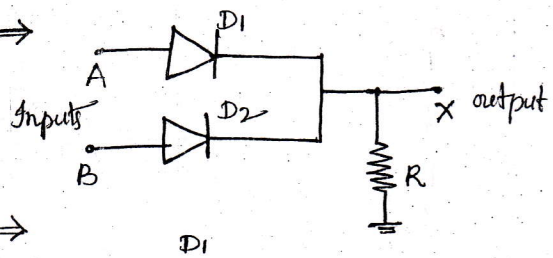
↓ Doide Logic ↳ Resistor Transistor Logic.

OR gates may be realized by using diodes or transistors.

DL OR gate:

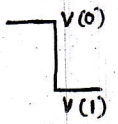
Positive logic: ⇒

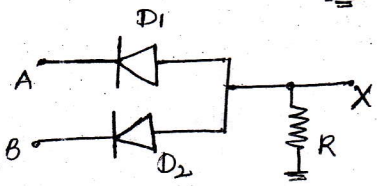




A	B	X
Low	Low	Low
Low	High	High
High	Low	High
High	High	High

Negative logic: ⇒





ie In positive logic diode

Operation:

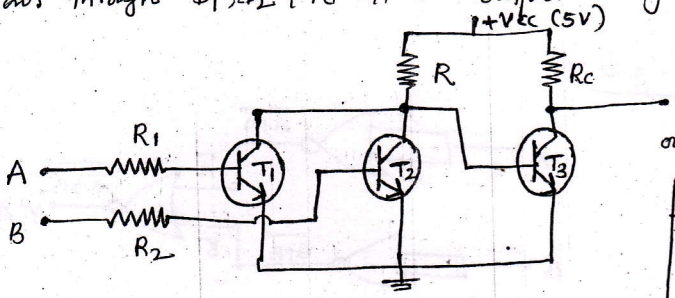
a) When both A and B are low (logic 0), both the diodes D_1 and D_2 are OFF, No current flow through R, Hence output is low (logic 0).

b) When A is low B is high, the diode D_1 is OFF and D_2 is ON, Current flows through D_2 and R, Hence output is high (logic 1).

c) When A is high, B is low, the diode D_1 is ON and Diode D_2 is OFF current flows through D_1 and R, Hence output is high (logic 1).

d) When Both A and B are high (logic 1), both diodes D_1 & D_2 are ON. Current flows through D_1, D_2 & R Hence output is high (logic 1).

RTL OR gate:



A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

In the transistor OR gate

Operation:

a) When A=0V & B=0V, both transistors T_1 & T_2 are OFF. no current flows through them. T_3 gets supply from +5V & T_3 is ON. and the output is $V_{CE(sat)} = 0.3V \cong 0V$ (logic 0) ie Low.

b) When A=0, B=5V T_1 is OFF, T_2 is ON, Current flows through T_2 & gets T_3 ON and output is Vcc ie +5V (logic 1) ie high.

c) When A=5V B=0, T_1 is ON, T_2 is OFF, Current flows through T_1 & T_3 gets OFF and ouput is Vcc = +5V (logic 1) ie high.

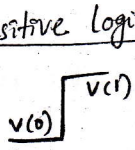
d) When both A=5V & B=5V, both transistors T_1 & T_2 are ON, now current flows through them & T_3 gets OFF. So the output is Vcc=+5V (logic 1) ie high.

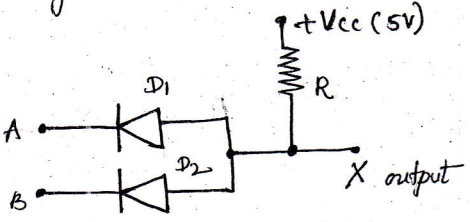
Realization of AND gate: (DL AND gate) & (RTL AND gate).

AND gate also may be realized by using diodes or transistors.

DL AND gate:

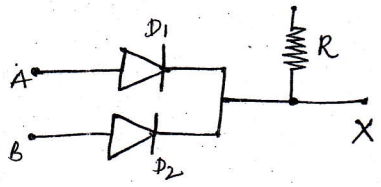
Positive logic : ⇒





A	B	X
Low	Low	Low
Low	High	Low
High	Low	Low
High	High	High

Negative logic : ⇒



In positive logic diode

Operation:

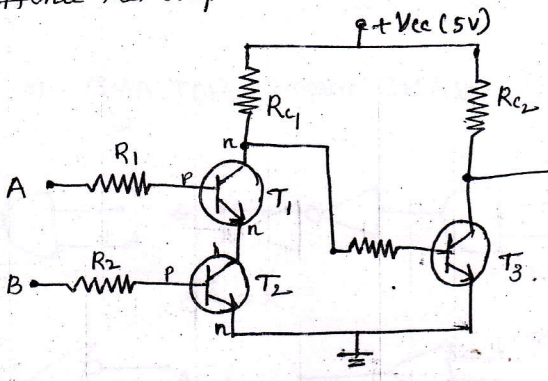
a) When both A and B are low, both diodes D_1 and D_2 are ON, Current flows through D_1, D_2 & R, So output is low (logic 0).

b) When A is low & B is high, the diode D_1 is ON and D_2 is OFF. Current flows through D_1 & R, So output is low (logic 0).

c) When A is high & B is low, the diode D_1 is OFF and D_2 is ON, current flows through D_2 & R. So output is low (logic 0).

d) When both A and B are high, both the diodes D_1 & D_2 are OFF, no Current flows them. Hence the output is $V_{cc} = 5V$ i.high (logic 1).

RTL AND gate:



A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

In transistor AND gate.

Operation:

a) When A = 0V, B = 0V, both the transistor T_1 & T_2 are OFF. no current flows through them. T_3 gets base drive from +5V supply ie T_3 is ON output is $V_{CE(sat)} = 0.3V \cong 0V$ (Logic 0) ie Low.

b) When A = 0V & B = +5V, the transistor T_1 is OFF & T_2 is ON, No current passes through them & T_3 gets ON, So output is $V_{CE(sat)} = 0.3V \cong 0V$ (logic 0) ie Low.

c) When A = +5V & B = 0V, the transistor T_1 is ON and T_2 is OFF, No Current passes through them and T_3 gets ON., So output is $V_{CE(sat)}$ as $0.3V \cong 0V$ (Logic 0) ie Low.

d) When both A = 5V, B = 5V, both the transistors T_1 & T_2 are ON, now Current flow through them & transistor T_3 gets OFF, So output is $V_{cc} = 5V$ (logic 1) ie high.

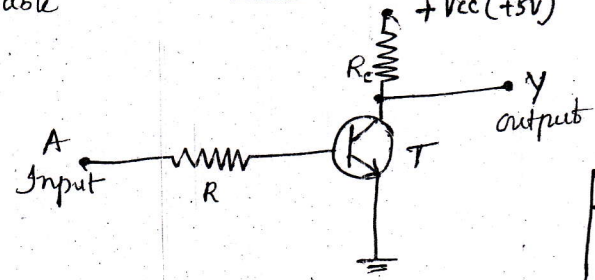
Realization of NOT gate : (RTL NOT gate) (or) Inverter :

A discrete NOT gate may be realized using a transistor.

A	Y
0	1
1	0

$Y = \overline{A}$ → over bar

RTL NOT gate :



A	Y
Low	High
High	Low

Operation:

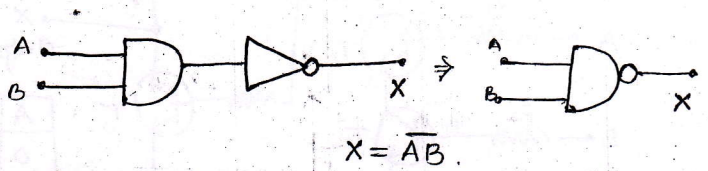
a) When A is low (A=0), transistor T is OFF.
No current flows through R_c, no voltage drop occurs across R. So the output X is +5V, high (logic 1).

b) When A is high (A=+5V), transistor T is ON, current flows through R_c. So, the output is $V_{CE(sat)} = 0.3V \cong 0V$ (logic 0) ie low.

Logic ckts which use these three gates only are called AOI logic ckts (AND/OR/Inverter).

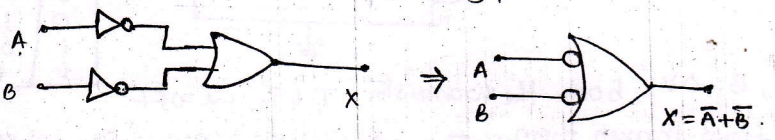
& Logic ckts which use AND gates & OR gates only are called AO logic ckts.

NAND gate : NAND means NOT AND. ie AND output is NOTed.



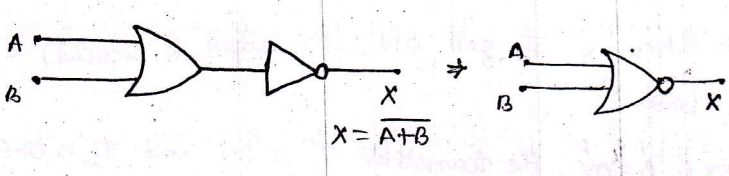
A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

(or)



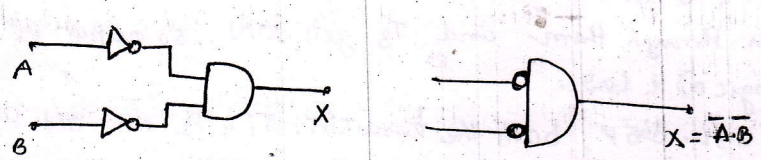
A	B	$\bar{A}$	$\bar{B}$	X
0	0	1	1	1
0	1	1	0	1
1	0	0	1	1
1	1	0	0	0

NOR gate : NOR means NOT OR gate. OR output is NOTed.



A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

(or)



A	B	$\bar{A}$	$\bar{B}$	X
0	0	1	1	1
0	1	1	0	0
1	0	0	1	0
1	1	0	0	0

Realization of NOR gate: (DTL - NOR gate) & (RTL NOR gate)

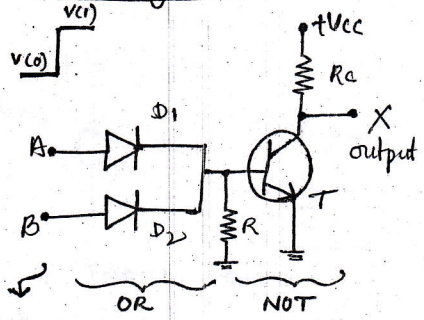
↳ Diode Transistor Logic.

A discrete two input NOR gate using diodes and transistors as

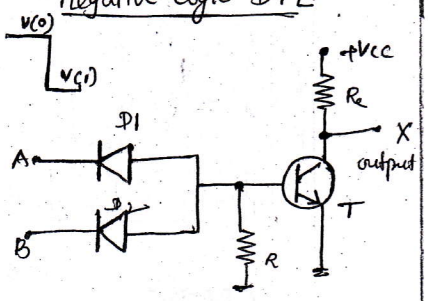
DTL-NOR gate:

A	B	X	
Low	Low	High	1
Low	High	Low	0
High	Low	Low	0
High	High	Low	0

Positive Logic DTL



negative Logic DTL



Operation:

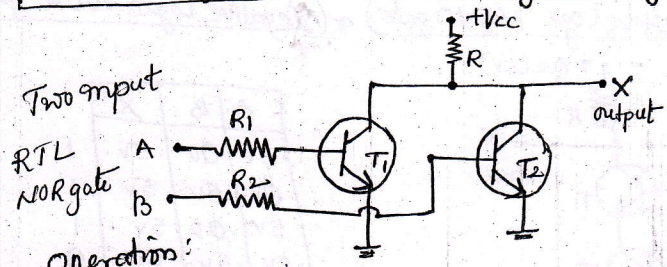
a) When both A and B are Low, both diodes D_1 & D_2 are OFF & Transistor T is OFF no current flows through Rc, Hence output voltage $X = V_{cc} = +5V$ ie logic 1 - High,

b) When A is low & B is high, diode D_1 is OFF and D_2 is ON, Current flows through D_2 & R, Transistor T will ON. Hence output $X = V_{CE(sat)} = 0.3V \cong 0V$ logic 0 ie Low.

c) When A is high & B is Low, diode D_1 is ON, D_2 is OFF, Current flows through D_1 & R, transistor T is ON, Hence output $X = V_{CE(sat)} = 0.3V \cong 0V$, logic 0 ie Low.

d) When both A and B are high, both diodes D_1 & D_2 are ON, current flows through D_1, D_2 & R, then transistor T is ON. Output $V_{CE(sat)} = 0.3 = 0V$ ie Low.

RTL NOR gate: Positive logic NOR gate (or) Negative logic NAND gate:



A	B	X	
0V	0V	5V	1
0V	5V	0V	0
5V	0V	0V	0
5V	5V	0V	0

Operation:

a) When both A = 0V & B = 0V, both transistors T_1 and T_2 are OFF, So no current flows through R, Hence the output $X = V_{cc} = +5V$, logic 1 ie High.

b) When A = 0V and B = 5V, the transistor T_1 is OFF & transistor T_2 is ON. Current flows through R & T_2. Hence the output $X = V_{CE(sat)} = 0V$ ie Logic 0 ie Low.

c) When A = +5V and B = 0V, the transistor T_1 is ON and transistor T_2 is OFF So Current flows through R & T_1, Hence the output voltage $X = V_{CE(sat)}$ as $0.3V \cong 0V$ Logic 0 ie low.

d) When both A = +5V, B = +5V, both the transistor T_1 & T_2 are ON, So Current flows through T_1, T_2 & R. Hence the output voltage $X = V_{CE(sat)}$ as $0.3V \cong 0V$. Logic 0 ie Low.

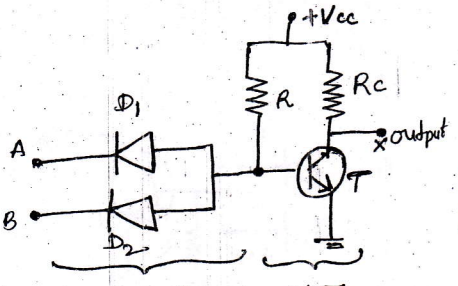
Realization of NAND gate: (DTL NAND gate) & (RTL NAND gate) & (TTL NAND gate).

A discrete two input NAND gate using diodes and transistors as.

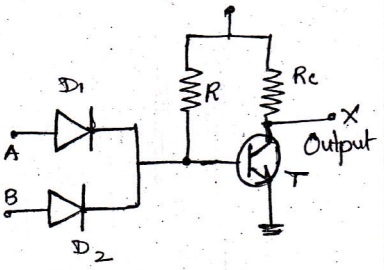
DTL NAND gate:

A	B	X	
Low	Low	High	1
Low	High	High	1
High	Low	High	1
High	High	Low	0

Positive Logic DTL



Negative Logic DTL



Operation:

a) When both inputs A and B are Low, both diodes D_1 & D_2 are ON, current flows through R, D_1 & D_2. Transistor T is OFF, Hence the output is Vcc ie high

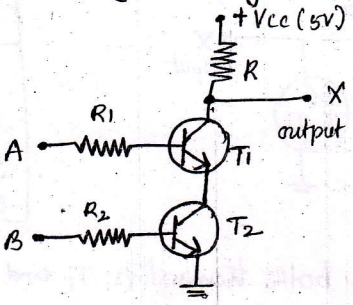
b) When input A is Low and B is high, diodes D_1 is ON and D_2 is OFF, So, current flows through D_1 & R. Transistor T is OFF, Hence the output voltage $X = V_{CE(sat)} + 5V$ ie logic 1, high.

c) When input A is high, B is Low, diodes D_1 is OFF and D_2 is ON, So, Current flows through D_2 & R, Transistor T is OFF, Hence output is Vcc ie high.

d) When both inputs A and B are high, both diodes D_1 & D_2 are OFF, So no current flows through them and transistor T is ON, So output is $V_{CE(sat)} = 0.3V = 0V$ ie Low.

RTL NAND gate: (Positive Logic NAND gate) or (Negative Logic NOR gate):

Two input RTL NAND gate.



A	B	X	
0V	0V	5V	1
0V	5V	5V	1
5V	0V	5V	1
5V	5V	0V	0

Operation:

a) When both inputs A = 0V & B = 0V, both transistors are OFF, no current flows through R, So output is Vcc = +5V ie logic 1, high.

b) When the input A is 0V & B = +5V, the transistor T_1 is OFF & T_2 is ON. So, current flows through R, So, output is Vcc = +5V, Logic 1, High.

c) When input A = +5V, B = 0V, the transistor T_1 is ON & T_2 is OFF no current flows through R, So output is Vcc = +5V, Logic 1, high.

d) When both the inputs A = +5V and B = +5V, both the transistors T_1 and T_2 are ON, short circuited to ground & Current flows through R, So the output voltage $X = V_{CE(sat)} \times 2 = 0.3 + 0.3 = 0.6 \simeq 0V$ logic 0 ie Low.

Applications of Logic gates:

1. Logic gates are extensively used in digital system such as computer, digital communication systems, in data processing and control and also finds wide amplification in measuring instruments and simulation systems.
2. Logic gates are usually embedded in large scale integrated ckts (LSI) and very large scale integrated ckts (VLSI) along with a large no. of other devices are not easily accessible (or) identifiable.
3. Logic gates are used for implementing boolean algebraic equations as the digital ckts responds to logic '0' and logic '1'.
4. Logic gates are used in major integrated logic families like TTL ie transistor transistor logic, CMOS - Complementary metal oxide semiconductor logic for their designing purpose.
5. X-OR gate is applied in the ckt known as Controlled inverter. XNOR gate is applied as a digital Comparator.

Transistor Transistor Logic (TTL):

TTL NAND gate:

TTL is an improvement over the earlier versions like RTL and DTL

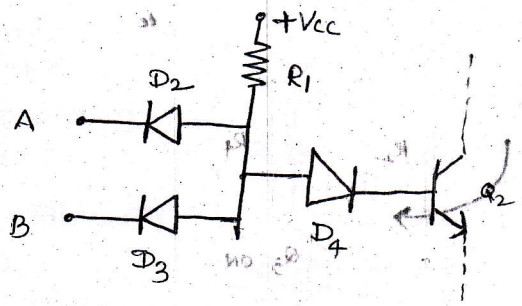
The ckt uses a multi-emitter transistor Q_1. A multi emitter transistor is a transistor having several emitters, all joined to a common base, but only one collector.

The no. of emitters may be as high as eight.

It is usual to have as many emitters as there are inputs to the logic gate.

The two emmitter-base jun are replaced by the diodes D_2 & D_3 & the collector base jun is replaced by the diode D_4

ie

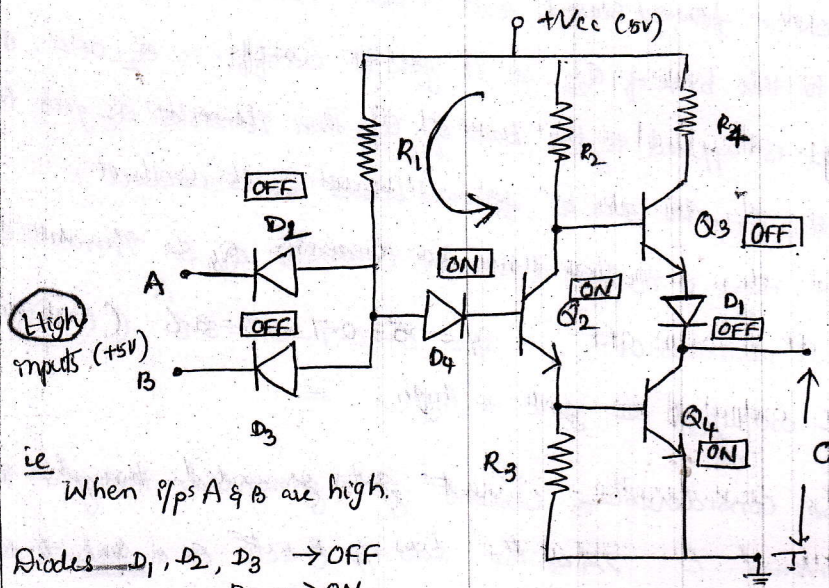


Operation: On the output side of the TTL gate, there are two transistors Q_3 & Q_4 with Diode D_1 in between, arrangement to form a totem pole. During normal operation of the gate either Q_3 or Q_4 conducts, depending upon the logic state of the output.

(i) Operation when all inputs are high:

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NAND gate.



ie When i/p's A & B are high.

Diodes $D_1, D_2, D_3 \rightarrow$ OFF
$D_4 \rightarrow$ ON.

Transistors $Q_2 - Q_4 \rightarrow$ ON
$Q_3 \rightarrow$ OFF.

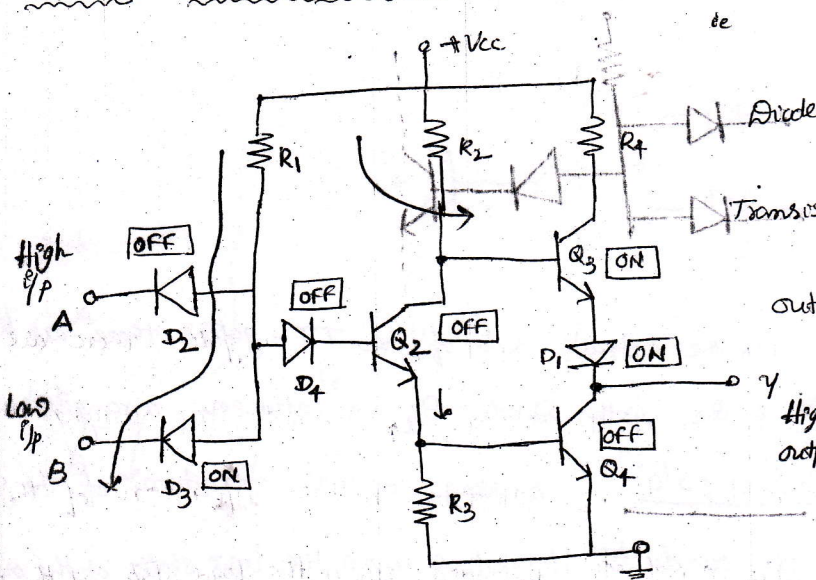
Output is Low.

ie When both i/ps A & B are high the diodes D_2 & D_3 are reverse-biased & hence they are OFF ie there is no conduction through them.

The supply voltage Vcc forces a current through resistor R_1 & diode D_4 gets forward biased & it allows to the base of transistor Q_2. then transistor Q_2 goes to saturation.

The collector current of Q_2 is appeared at the base of Q_3 then it goes to cutoff ie OFF. & Diode D_1 OFF. $V_{CE(sat)}$ of Q_2 = 0.1 V. $V_{BE(sat)}$ of Q_2 = 0.8 V ≈ 1. So Transistor Q_4 goes to saturation. since the emitter current of Q_2 supplies the necessary base-drive for transistor Q_4 & Hence Q_4 turns ON.

(ii) Operation when any one of the inputs is low:



ie Input A ... High
Input B ... Low

Diodes D_1, D_3 → ON
D_2, D_4 → OFF.

Transistors Q_3 → ON
Q_2, Q_4 → OFF.

output → High

ie. When i/p terminal A is high & B is low, hence D_2 goes to OFF state & D_3 goes to ON ie forward biased & it conduct. Hence diode D_4 OFF state. It is applied to the base of Q_2, so it goes to cutoff. ie Q_2 OFF. Its collector voltage is applied to the base of Q_3 then transistor Q_3 goes to saturation. (Vcc) & D_1 also goes to forward biased & its conduct. Since Q_2 is OFF there is no base drive for transistor Q_4 So. Transistor Q_4 is goes to cutoff it remains OFF. $Y = 5 - 0.7 - 0.7 = 3.6$ (High voltage).

Hence the output of the gate is high.

Sink: The considerable current gets grounded through the input terminal B as the Low i/p B acts as a sink to the ckt.

Hence the above TTL logic gate as work as NAND gate.

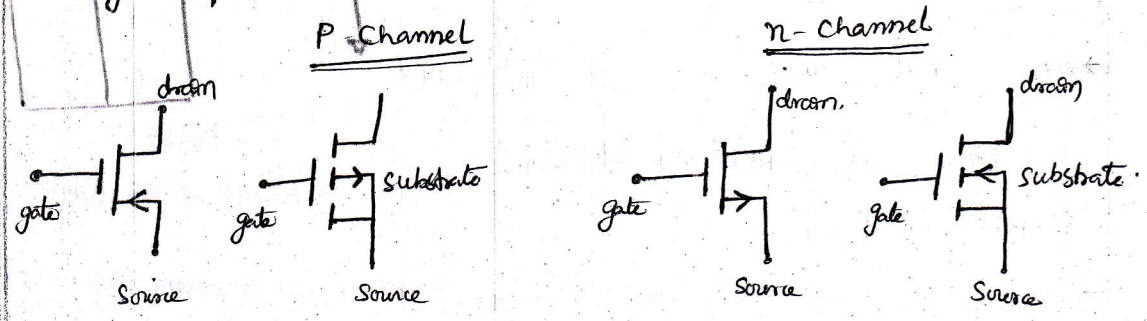
Complementary Metal Oxide Semiconductor Logic Ckts : (CMOS)

There are two types of field effect transistors

1. JFET (Junction field effect transistor)
2. MOS (Metal Oxide Semiconductor).

MOS transistors can be fabricated on less area than Bipolar transistors.

Symbols for MOS transistors:



CMOS ckts consists of both types of MOS devices i.e p-channel & n-channel interconnected to form logic functions.

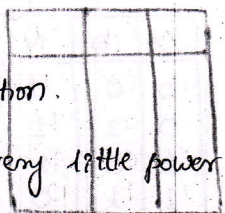
CMOS devices are chips in which both p-channel & N-channel MOSFETs are connected in a push-pull arrangement.

Behavior :

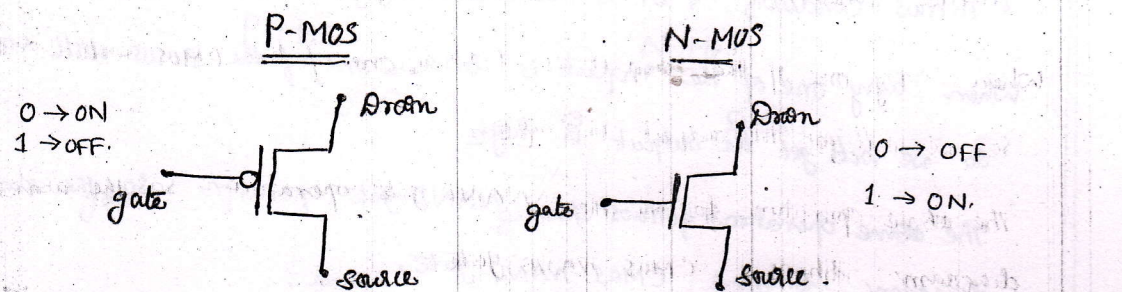
→ The n-channel MOS conducts when its gate-to-source voltage is +Ve.

→ The p-channel MOS conducts when its gate-to-source voltage is −Ve.

Characteristics of CMOS :

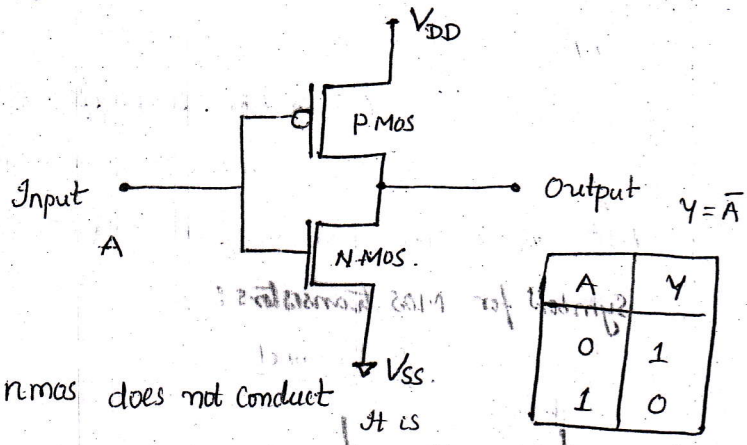


1. Simple & Cheaper in fabrication.
2. Small in size & consume very little power.
3. MOS ICs do not use the IC resistance elements so they occupy much less space on a chip.
4. Fabrication of MOS ICs is not so complex as TTL ICs.
5. Low operating speed.
6. Power dissipation is very low.



CMOS - Inverter & NOT gate :

Input	Output
Low	High
High	Low

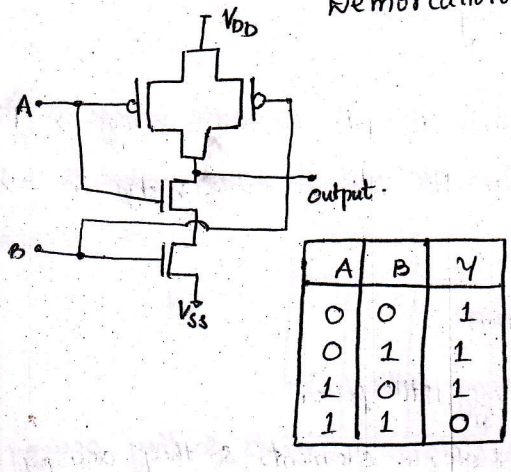


A	Y
0	1
1	0

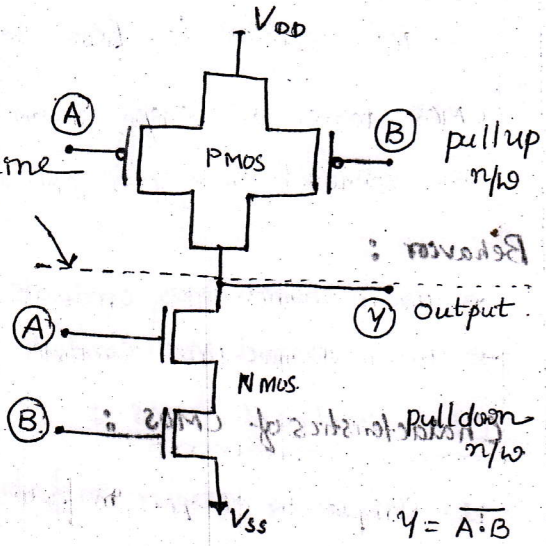
→ When input is low (0) nmos does not conduct It is Open ckted. Pmos will conduct & short ckted. V_{DD} is appears at the output which is high (1)

→ When input is high pmos does not conduct it is open ckted & n-mos will conduct & it is short ckted to ground. So, output is low.

CMOS - NAND gate :



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



When both inputs are low i.e $A=0, B=0$. PMOS conducts & n-mos does not conduct. So V_{DD} is appeared at the output. i.e Output is high

When both inputs are high i.e $A=1, B=1$. PMOS does not conduct & n-mos conducts. & it is connected to ground, Hence output is low.

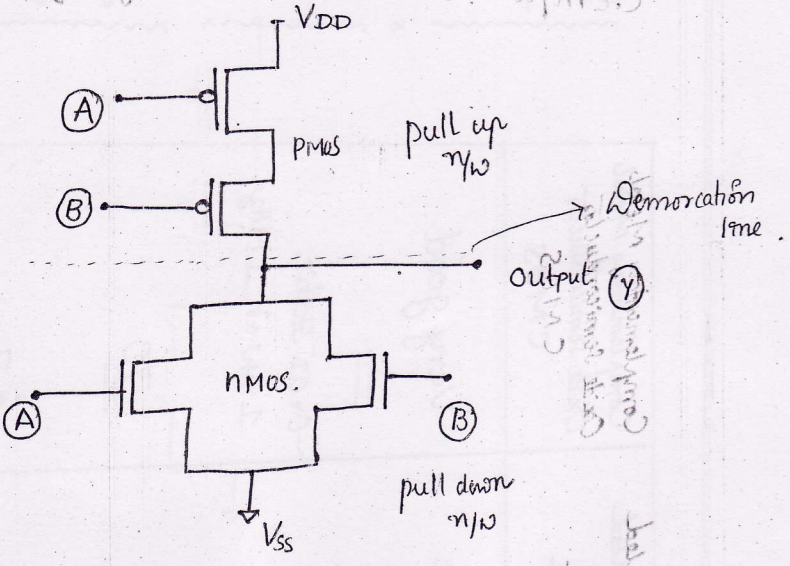
When any one of the input is low the one of the PMOS will conduct. So we will get the output is high.

The above operation follows the NAND gate operation So the above diagram shows CMOS NAND gate.

CMOS - NOR gate :

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

$Y = \overline{A+B}$



When both inputs are low i.e A = 0, B = 0. both PMOSes are conduct & V_{DD} is transmitted to the output since both nMOSes are does not conduct. Hence output is high.

When any one of the input is high & both inputs are high the nMOS will conduct & shortcikted to ground. pmos will not conduct. Hence output is low.

Hence above logic gate follows CMOS NOR gate Operation.

Pullup Network : Pull up network is a P & n mos switches with one terminal is connected to V_{DD} & another terminal is connected to the output.

Pull down Network : Pull down network is a n & p mos switches with one terminal is connected to output & another terminal is connected to the Vss which is ground.

Demorcation line : Demorcation line is a line which seperates pullup network and pull down network. above PMOS should present & below nMOS should present.

CMOS AND gate : CMOS AND is CMOS NAND followed by Inverter.

CMOS OR gate : CMOS OR is CMOS NOR followed by Inverter.

↓ Complementary.

[PTO]

Comparison between the logic families of 90M 20MO

SL No	Parameter	Resistor Transistor Logic RTL	Diode Transistor Logic DTL	Transistor Transistor Logic TTL (Standard)	Emitter Coupled Logic ECL	Complementary Metal Oxide Semiconductor CMOS
1	Noise Immunity	Average	Good	Very good	Average	Very good.
2	Power Dissipation per gate (mW)	12	8-12	10	40-55	0.01 static 1mW at 1 MHz.
3	Propagation Delay per gate (nSec)	14	30	10	2	70
4	Figure of Merit (PJ)	168	300	100	95	0.7
5	Clocking Rate (MHz)	8	72	35	Above 60	10
6	Fanout	5	8	10	25	Above 50

Characteristics of Logic families :

1. **Propagation Delay :** Propagation delay is the max. time taken by output to change its state in response to input. It determines the speed of operation of a gate.

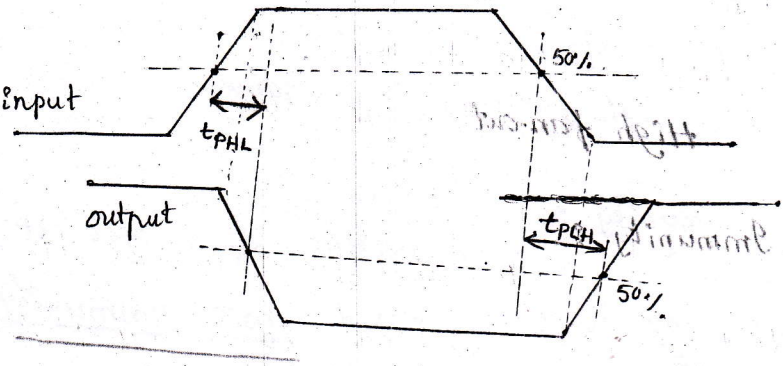


Fig : I/p - O/p waveforms for propagation delay.

Propagation delay (t_p) is average of the two times t_{PHL} & t_{PLH} & the times are measured from 50% of voltage levels.

where t_{PHL} → The time delay when output goes from High to Low state.

t_{PLH} → The time delay taken by the o/p to go from Low to high state.

ie. $$t_p = \frac{t_{PHL} + t_{PLH}}{2}$$ = Propagation delay (nsec).

2. **Power Dissipation :** P_D Power Dissipation is defined as the power dissipated in an IC & It is measured in mW

Low power dissipation is desirable in any digital IC.

3. **Figure of merit :** Figure of merit is defined as the product of propagation delay (nsec) and power dissipation (mw) & It is measured in pico joules. (PJ). It is also known as speed power product. ie.

Figure of merit = Propagation delay × Power dissipation

$= t_p \times P_D$

$= n\text{sec} \times mW$

$= PJ$.

4. **Fan In :** The fan In of a logic gate is defined as the no. of inputs (coming from similar ckts) that a logic gate can handle properly.

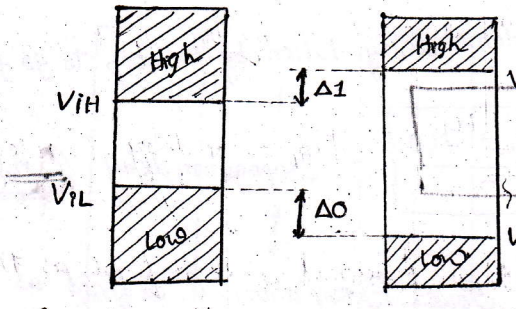
5. **Fan-Out :** or **Loading factor :** The fan-out is defined as the max. no. of standard logic inputs that an output can drive without affecting the inputs.

High fan-out is desirable.

6. **Noise Immunity :** The ability of a logic ckt to tolerate the effect of noise is called noise immunity.

(or) noise voltages on its i/ps.

The amount by which a ckt can effect of noise (or) quantitative measure of noise immunity is called noise margin.



$\Delta 1$ = High state noise margin

$\Delta 0$ = Low state noise margin.

$\Delta 1 = V_{OH} - V_{IH}$

$\Delta 0 = V_{IL} - V_{OL}$

Higher noise margin is desirable for logic ckts or families.

7. **Operating Temperature :** Digital ICs should be capable of operating for temperature ranging from 0 to +70°C for industrial applications and the range of −55°C to +125°C for military applications.

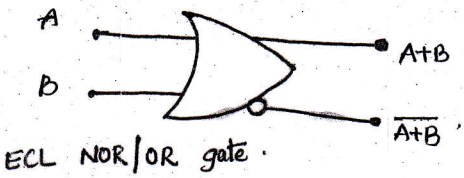
Emitter Coupled Logic (ECL):

→ ECL is the fastest of all logic families

→ In ECL the transistors are used in differential amplifier configuration.

→ ECL provides two outputs which are always complement of each other.

→ Due to low noise margin ECL is an unsuitable for use in heavy industrial environments.



ECL NOR/OR gate.

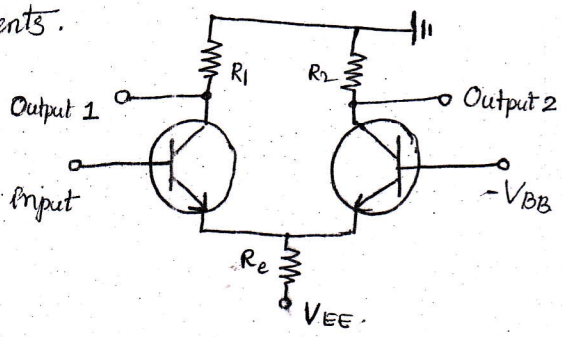


fig: Basic ECL ckt

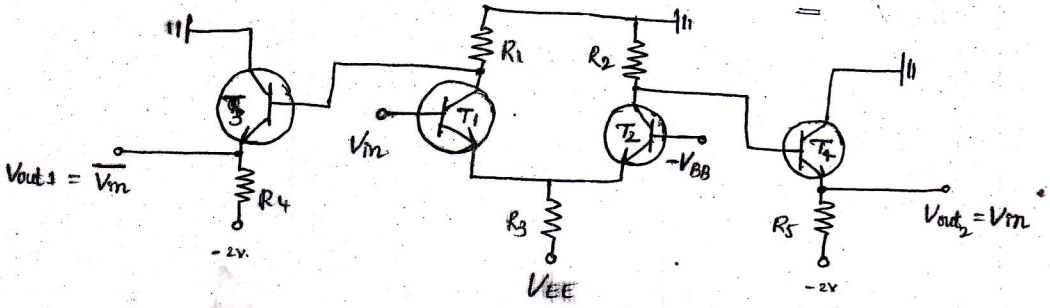


Fig: Basic ECL with addition of Emitter followers.

ie ECL ckt can be used as an Inverter.

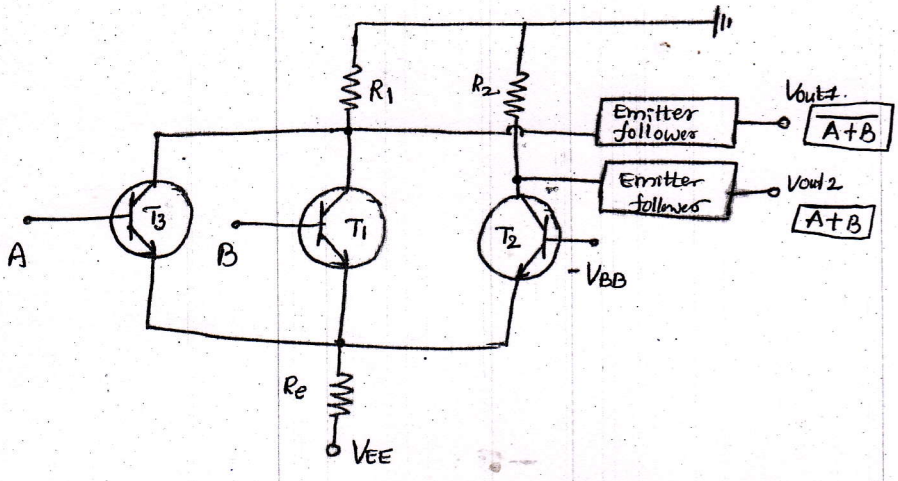


fig: ECL NOR/OR ckt.

Drawbacks:
1. Low noise margin
2. Higher power drain.
3. Its -Ve voltage supply & logic familes which are not compatible with other logic family

Cont'd

Unit - 4

Multivibrators

Syllabus : Analysis and Design of Bistable, Monostable, Astable Multivibrators and Schmitt trigger ckt using BJT.

Multivibrator : A multivibrator is basically a two stage RC Coupled amplifier with positive feedback from the output of one amplifier to the input of the other.

* Multivibrator is a switching ckt and may be defined as an electronic ckt that generates non-sinusoidal waves such as rectangular waves, sawtooth waves, square waves etc.
* Multivibrators are capable of storing binary numbers, counting pulses, synchronizing arithmetic operations and performing other essential functions used in digital systems.

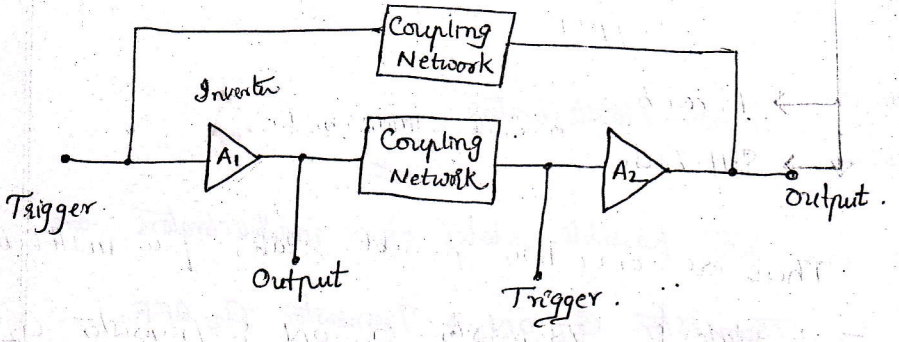


Fig: Basic configuration of a Multivibrator.

Multi means many, Vibrator means Oscillator.

A ckt which can oscillate at a no. of frequencies is called a multivibrator.

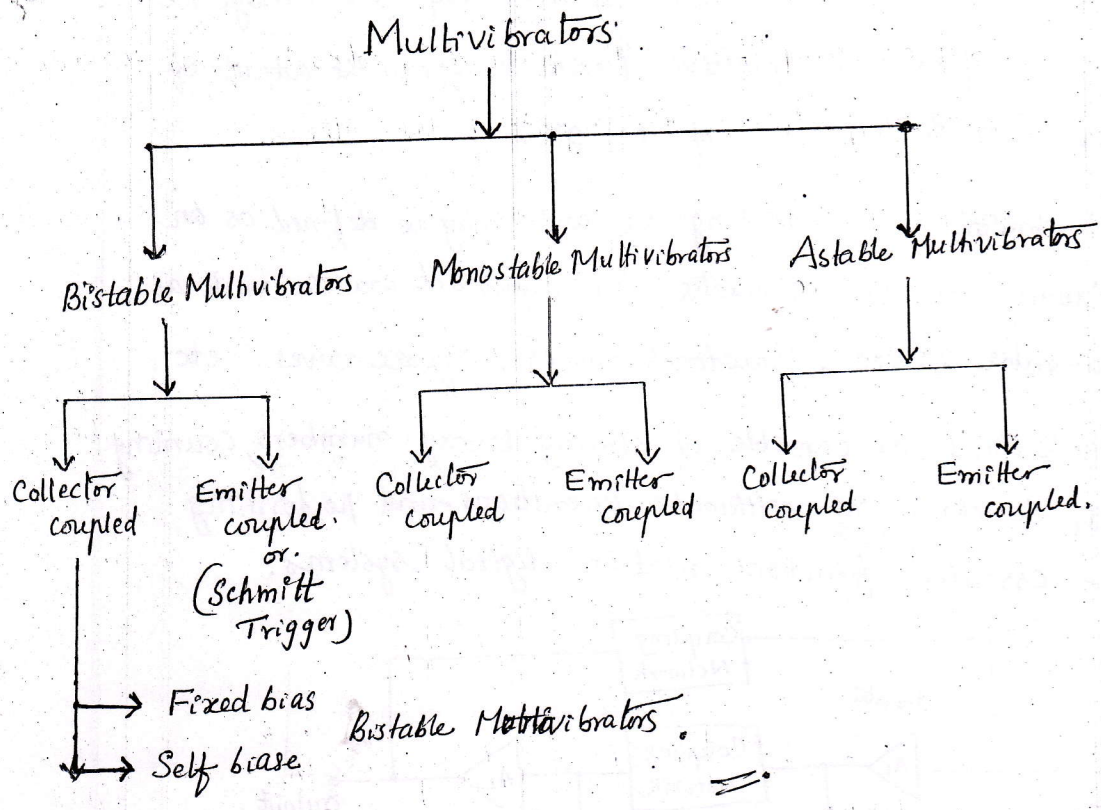
→ Multivibrators have two stage cross coupled inverters.

ie The output of the first stage is coupled to the input of the second stage and the output of the second stage is coupled to the input of the first stage. Hence Multivibrators called as Regenerative Amplifiers.

Classifications of Multivibrators :

Multivibrators are broadly classified into three types, based upon their output states.

1. Bistable Multivibrators
2. Monostable Multivibrators and
3. Astable Multivibrators



Bistable Multivibrators.

There are only two possible states of a multivibrators are.

First state : Transistor Q_1 ON & Transistor Q_2 OFF.

Second state : Transistor Q_1 OFF & Transistor Q_2 ON.

Bistable Multivibrator has got two stable states.

Monostable Multivibrator has got only one stable state & other state being quasi stable state.

Astable Multivibrator has got no stable state. both the states being quasi stable states.

Stable state : The state in which the device can stay permanently. Only when a proper external triggering signal is applied, it will change its state.

Quasi stable state : It is a temporarily stable state.

After a predetermined time, the device will automatically come out of the quasi stable state.

In bistable ckts both the coupling elements are resistors. (Both are dc coupling).

In Monostable ckts One coupling element is a capacitor (ac coupling) & other coupling element is a resistor (dc coupling).

In Astable ckts both the coupling elements are capacitors. (Both are ac coupling).

Applications :

Bistable Multivibrator is the basic memory element. It is used to perform many digital operations such as counting & storing of binary data.

It also finds extensive applications in the generation and processing of pulse type waveforms.

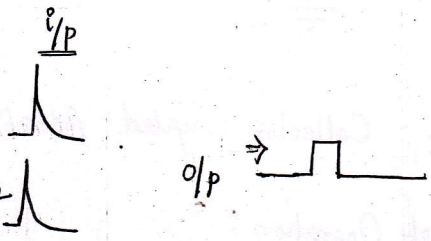
Monostable Multivibrator finds extensive applications in pulse ckts. It is used as a gating ckt or a delay ckt.

Astable Multivibrator is used as a master oscillator to generate square waves. It is often a basic source of fast waveforms.

Other Names :

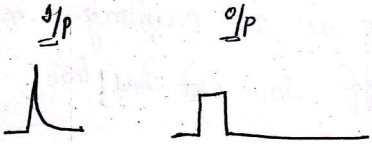
Bistable Multivibrator : (BMV)

- Binary's.
- Flip-flops
- Eccles-jordan ckt
- Trigger ckt
- Scale of two toggle ckt



Monostable Multivibrator : (MMV)

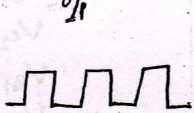
- Single shot / oneshot
- Single swing.
- delay ckt
- Univebrator
- Gating ckt.



Astable Multivibrator : (AMV)

- Free running.
- Square wave generator
- Synchronized Oscillator
- Relaxation Oscillator

i/p — None.



Astable Multivibrators :

Astable or free running multivibrator has two quasi-stable states & it keeps on switching b/w these two states, by itself. No external triggering signal is needed.

The two amplifier stages of an astable multi are regeneratively cross-coupled by two capacitors.

The output voltage of an astable multi is a square wave of period T. Since the multi generates square wave.

So Astable multi is also termed as Square wave generator or square wave oscillator or Relaxation oscillator or non sinusoidal oscillator.

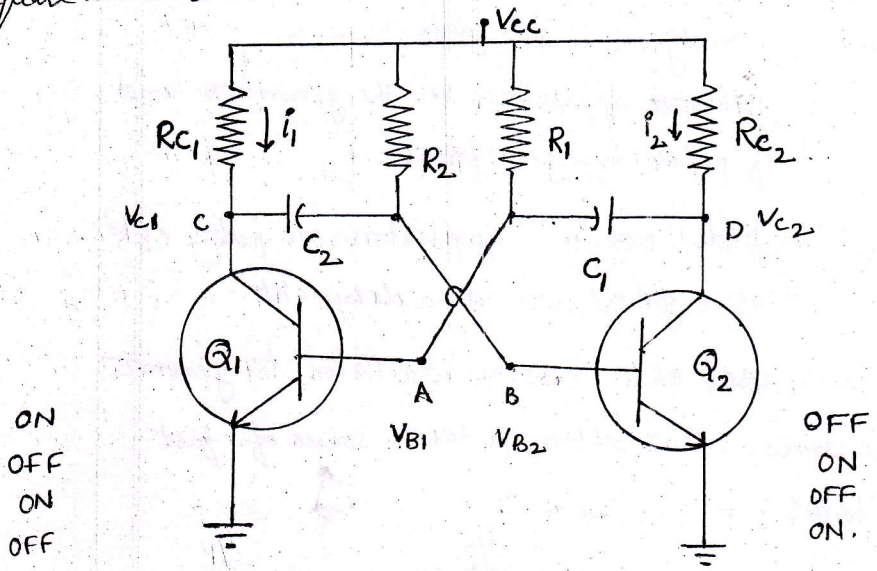


Fig: Collector Coupled Astable multivibrator.

Principle of Operation :

The collectors of both the transistors Q_1 & Q_2 are connected to the bases of the other transistors through the coupling capacitors C_1 & C_2. Since both are ac coupling, neither transistor can remain permanently at cut-off. So ckt has two quasi stable states.

Let us say at $t<0$, Q_2 was OFF & Q_1 was ON.

Hence for $t<0$, V_{B2} is negative.

$V_{C_2} = V_{CC}$

$V_{B1} = V_{BE(sat)}$

$V_{C_1} = V_{CE(sat)}$.

The capacitor C_2 charges through R_2 & V_{B_2} rises exponentially towards V_{cc}.

At $t=0$, V_{B2} reaches the cut in voltage V_γ & Q_2 Conducts. As Q_2 conducts its collector voltage V_{C2} drops by $I_2 R_C = V_{cc} - V_{CE(sat)}$ It is transmitted to the base of Q_1 through the coupling capacitor C_1 & hence V_{B1} also falls by $I_2 R_C$. Q_1 goes to OFF state.

ie Q_1 is OFF, Q_2 is ON

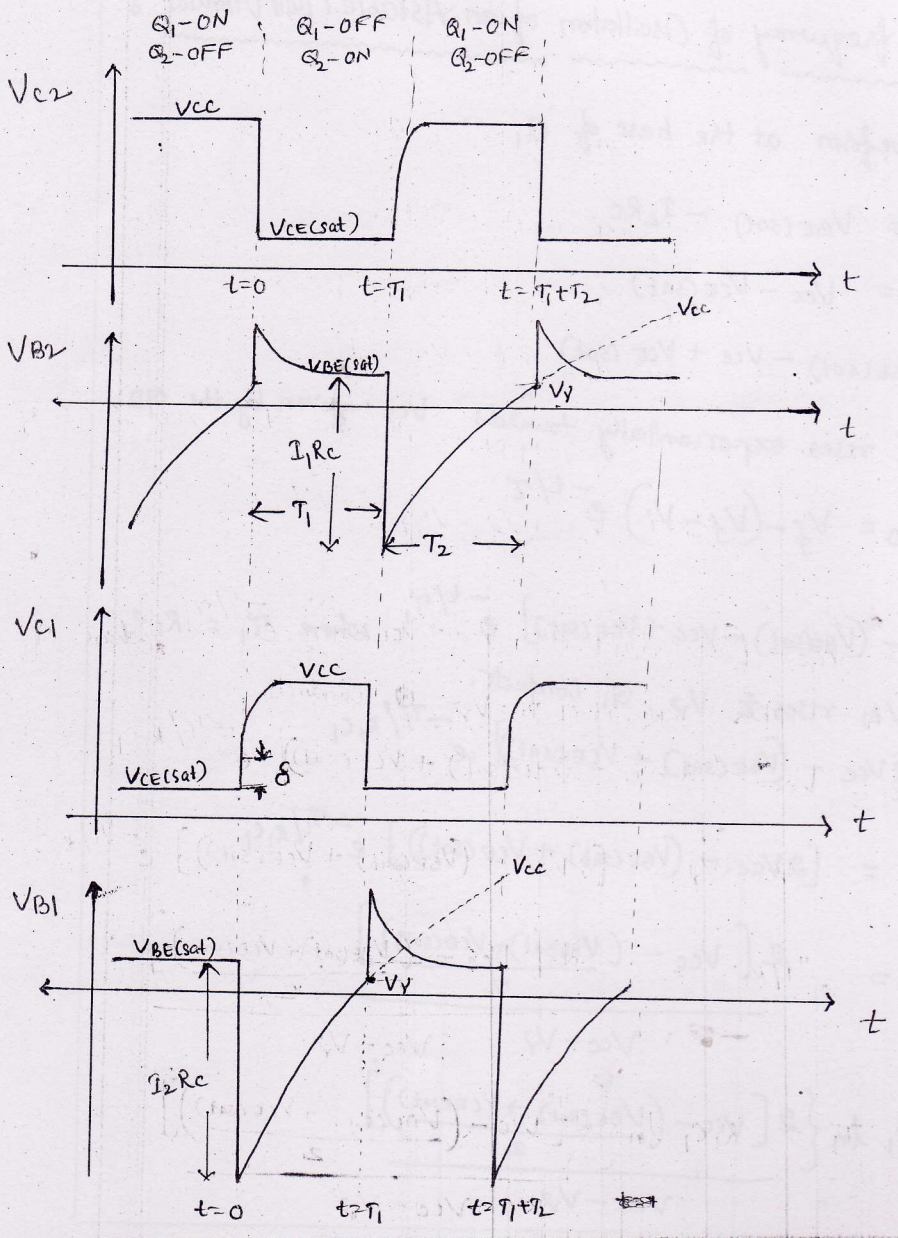
So,

$$V_{B_1} = V_{BE(sat)} - I_2 R_C.$$

$$V_{C_1} = V_{CC}$$

$$V_{C_2} = V_{CE(sat)}$$

V_{C1} is coupled through the coupling capacitor C_2 to the base of Q_2 causing an overshoot δ in V_{B_2}.



Now since Q_2 is ON, C_1 charges from V_{cc} through R_1 & hence V_{B1} rises exponentially.

At $t = T_1$ when V_{B1} rises to V_γ, Q_1 conducts and due to regenerative action Q_1 goes into saturation and Q_2 to cut off.

For $t > T_1$ the coupling capacitor C_2 charges from V_{cc} through R_2 &

At $t = T_1 + T_2$ when V_{B2} rises to the cut-in voltage V_γ, Q_2 conducts & due to regenerative feedback Q_2 goes to ON & Q_1 to OFF state.

∴ The cycle of events repeats and the ckt keeps on oscillating b/w its two quasi stable states.

Hence the output is a square wave. It is called a square wave generator & square wave oscillator & Relaxation Oscillator, so it is a free running Oscillator.

Expression for the frequency of Oscillation of an Astable Multivibrator

Consider the waveform at the base of Q_1

At $t = 0$. $\quad V_{B1} = V_{BE(sat)} - I_2 R_C$.

but $\quad I_2 R_C = V_{cc} - V_{CE(sat)}$.

$\therefore \quad V_{B1} = V_{BE(sat)} - V_{cc} + V_{CE(sat)}$.

For $0 < t < T_1$ V_{B1} rises exponentially towards V_{cc} given by the eqn.

$$V_0 = V_f - (V_f - V_i)\, e^{-t/\tau}.$$

$$\therefore V_{B1} = V_{cc} - [V_{cc} - (V_{BE(sat)} - V_{cc} + V_{CE(sat)}]\, e^{-t/\tau_1} \quad \text{where } \tau_1 = R_1 C_1.$$

∴ At $t = T_1$, when V_{B1} rises to V_γ, Q_1 conducts.

$$V_\gamma = V_{B1} = V_{cc} - [2V_{cc} - (V_{BE(sat)} + V_{CE(sat)})]\, e^{-T_1/R_1C_1}.$$

$$\Rightarrow \quad V_{cc} - V_\gamma = [2V_{cc} - (V_{BE(sat)} + V_{CE(sat)})]\, e^{-T_1/R_1C_1}$$

$$\Rightarrow \quad e^{T_1/R_1C_1} = \frac{2\left[V_{cc} - \left(\frac{V_{BE(sat)} + V_{CE(sat)}}{2}\right)\right]}{V_{cc} - V_\gamma}$$

$$\Rightarrow \quad T_1 = R_1 C_1 \ln\left\{\frac{2\left[V_{cc} - \left(\frac{V_{BE(sat)} + V_{CE(sat)}}{2}\right)\right]}{V_{cc} - V_\gamma}\right\}.$$

$$\Rightarrow \quad T_1 = R_1 C_1 \cdot \ln 2 + R_1 C_1 \ln \left[\frac{V_{CC} - \left(V_{BE(sat)} + V_{CE(sat)}\right)/2}{V_{CC} - V_\gamma} \right]$$

At room temperature for a transistor

$$V_\gamma = \frac{V_{BE(sat)} + V_{BE(sat)}}{2}$$

$$\therefore \quad T_1 = R_1 C_1 \ln 2$$

$$\Rightarrow \boxed{T_1 = 0.693 R_1 C_1}$$

Similarly we can show that the time T_2 for which Q_2 is OFF & Q_1 is ON is given by.

$$T_2 = R_2 C_2 \ln 2$$

$$\therefore \boxed{T_2 = 0.693 R_2 C_2}$$

∴ The period of the waveform $T = T_1 + T_2$

$$\therefore \boxed{T = 0.693 (R_1 C_1 + R_2 C_2)}$$

The frequency of Oscillations

$$\boxed{f = 1/T = \frac{1}{0.693 (R_1 C_1 + R_2 C_2)}}$$

If $R_1 = R_2 = R$ and $C_1 = C_2 = C$ then $T_1 = T_2 = T/2$

So, $T = 2 \times 0.693 RC$

$$\therefore \boxed{T = 1.386 RC}$$

and $$\boxed{f = \frac{1}{1.386 RC}}$$

∴ Pulse Width of the Astable multivibrator is

$T = 0.693 (R_1 C_1 + R_2 C_2)$ for unsymmetry

$T = 1.386 RC$ for symmetry.

Monostable Multivibrator :

→ The monostable multivibrator has one permanently stable state and one quasi-stable state.

→ A triggering signal is required to induce a transition from the stable state to the quasi stable state.

→ The ckt remains in its quasi stable state for a time equal to RC time constant of the ckt.

It returns from the quasi-stable state to its Original state as stable state by itself without any external triggering pulse after a time 'T' is called as One-shot, a single cycle, a single step ckt or a univibrator.

→ It generates a Rectangular waveform which can be used to gate other ckts. So it is also called a Gating ckt.

→ It generates a fast transition at a predetermined time T after the input trigger. So it is also referred as a delay ckt.

→ The two amplifier stages of a monostable multi are regeneratively cross coupled by one coupling element is capacitor and another coupling element is resistor.

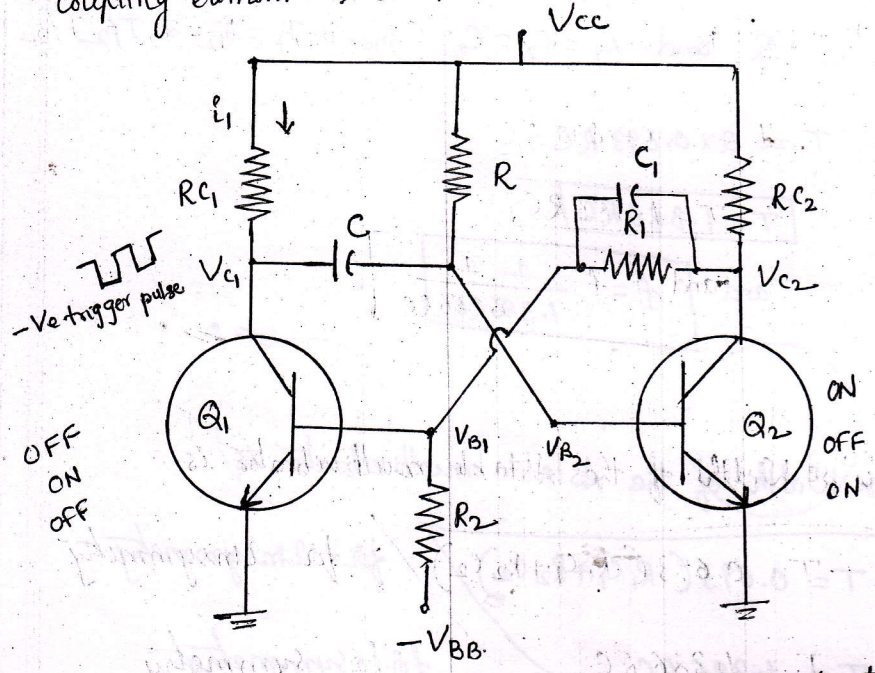


Fig: Collector Coupled Monostable Multivibrator.

Speed up capacitor or Transpose capacitor

Where C_1 Commutating capacitor

↑

To increase the speed of operation. (Transition time may be reduced)

Principle of Operation :

The base of Q_1 is connected to $-V_{BB}$ through a resistor R_2 to ensure that Q_1 is cut off. The base of Q_2 is connected to V_{CC} through R to ensure that Q_2 is ON.

Stable State :

For $t<0$ the monostable ckt is in stable state with Q_2-ON & Q_1-OFF

$$\therefore \quad V_{B_2} = V_{BE(sat)}$$

$$V_{C_2} = V_{CE(sat)}$$

$$V_{C_1} = V_{CC}.$$

The voltage at the base of Q_1 using the superposition theorem.

$$V_{B_1} = -V_{BB} \cdot \frac{R_1}{R_1+R_2} + V_{CE(sat)} \cdot \frac{R_2}{R_1+R_2}.$$

Quasi stable state :

A -Ve triggering s/l applied at $t=0$ brings Q_2 to OFF state & Q_1 to ON state. A current I_1 flows in R_C of Q_1.

So, the collector voltage of Q_1 drops suddenly by $I_1 R_C$ volts. Since the voltage across the coupling capacitor C cannot change, the voltage at the base of Q_2 also drops by $I_1 R_C$.

where $I_1 R_C = V_{CC} - V_{CE(sat)}$. Since Q_1 is ON.

$$V_{B_1} = V_{BE(sat)}$$

$$V_{C_1} = V_{CE(sat)}$$

$$V_{B_2} = V_{BE(sat)} - I_1 R_C.$$

$$V_{C_2} = V_{CC} \cdot \frac{R_1}{R_1+R_C} + V_{BE(sat)} \cdot \frac{R_C}{R_1+R_C}.$$

ie

In the time interval $0 < t < T$, the voltages V_{C_1}, V_{B_1}, V_{C_2} remain constant at their values at $t=0$, but the voltage at the base of Q_1 rises exponentially towards V_{CC} with time constant $\tau = RC$, until at $t=T$, V_{B_2} reaches the cut in voltage V_γ of the transistor.

for $t>T$, the reverse transition takes place i.e Q_2 conducts and Q_1 is cutoff.

ie The transition from the stable state to the quasi stable state takes place at $t=0$ & the reverse transition from the quasi stable state to the stable state at $t=T$.

" The time T for which the ckt is in its quasi stable state is referred as the Delay time or gate width or pulse width or pulse duration "

Expression for the Gate width T of a monostable multivibrator :

Consider the wave form at the base of Q_2 for the interval $0 < t < T$.

$$\therefore \quad V_0 = V_f - (V_f - V_{in})\, e^{-t/\tau}.$$

$$V_{B_2} = V_{cc} - \left(V_{cc} - (V_{BE(sat)} - I_1 R_c)\right) e^{-t/\tau}$$

But. $I_1 R_c = V_{cc} - V_{CE(sat)}$

$$\therefore V_{B_2} = V_{cc} - \left[V_{cc} - (V_{BE(sat)} - V_{cc} + V_{CE(sat)})\right] e^{-t/\tau}.$$

$$V_{B_2} = V_{cc} - \left[2V_{cc} - (V_{BE(sat)} + V_{CE(sat)})\right] \cdot e^{-t/\tau}.$$

At $t = T$, $V_{B_2} = V_\gamma$.

$$\Rightarrow \quad V_\gamma = V_{cc} - \left[2V_{cc} - (V_{CE(sat)} + V_{BE(sat)})\right] e^{-T/\tau}.$$

$$\Rightarrow \quad (V_{cc} - V_\gamma) e^{T/\tau} = 2V_{cc} - (V_{CE(sat)} + V_{BE(sat)})$$

$$\Rightarrow \quad e^{T/\tau} = \frac{2V_{cc} - [V_{CE(sat)} + V_{BE(sat)}]}{V_{cc} - V_\gamma}.$$

$$\Rightarrow \quad T/\tau = \frac{\ln 2\left[V_{cc} - \left(\frac{V_{CE(sat)} + V_{BE(sat)}}{2}\right)\right]}{V_{cc} - V_\gamma}.$$

$$\Rightarrow \quad T = \tau \ln 2 + \tau \ln \left[\frac{V_{cc} - \left(\frac{V_{CE(sat)} + V_{BE(sat)}}{2}\right)}{V_{cc} - V_\gamma}\right]$$

At room temperature

The cut in voltage is the average of saturation turn voltages.

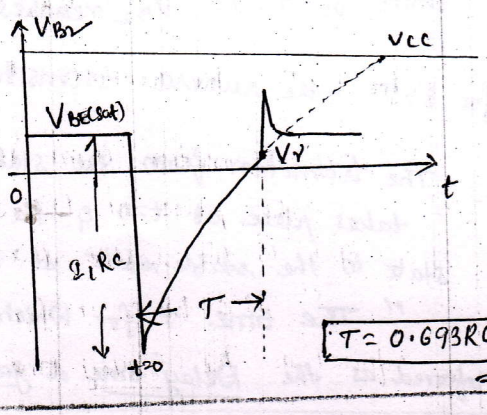
ie $V_\gamma = \frac{V_{CE(sat)} + V_{BE(sat)}}{2}$

$$\therefore \quad T = \tau \ln 2.$$

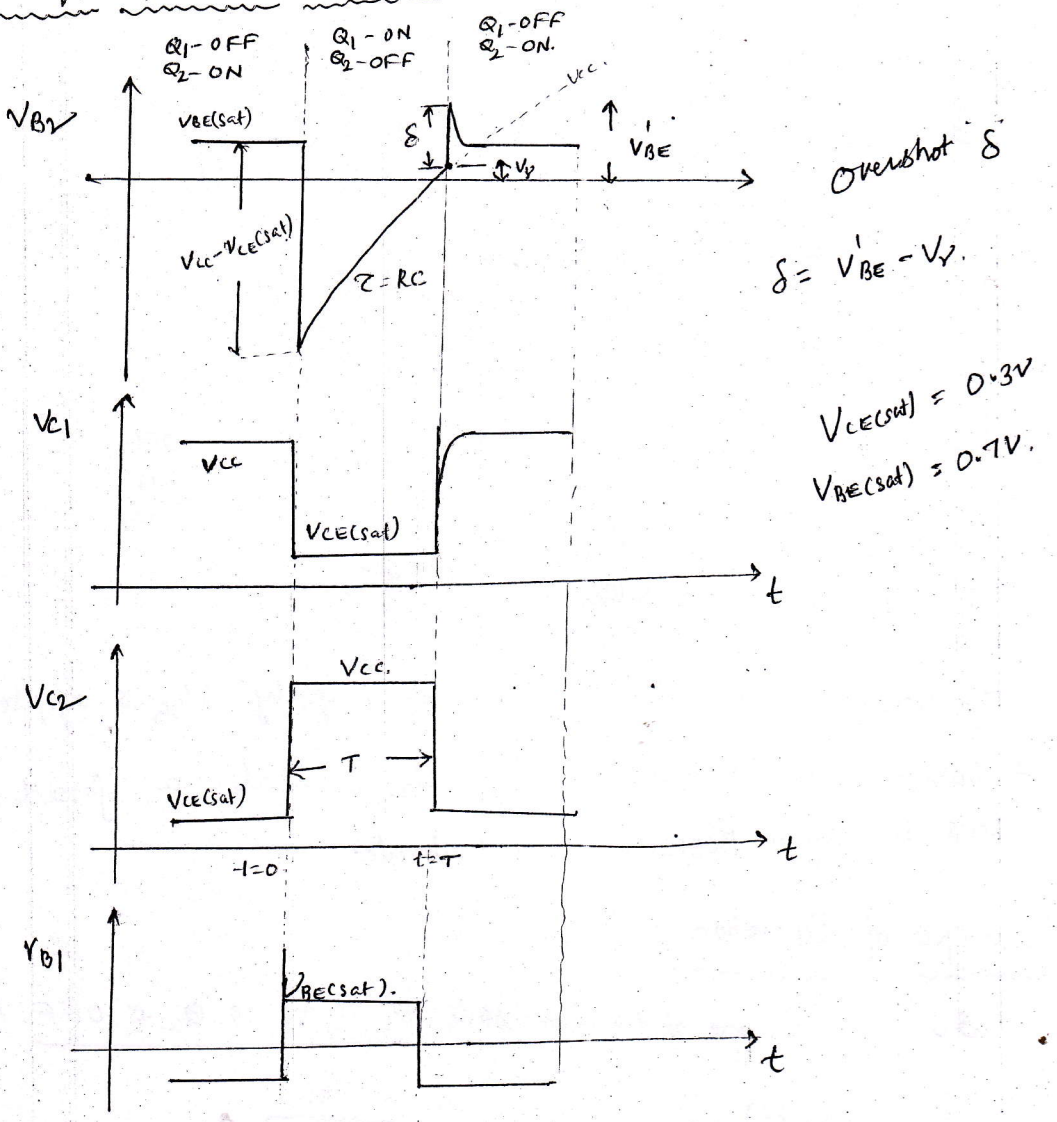
$$T = 0.693\, RC.$$

$$\therefore$$ **Gate width or Pulse width $T = 0.693\, RC$.**

The delay time may be varied by varying the time constant ($\tau = RC$).



Waveforms of Monostable Multivibrator :-



Overshot δ

$\delta = V'_{BE} - V_\gamma$.

$V_{CE(sat)} = 0.3V$

$V_{BE(sat)} = 0.7V$.

Bistable Multivibrator :

* A bistable multivibrator is the basic memory element. It is used to perform many digital operations such as counting & storing of binary data.

→ The Bistable multivibrator is also called a binary or Eccles jordan ckt & trigger ckt & scale of two toggle ckt, flipflop.

→ In Binary coupling elements both are resistors (dc coupling)

→ It has two stable states, doesn't contain quasi stable state.

→ Here transition performed from one state to the other state by means of external triggering signals.

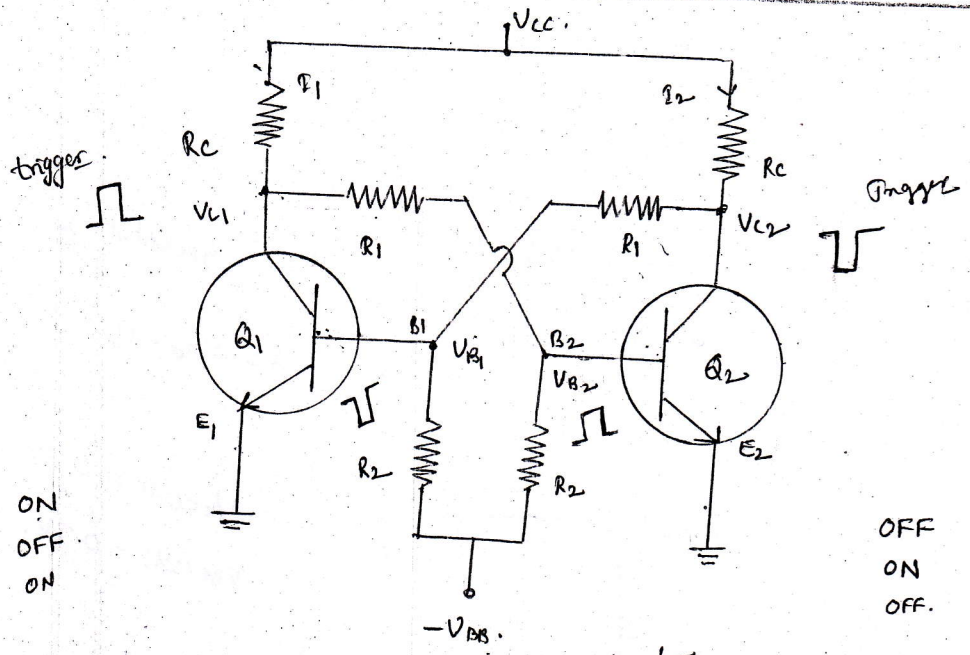


Fig: Fixed bias bistable Multivibrator.

→ The binary in which the external supply V_{BB} is applied to base bias transistor Q_1 and Q_2 is called a fixed bias binary a Bistable multivibrator.

Principle of Operation:

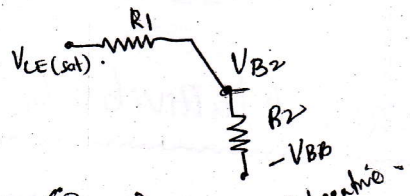
Suppose in one of the stable state Q_1 is ON & Q_2 is OFF. H

$\therefore$ $V_{C1} = V_{CE(sat)}$

$V_{B1} = V_{BE(sat)}$.

$V_{C2} = V_{CC}$

$$V_{B2} = -V_{BB}\cdot\left(\frac{R_1}{R_1+R_2}\right) + V_{CE(sat)}\left(\frac{R_2}{R_1+R_2}\right)$$



The multivibrator can be driven from the first stable state to the other stable state by applying either a negative trigger to the base of Q_1 & positive trigger pulse to the base of Q_2 transistor.

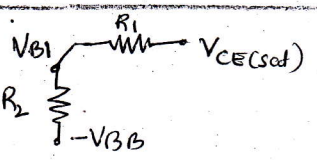
A -ve triggering S/L is applied at base of Q_1 & at the collector of Q_2. The transistor Q_1 goes to Cutoff. As Q_1 OFF Collector voltage of Q_1 is transmitted to the base of Q_2 through R_1 then transistor Q_2 goes to saturation i.e Q_2-ON.

$V_{C1} = V_{CC}$

$V_{C2} = V_{CE(sat)}$.

$V_{B2} = V_{BE(sat)}$

$V_{B1} = -V_{BB} \cdot \frac{R_1}{R_1+R_2} + V_{CE(sat)} \frac{R_2}{R_1+R_2}$ (negative).

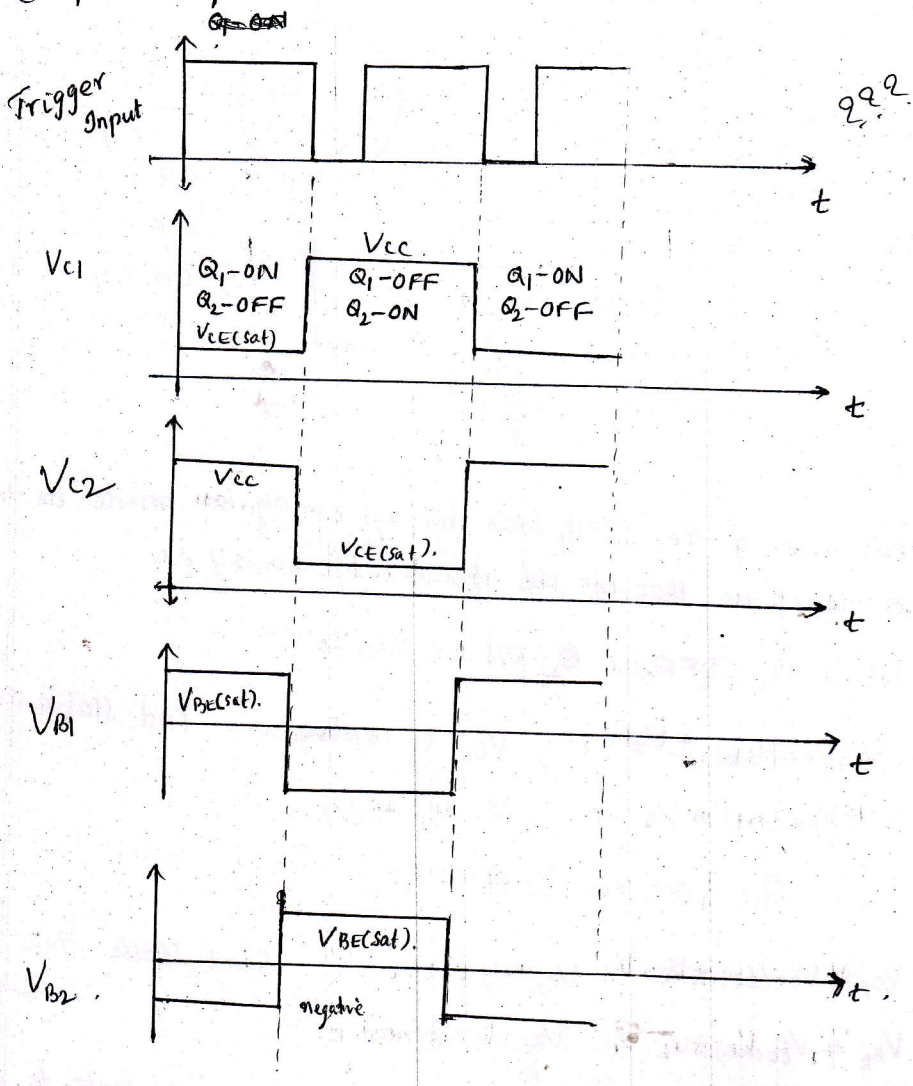


The ckt will now remain in this second stable state ie Q_1 - OFF, Q_2 - ON. Until a positive pulse is applied to the base of transistor Q_1 & a negative pulse to the base of transistor Q_2.

A +Ve trigger s/l is applied at the base of Q_2 & at the collector of Q_1. the Transistors Q_1 goes to Saturation & Q_2 goes to Cutoff.

Hence the transistors goes to its original states by External Signalling inputs.

Output Waveforms :

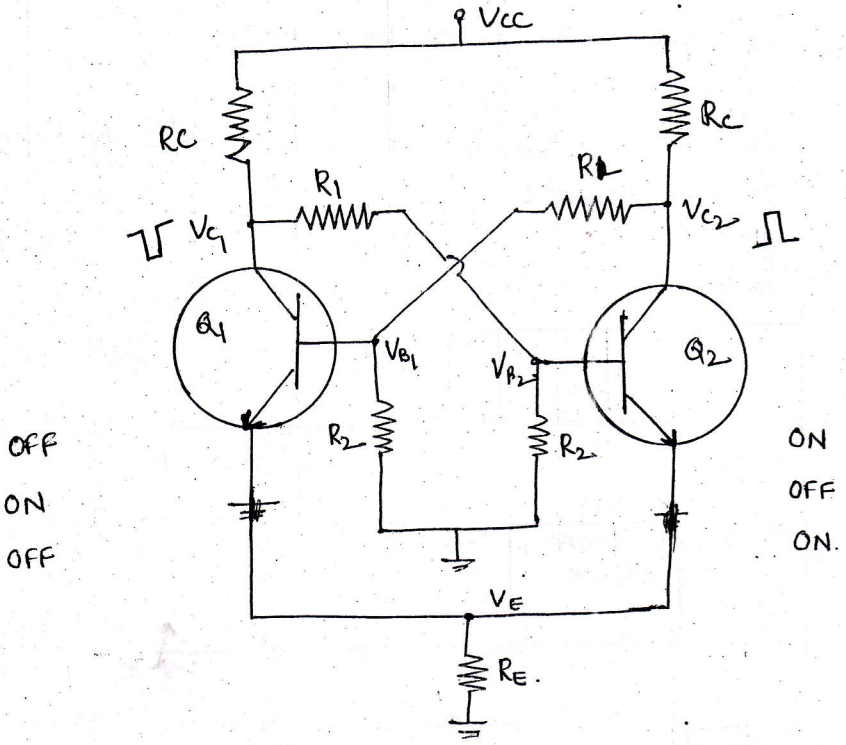


Self Biased bistable Multivibrator:

→ A fixed biased bistable multivibrator requires two power supplies one positive ie V_{CC} & One negative ie $-V_{BB}$.

→ The need for the negative power supply may be eliminated by using a common emitter resistor R_E.

→ The binary using the common emitter resistor R_E to provide self bias is called the self biased bistable multivibrator.



The analysis of the self bias binary may be made on the same lines as that of the fixed bias binary.

let Q_1 - OFF, Q_2 - ON. then.

$V_{C_2} = V_{CE(sat)} + V_E$ V_{B_1} is negative. first stable state.

$V_{B_2} = V_{BE(sat)} + V_E$. $V_{C_1} = V_{CC}$.

Q_1 - ON. Q_2 - OFF.

$V_{C_1} = V_{CE(sat)} + V_E$ $V_{C_2} = V_{CC}$ Second stable state.

$V_{B_2} = V_{BE(sat)} + V_E$. V_{B_2} is negative.

∴ The multivibrator can be driven from the first stable state to the other stable state by applying external triggering signals.

Commutating Capacitors :

→ In order to increase the switching speed of multivibrators, to shunt the coupling resistors R_1, R_1 by suitable capacitors (C_1 & C_2). These capacitors are called as commutating capacitors & also termed as speed up capacitors & transpose capacitors.

→ The main feature of the commutating capacitors is that they reduce the transition time and increase the switching speed. Hence the name speed-up capacitors.

→ The smallest allowable interval b/w two successive triggers is termed as the resolving time of the flip-flop.

→ The reciprocal of the resolving time represents the max. frequency at which the binary can respond.

$$C_1 = C_2 = \frac{1}{2.3\, f_{max}\,(R_1 // R_2)}$$

but $R_1 // R_2 = \frac{R_1 R_2}{R_1 + R_2}$

$$\therefore \boxed{C_1 = C_2 = \frac{R_1 + R_2}{2.3\, R_1 R_2\, f_{max}}}$$

$$f_{max} = \frac{1}{2\tau} = \frac{1}{2 \cdot \frac{R_1 R_2}{R_1 + R_2} C_1}$$

$$f_{max} = \frac{R_1 + R_2}{2 R_1 R_2 C_1}$$

$$\text{or } \boxed{C_1 = C_2 = \frac{R_1 + R_2}{2 \cdot R_1 R_2\, f_{max}}}$$

→ The time required for the purpose of completing the recharging of capacitors after the transfer of conduction is called the settling time.

→ The sum of the transition time (t_t) and the settling time (t_s) is called the resolution time.

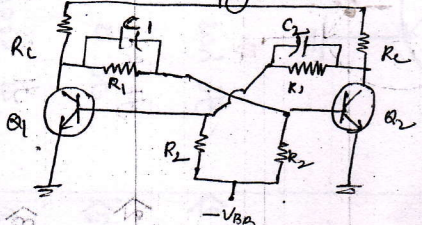
If commutating capacitors are too small, t_t is ↑ but t_s will be small.

If commutating capacitors are too large, t_t is ↓ but t_s will be large.

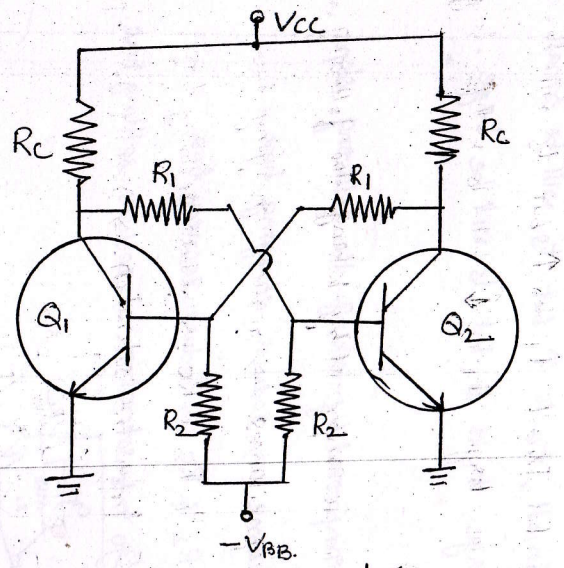
Methods of Improving Resolution :

The Resolution of a binary can be improved by taking the following steps.

1. By reducing all stray capacitances. → Reduces charging time.
2. By reducing the resistors R_1, R_2 & R_C → Reduces recovery time
3. By not allowing the transistors to go into saturation. → reduces settling time.



Bistable Multivibrator

1) 

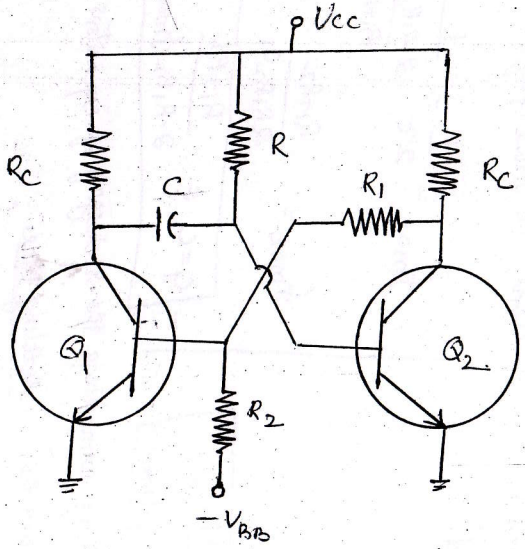
2) It has two stable states.

3) It is a flip flop.

4) It requires triggering pulse for every transition.

5) It is also called as binary or Eccles jordan ckt or trigger ckt.

Monastable Multivibrator

1) 

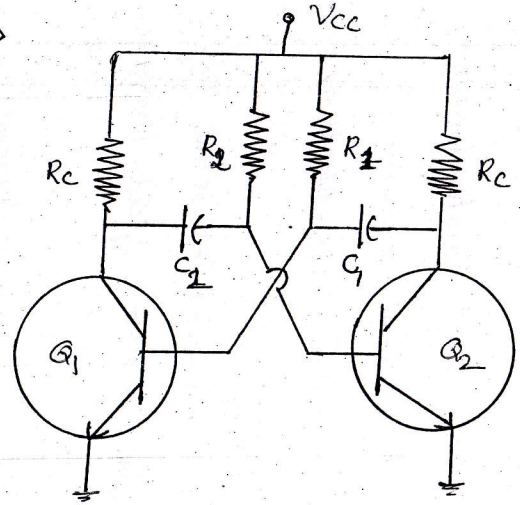
2) It has one stable state and one quasi stable state.

3) It is a pulse generator

4) It requires only one triggering pulse to change the state temporarily and it returns back to its original state.

5) It is also called as one shot or delay ckt & gating ckt & single swing & univibrator.

Astable Multivibrator

1) 

2) It has two quasi stable states.

3) It is a square wave generator

4) It does not require the triggering pulse. It is a free running multivibrator.

5) It is also called as free running multivibrator or Synchronized oscillator & Relaxation oscillator.

6) Positive & Negative pulses are of equal widths.

Applications.

7) It is a discrete component one bit memory element which can be used in shift registers, counters etc.

8) It can be used as a frequency divider (as a divide by two counter).

9) It is used to generate square waves of symmetrical shape by sending regular triggering pulse to the input. By adjusting the frequency of the input trigger pulses, the width of the square wave can be altered.

10) It has both coupling elements are resistors (dc coupling).

=.

6) Pulse width or gate width

$T_p = 0.69RC$.

Applications:

7) It is used as a time delay unit since it produces a transition at a fixed time after the trigger signal.

8) It is used to function as an adjustable pulse width generator.

9) It is used to generate uniform width pulses from a variable width into pulse train and generate clean and sharp pulses from the distorted pulses.

10) It has one coupling element capacitor (ac coupling) & one coupling element resistor (dc coupling).

=.

6) Pulse width or gate width

$T_p = 0.69 (R_1C_1 + R_2C_2)$.

If $R_1 = R_2 = R$ & $C_1 = C_2 = C$ then

$T_p = 0.69 \times 2RC = 1.38RC$.

7) Applications

It is operated as an oscillator over a wide range of audio & radio frequencies.

8) It is used in construction of digital voltmeter and SMPS.

9) It is used as square wave generator, voltage to frequency converter & in pulse synchronization, as a clock for binary logic signals. etc.

10) It has two coupling elements both are capacitors (ac coupling).

=.

Triggering of Bistable Multivibrator:

We know a binary or flip-flop has two stable states.

The process of bringing about a change of state of the binary by applying an external pulse is termed as triggering.

When a trigger pulse is applied the short duration of time when conduction transfers from one transistor to the other is termed as transition time.

Usually a negative pulses of short duration is applied suitably to the collector of the OFF transistor to cause triggering.

Types of Triggering:

Triggering of multis of two types.

1. Unsymmetrical / Asymmetrical triggering / set-reset triggering.
2. Symmetrical triggering.

Unsymmetrical Triggering:

Two triggering pulses from two seperate sources are needed to change the states of the binary.

Asymmetrical Triggering:

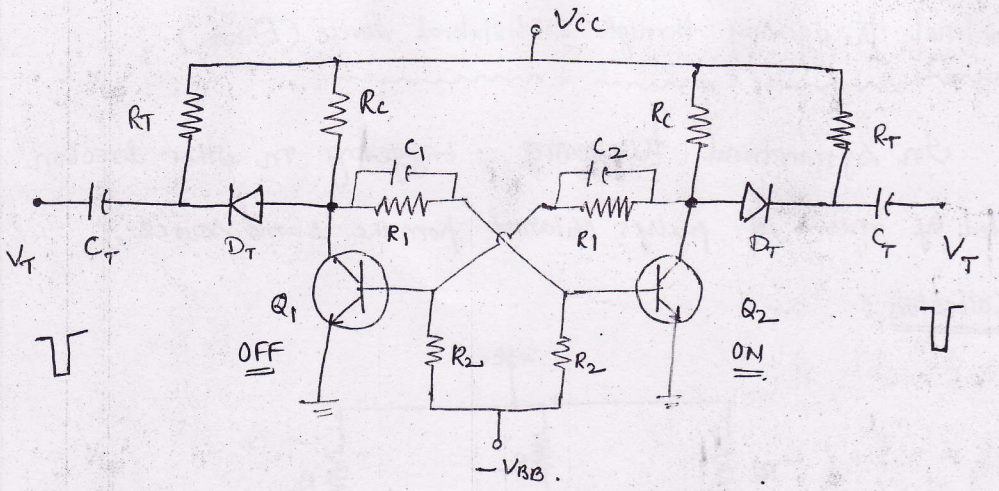
Only one triggering pulse is needed to bring about change of the state. Transition from ON to OFF & OFF to ON, a single source triggering can be effected in both directions.

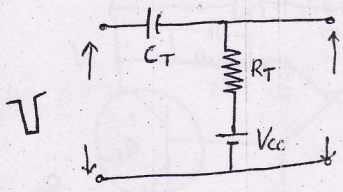
i.e. It should be noted that only bistable & monostable multis require triggering. There is no need of triggering of astable multivibrator.

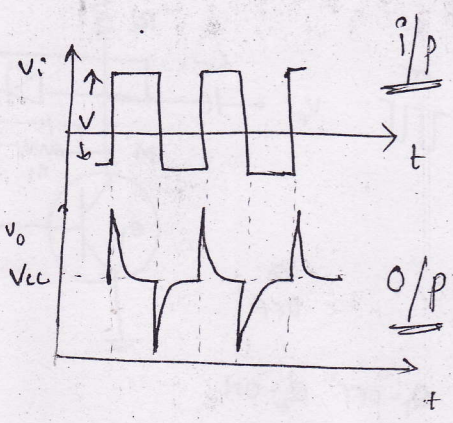
Unsymmetrical triggering through a Unilateral device (Diode):

At Collectors: Consider a fixed bias binary along with the triggering ckt comprising of R_T, Capacitor C_T & diode D_T, C_1 & C_2 are commutating capacitors.

R_T & C_T together constitute a differentiator ckt. When a pulse is applied as input, the output is in the form of spikes as +ve & −ve wrt Vcc.





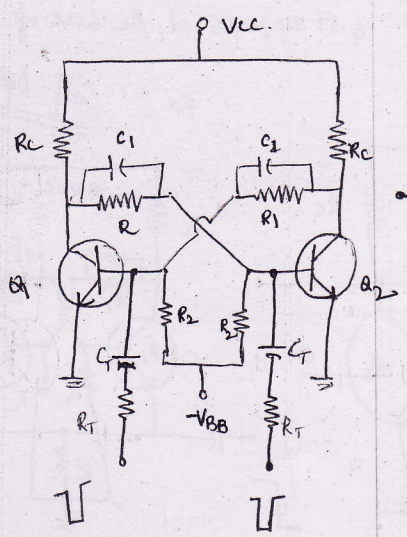


It seen that diode D_T can transmit only negative spikes. It is appearing at collector of Q_1 (which is OFF) transmitted through C_1 appears at the base of ON transistor Q_2.

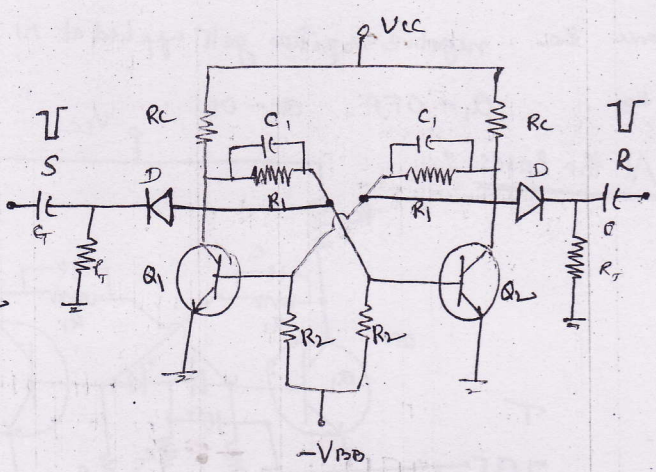
ie Q_2 - becomes OFF Q_1 becomes ON.

In order to restore the binary to the original state ie Q_1 - OFF, Q_2 - ON. Similar triggering is provided at the collector of Q_2.

At Bases: Asymmetrical binary triggering requires two triggering pulses from two seperate sources.



(without diode)

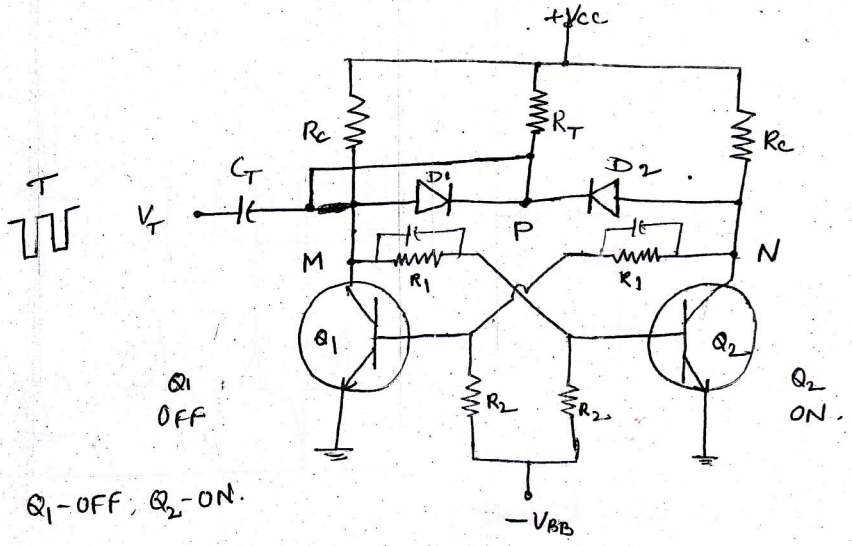


(with diode)

Symmetrical triggering through a Unilateral device (Diode) :

In symmetrical triggering, triggering in either direction is effected by means of pulses obtained from the same source.

At the Collectors :



let Q_1 - OFF, Q_2 - ON.

Since Q_2 is ON ie in saturation $V_N = V_{CE(sat)} \cong 0$. Hence the supply voltage Vcc is +Ve & reverse biases the diode D_2.

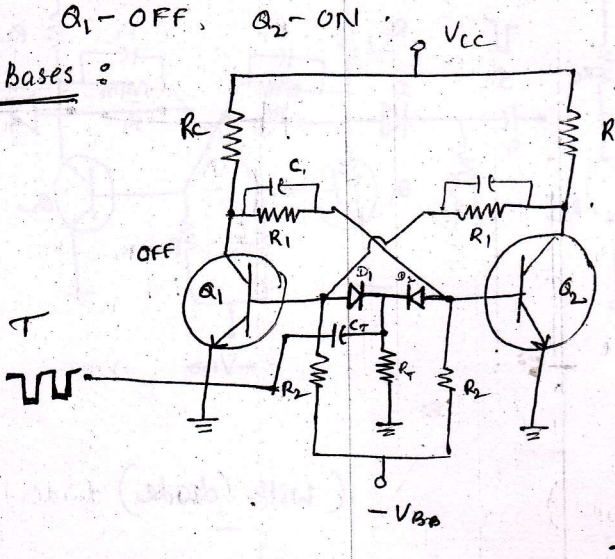
When a -Ve triggering pulse appears at P diode D_1 gets forward biased and readily conducts. Hence the -Ve spike gets applied at M. It is Txed through capacitor C_1 & it appears at the base of Q_2 then.

Q_2 - OFF & Q_1 - ON.

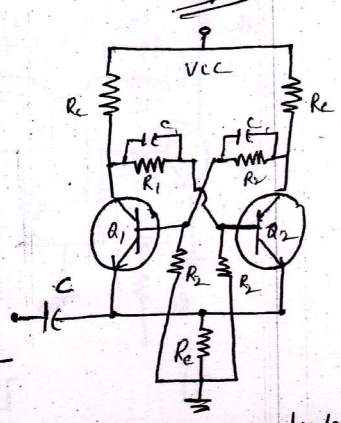
Since Q_1 - ON, Q_2 - OFF. $V_M = V_{CE(sat)} = 0$. D_1 becomes reverse biased.

When the next -Ve spike appears at P then D_2 - ON & conducts. Hence the negative spike gets applied at N & it appears at the base of Q_1 then. Q_1 - OFF, Q_2 - ON.

At the Bases :



For a Self Biased Binary



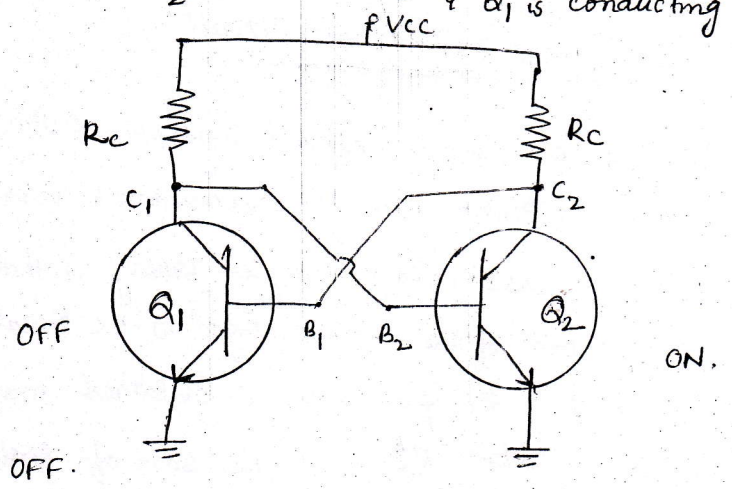
∴ Without steering diodes +Ve step is applied at common emitters of the flipflop.

A Direct Connected Binary :

No coupling elements are used and the collector of each transistor is connected to the base of the other transistor directly by a wire.

It is also called DCTL. Direct Coupled Transistor Logic.

In one state transistor Q_1 is in saturation & Q_2 is conducting slightly. & in the other state Q_2 is in saturation & Q_1 is conducting slightly.



let Q_1 is OFF.

Transistor Q_2 - Emitter is grounded & Collector, Base are connected to Vcc through resistor Rc.

∴ The currents of Q_2.

$$I_{B_2} = \frac{V_{cc} - V_{BE_2}}{R_c} \quad \& \quad I_{c_2} = \frac{V_{cc} - V_{CE_2}}{R_c}.$$

V_{BE_2} & V_{CE_2} are small compared with V_{cc}.

$$\therefore \boxed{I_{B_2} \approx \frac{V_{cc}}{R_c} \approx I_{c_2}}$$

If $I_{B_2} >> \frac{I_{c_2}}{h_{fe}}$, then Q_2 is said to be indeed driven into Saturation.

$V_{BE_1} = V_{CE_2} = 0.05V$ ≤ a small +Ve value. So Q_1 is not OFF & it will be conducting slightly. So this ckt is not used these days.

Advantages :

1. Extremely simple ckt.
2. Low power dissipation
3. Transistors with low breakdown voltages may be used.
4. Only one supply voltage of low value about 1.5V is required
5. Easily constructed as an IC because of few elements (resistors & transistors).

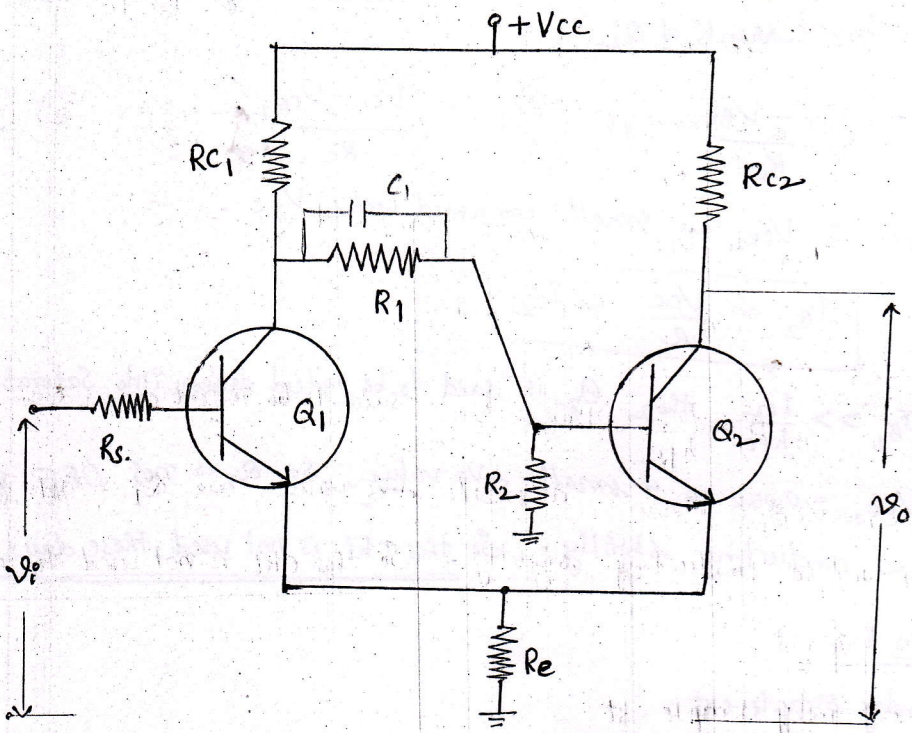
Disadvantages:

1. Since Q_2 is driven heavily into saturation, the storage time delay will be large & the switching speed will be long.
2. The o/p voltages are equal to the saturation base & collector voltages from transistor to transistor.
3. Since an OFF collector is tied directly to an ON base, it is difficult to trigger the binary by the usual method of applying a pulse to the OFF transistor.

The Emitter Coupled Binary (or) The Schmitt Trigger Circuit

→ Schmitt trigger is a Emitter coupled Bistable Multivibrator. It is named after his inventor of its vacuum tube version.

→ It differs from the basic collector-coupled binary in that the coupling from the output of the second stage to the input of the first stage is missing & the feedback is obtained now through a common emitter resistor R_e. & the base of first transistor is connected to a voltage source. v_i.



The output of a Schmitt trigger is a square wave, whatever the wave-form of the input signal.

For n-p-n transistor	$V_\gamma = 0.5V$	$V_\gamma = .0.1V$	Ge.
For p-n-p transistor	$V_{BE(sat)} = 0.7V$	$V_{BE(act)} = 0.2V$	
All are -Ve.	$V_{BE(act)} = 0.6V$	$V_{BE(sat)} = 0.3V$	

Si

Principle of Operation :

Let the i/p to the transistor Q_1 be a sinusoidal voltage.

$$V_i = V_m \sin \omega t$$

when $v_i = 0$ & not present. Q_1 - OFF

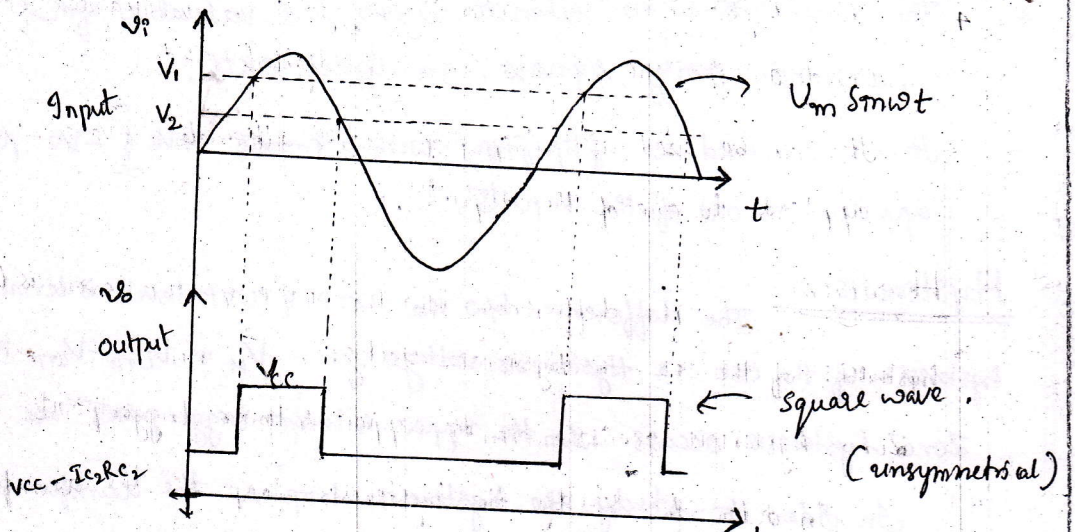
However base of Q_2 drive from the supply voltage V_{cc} & hence it conducts, but it would be conducting in the active region.

∴ Q_1 - OFF, Q_2 - ON → Normal state of schmitt Trigger.

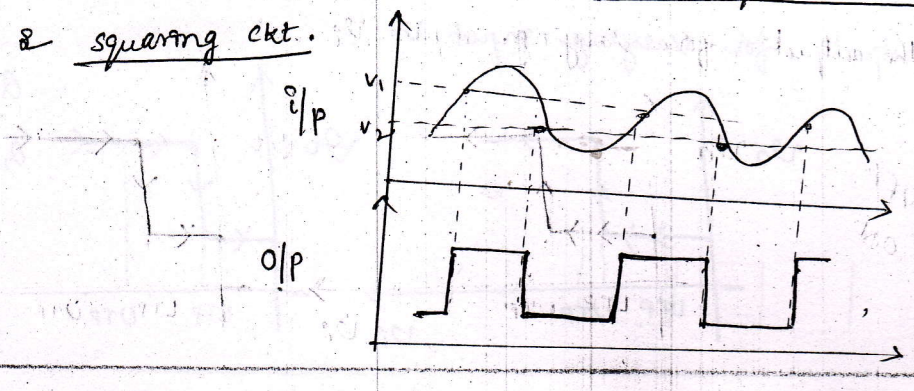
If an i/p V_i of sufficient amplitude is applied at the base of Q_1. then Q_1 - ON. When Q_1 turns ON its collector voltage V_{c_1} falls causing a fall in the voltage applied to the base of Q_2 - Q_2 - OFF & its collector voltage rises to V_{cc}.

∴ Since when V_i is increasing V_o also increses. So the output and input in a schmitt trigger are always in phase.

If V_i is decreased & removed so no current flows into the base of Q_1 then Q_1 - OFF & Q_2 - ON. The ckt has now returned to its normal state.



Thus. The schmitt trigger termed as Sine to Square converter & squaring ckt.



Let V_1 = Upper triggering voltage (V_{UTP}).

ie The value of the input voltage V_i which makes Q_1 conduct is termed as Upper trigger point or Upper trip point.

V_2 = Lower triggering voltage (V_{LTP})

ie The value of the input voltage V_i which makes again Q_2 conduct is termed as Lower trigger point or Lower trip point.

V_H = Hysteresis voltage, $V_H = V_{UTP} - V_{LTP}$

UTP: A point at which Q_1 starts conducting is called Upper trigger point.
LTP: A point at which Q_2 starts conducting is called Lower Trigger point.

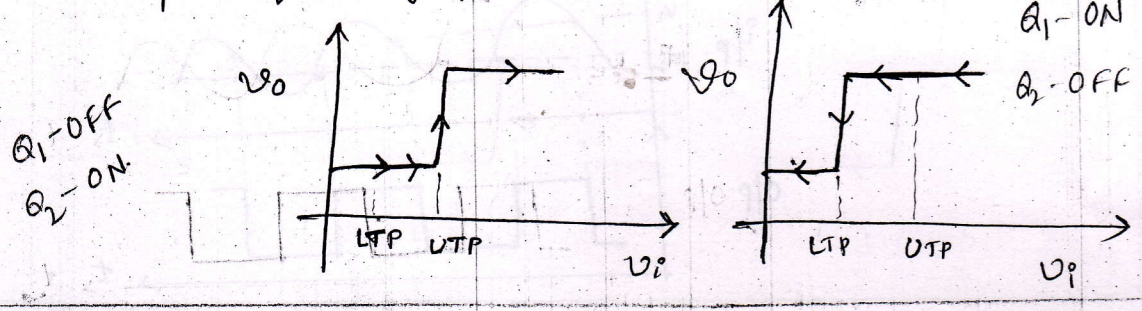
Applications of Schmitt Trigger:

1. It can be used as an amplitude / voltage comparator.
2. It is used for generation of a rectangular waveform ie unsymmetrical square wave from sine wave or any other form.
3. It is used for wave shaping ckts.
4. The hysteresis in schmitt trigger is valuable for conditioning noisy signals, in digital ckts.
5. It can be used as flip-flop with alternate +Ve & -Ve pulses applied to one of the inputs.

Hysteresis: The difference b/w the UTP & LTP levels is termed as the hysteresis of the ckt & Hysteresis voltage. $V_H = V_{UTP} - V_{LTP} = V_1 - V_2$.

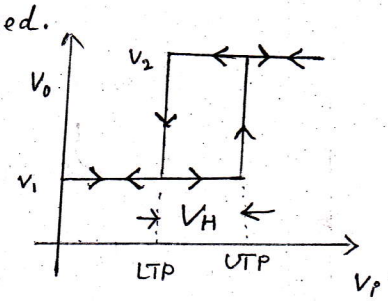
Zero hysteresis occurs when the upper & lower trigger points are equal.

In order to study the hysteresis loop or the transfer characteristics of the schmitt trigger. It is necessary to obtain values of v_o the output, for varying input v_i.



The curves shown in above may be clubbed together and the total transfer characteristics can be plotted.

The closed loop shows the hysteresis loop.



$$V_H = V_1 - V_2 = UTP - LTP$$

$$= .$$

Hysteresis: The lagging of the lower threshold voltage from the upper threshold voltage is known as the Hysteresis.

Expressions for UTP & LTP:

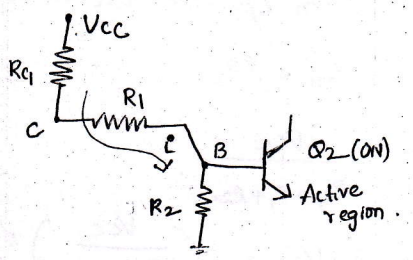
V_1 (UTP):

$$V_1 = V_\gamma + V_{E2}$$

Q_1 - OFF
Q_2 - ON

$$\Rightarrow \boxed{V_1 = V_\gamma + i_{C_2} R_e}$$

To evaluate i_{C_2}.



Thevinin equavalent ckt at 'B'

$$V_{TH} = iR_2$$

$$i = \frac{Vcc}{R_{C_1} + R_1 + R_2}$$

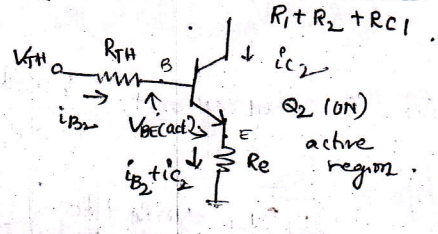
$$\Rightarrow V_{TH} = \left(\frac{Vcc}{R_{C_1} + R_1 + R_2}\right) R_2$$

$$R_{TH} = R_2 // (R_{C_1} + R_1)$$

$$\therefore R_{TH} = \frac{R_2 (R_1 + R_{C_1})}{R_1 + R_2 + R_{C_1}}$$

Applying KVL to the loop

$$V_{TH} = i_{B_2} R_{TH} + V_{BE(act)} + (i_{B_2} + i_{C_2}) R_e$$



We know on the active region.

$$h_{fe} = \frac{i_{C_2}}{i_{B_2}} \Rightarrow i_{C_2} = h_{fe}\, i_{B_2}.$$

$$\therefore V_{TH} = i_{B_2} R_{TH} + V_{BE(act)} + i_{B_2} (1 + h_{fe}) R_e$$

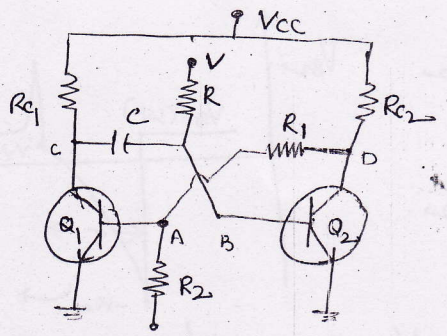
$$\therefore i_{B_2} = \frac{V_{TH} - V_{BE(act)}}{R_{TH} + R_e (1 + h_{fe})}$$

$$i_{C_2} = h_{fe} \cdot i_{B_2}.$$

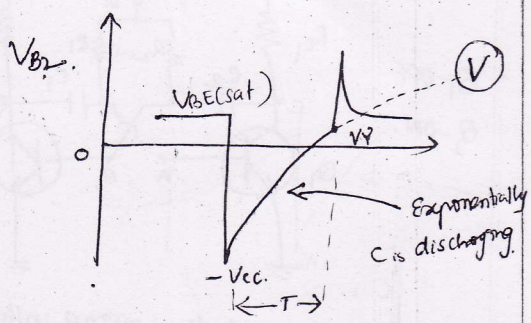
$$\therefore \boxed{V_1 (UTP) = V_\gamma + h_{fe} \cdot i_{B_2} \cdot R_e}$$

$$\therefore \boxed{V_1 (UTP) = V_\gamma + h_{fe} \cdot R_e \left(\frac{V_{TH} - V_{BE(act)}}{R_{TH} + R_e (1 + h_{fe})}\right)}$$

Monostable Multi as Voltage to Time Converter :



Q_1-OFF
Q_2-ON.



∴ The mathematical expression for the exponentially rising voltage V_{B_2} is

$$V_{B_2} = V_f - (V_f - V_{in}) e^{-t/RC}$$

$V_{initial\ of\ B_2} = -V_{cc}$

$V_{final\ of\ B_2} = V$

$$\therefore V_{B_2} = V - [V - (-V_{cc})] e^{-t/RC}$$

$$\therefore V_{B_2} = V - [V + V_{cc}] e^{-t/RC}.$$

at $t = T$, $V_{B_2} = V_V \cong 0$.

$$0 = V - (V + V_{cc}) e^{-T/RC}$$

$$(V + V_{cc}) e^{-T/RC} = V$$

$$e^{T/RC} = V / V + V_{cc}$$

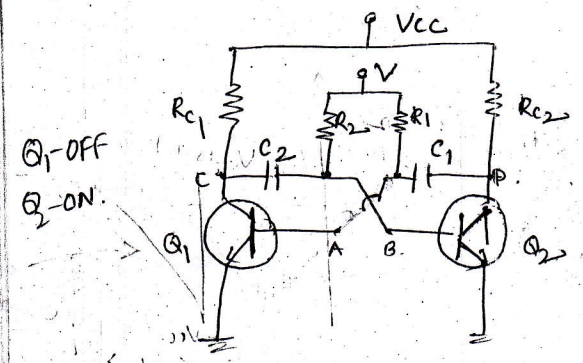
$$\Rightarrow e^{T/RC} = \frac{V + V_{cc}}{V}$$

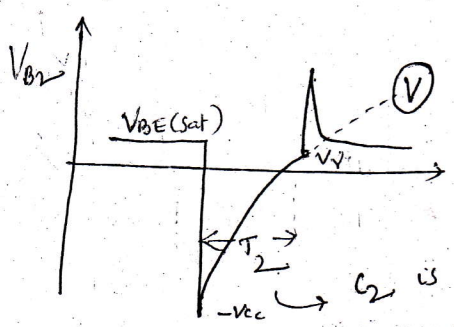
$$T/RC = \log_e \left(1 + \frac{V_{cc}}{V}\right)$$

$$\therefore \boxed{T = RC \log_e \left(1 + \frac{V_{cc}}{V}\right).}$$

V_{cc}, R & C being fixed, as V changes T also changes. Hence the pulse width is a function of the auxiliary voltage V so the monostable multivibrator is termed as Voltage to Time converter (V-T).

Astable multivibrator as Voltage to frequency Convertor :





The exponentially rising voltage V_{B_2} is expressed as

$$V_{B_2} = V_f - (V_f - V_{in})\, e^{-t/RC}$$

$R = R_2$
$C = C_2$.

Initial value of $V_{B_2} = V_{in} = -V_{cc}$

Final value of $V_{B_2} = V_f = V$

$$\therefore \quad V_{B_2} = V - (V + V_{cc})\, e^{-t/R_2C_2}$$

At $t = T_2$, $V_{B_2} = V_f \cong 0$.

$$0 = V - (V + V_{cc})\, e^{-T_2/R_2C_2}.$$

$$\Rightarrow (V + V_{cc})\, e^{-T_2/R_2C_2} = V$$

$$e^{T_2/R_2C_2} = \frac{V + V_{cc}}{V}$$

$$\Rightarrow T_2 = R_2C_2 \cdot \log_e\left(1 + \frac{V_{cc}}{V}\right).$$

Similarly,

$$T_1 = R_1C_1 \cdot \log_e\left(1 + \frac{V_{cc}}{V}\right).$$

$\therefore$ Time width a period $T = T_1 + T_2$.

$$\therefore \boxed{T = (R_1C_1 + R_2C_2)\log_e\left(1 + \frac{V_{cc}}{V}\right)}$$

(or)

$$T = 2RC \log\left(1 + \frac{V_{cc}}{V}\right) \quad \text{if} \quad R_1 = R_2 = R \;\&\; C_1 = C_2 = C.$$

frequency $f = 1/T$.

$$\therefore \boxed{f = \frac{1}{2RC \log\left(1 + \frac{V_{cc}}{V}\right)}}$$

Hence V varies, f also varies, i.e. Frequency is a function of voltage V. So the astable multi is referred to as voltage to frequency converter (V-f).

Unit- III

TIME BASE GENERATORS

* A time based generator is one that provides an output waveform (voltage or current), a portion of which varies linear with time.
* It may be voltage time based generator, current time based generator

Voltage time base generator

* It is one that provides an output voltage waveform, a portion of which exhibits a linear variation of voltage with respect to time

Current time base generator

* It is one that provides an output current waveform, a portion of which exhibits a linear variation of current with respect to time.

Applications

* Time base generators are used in televisions, CRO's, RADAR display time modulation, precise time measurements
* To display the variation with respect to time of an arbitrary waveform on the screen of oscilloscope, it is required to apply to one set of deflecting plates, a voltage which varies linearly with the time
* Time base generators are also called as "Sweep circuits"

Types of Time base Generators

i. Voltage Time base Generator
ii Current time base Generator

Time Base Generator

Voltage Time base Generator

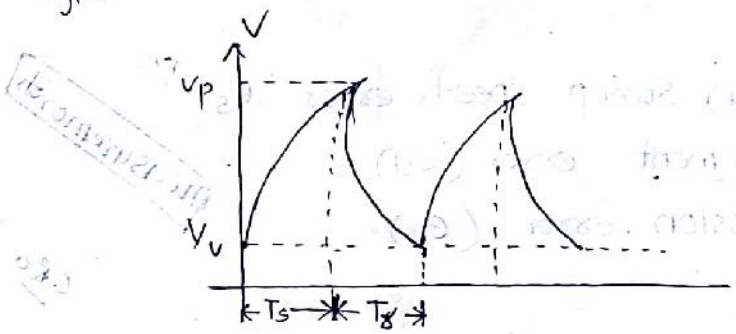
1. Exponential Sweep Circuit
2. UJT Sweep circuit
3. Transistor Switch Sweep Circuit
4. Transistor Current constant Sweep circuit
5. Bootstrap Sweep circuit
6. Miller sweep circuit

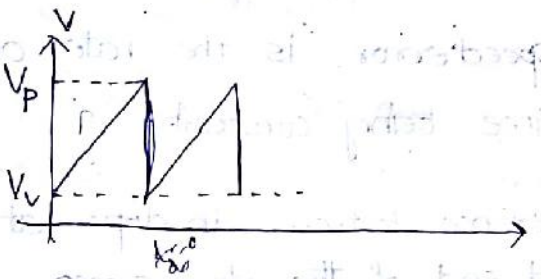
Current time base Generator

1. Transistor current sweep circuit

General features of Time base signal

* A typical waveform of a time base voltage as follows





ideal time base generator.

Sawtooth: look like saw

i.e The voltage starting from initial value increases linearly with time to maximum value after which it returns again to its initial value.

1. Sweep time T_s:

The time during which the output increases linearly from initial to final value is called as sweep time T_s.

2. Restoration Time (T_r):-

The time taken by the signal (output voltage to return to its initial value is called "Restoration time" or "Return time" or "Fly back time."

NOTE:

* In sawtooth waveform, the restoration time is zero
* Therefore, linear sweep signals are difficult to generate time base generators.
* Linear sweep signals may be distorted when transmitted through a coupling network.
* The deviation from linearity is expressed in three ways
  i) The slope (or) Sweep speed error e_s
  ii) The displacement error (e_d)
  iii) The transmission error (e_t)

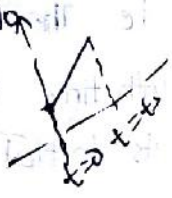
Measurements

i Sweep speed error:

The slope or sweep speed error is the rate of change of sweep voltage with time being constant

$$e_s = \frac{\text{difference in slope at beguning and end of the slope sweep}}{\text{Initial value of slope}}$$

$$e_s = \frac{\left.\frac{dV_o}{dt}\right|_{t=0} - \left.\frac{dV_o}{dt}\right|_{t=t_s}}{\left.\frac{dV_o}{dt}\right|_{t=0}}$$

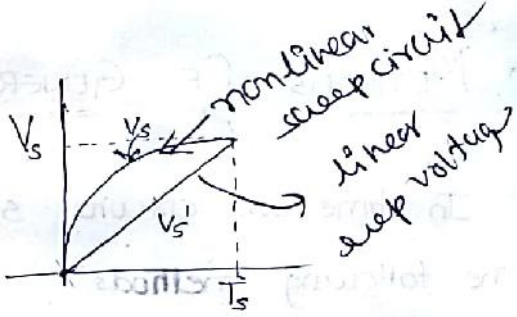


ii Displacement error:

It is the ratio of maximum difference between the actual sweep voltage and the linear sweep voltage which passes through the begining and end points of Amplitude

actual sweep voltage

$$e_d = \frac{(V_s - V_s')_{max}}{V_s}$$



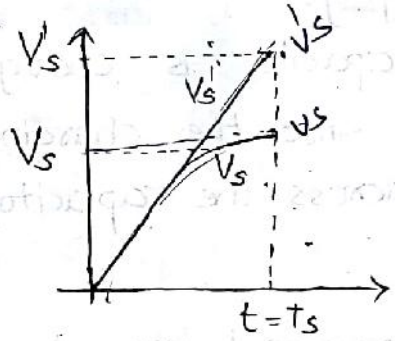
V_s - actual sweep voltage

V_s' - linear sweep voltage

V_s - Amplitude of sweep signal at $t = T_s$

Transmission error:- $[e_t]$

The ratio of difference between the input sweep voltage and output sweep voltage to the input sweep voltage at the end of the sweep time.



$$e_t = \frac{V_s' - V_s}{V_{sc}'}$$

where

V_s' - linear input sweep voltage

V_s - actual or output sweep voltage

NOTE:-

* The relation between the errors e_s, e_t, e_d is given as

$$e_d = \frac{e_s}{8} = \frac{e_t}{4}$$

or $$e_s = 8e_d = 2e_t$$

* The sweep speed error e_s is more dominant and the displacement error is least severe one.

METHODS OF GENERATING TIME BASE WAVEFORM

In time base circuits sweep linearity is achieved by one of the following methods

i Exponential Charging Circuit:

In this method, a capacitor is charged from a supply voltage through a resistor to a voltage which is small compared with the supply voltage

ii Constant Current Charging:

In this method, a capacitor is charged linearly from a constant current source since the charging current is constant, the voltage across the capacitor increases linearly

iii Miller Circuit

In this method an operational integrator is used to convert an input step voltage into a ramp waveform. (negative going ramp)

iv ~~Penta~~ The Phantastron circuit:

In this method, a pulse input is converted into a ramp. This is a new version of Miller circuit.

v Bootstrap Circuit:

* In this method a capacitor is charged linearly by a constant current which is obtained by maintaining a constant voltage across a fixed resistor in series with the capacitor.
* It generates positive going ramp.

vi) Compensating networks:

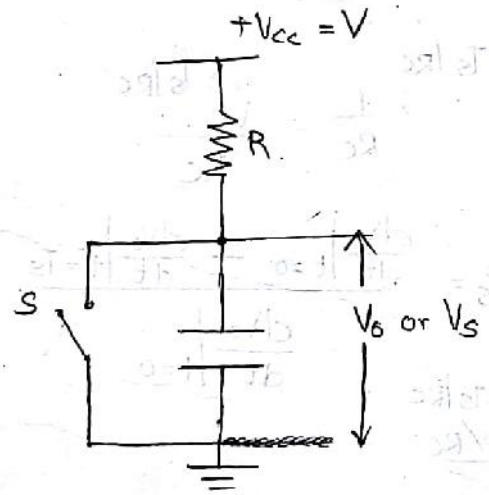
In this method a compensating circuit is introduced to improve the linearity of the basic Miller and bootstrap time base generators.

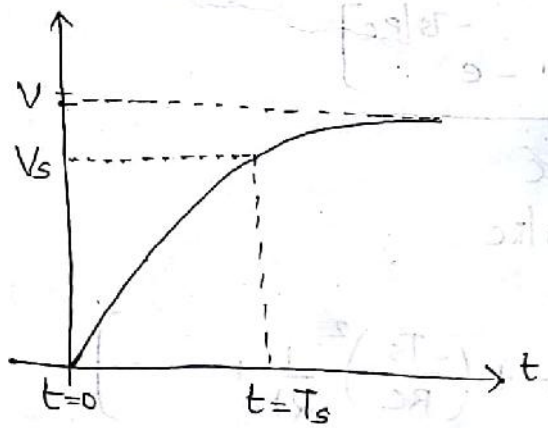
vii) An Inductor Circuit

In this method an RLC series circuit is used, since an inductor does not allow the current passing throughout it to change instantaneously, the current through the capacitor more or less remains constant and hence a more linear sweep voltage is obtained.

VOLTAGE TIME BASE GENERATOR

i Exponential Sweep Circuit





* The switch S is normaly closed at $t=0$
* When $t>0$, the switch is opened, the capacitor charges towards the supply voltage V with the time constant RC
* The voltage across the capacitor at any instant of time is given by $V_0(t) = V(1-e^{-t/RC})$

a. Slope or Sweep Speed error

$$V_0(t) = V(1-e^{-t/RC})$$

$$\frac{dV_0}{dt} = \frac{d}{dt}\left[V - Ve^{-t/RC}\right]$$

$$= 0 - V\left(e^{-t/RC} \cdot \frac{-1}{RC}\right)$$

$$= Ve^{-t/RC}\frac{1}{RC}$$

$$\left.\frac{dV_0}{dt}\right|_{t=0} = V \cdot e^{-(0/RC)} \cdot \frac{1}{RC} = \frac{V}{RC}$$

$$\left.\frac{dV_0}{dt}\right|_{t=T_s} = V \cdot e^{-T_s/RC} \cdot \frac{1}{RC} = \frac{Ve^{-T_s/RC}}{RC}$$

$$\text{slope error } e_s = \frac{\left.\frac{dV_0}{dt}\right|_{t=0} - \left.\frac{dV_0}{dt}\right|_{t=T_s}}{\left.\frac{dV_0}{dt}\right|_{t=0}}$$

$$= \frac{\frac{V}{RC} - Ve^{-T_s/RC}/RC}{\frac{V}{RC}}$$

$$= \frac{\frac{V}{RC}\left[1 - e^{-T_s/RC}\right]}{V/RC}$$

$$= 1 - e^{-T_s/RC}$$

$$= 1 - \left[1 - \frac{T_s}{RC} + \left(\frac{-T_s}{RC}\right)^2 \cdot \frac{1}{2!} + \cdots\right]$$

$$= 1-1 + \frac{T_s}{RC} + \left(\frac{T_s}{RC}\right)^2 \frac{1}{2!} + \cdots$$

Neglecting higher order terms, we get

$$\boxed{e_s = \frac{T_s}{RC}}$$

b Transmission error :-

$$e_t = \frac{V_s' - V_s}{V_s'}$$

$$V_s = V_o = V(1-e^{-t/RC})$$

at $t = T_s$ $\quad V_o = V(1-e^{-T_s/RC})$

Expanding, we get

$$V_s = V_o = V\left[1 - \left(1 - \frac{T_s}{RC} + \left(\frac{T_s}{RC}\right)^2 \cdot \frac{1}{2!} - \cdots\right)\right]$$

$$= V\left[1-1 + \frac{T_s}{RC} - \left(\frac{T_s}{RC}\right)^2 \frac{1}{2} + \cdots\right]$$

$$V_s = V\left[\frac{T_s}{RC} - \left(\frac{T_s}{RC}\right)^2 \frac{1}{2}\right]$$

Initial slope $\left.\frac{dV_o}{dt}\right|_{t=0} = \frac{V}{RC}$ $\quad \left\{ \because \frac{d}{dt}(V(1-e^{-t/RC})) = \frac{Ve^{-t/RC}}{RC} \right.$

If the initial slope is maintained at $t = T_s$, then the input voltage $\quad \left. \text{at } t=0 \;\; \frac{d}{dt}V_o = \frac{V}{RC} \right\}$

$V_s' = T_s \cdot$ (initial slope)

$$= T_s \cdot \frac{V}{RC}$$

$$V_s' = \frac{V \cdot T_s}{RC}$$

Now $\quad e_t = \dfrac{\frac{VT_s}{RC} - V\left[\frac{T_s}{RC} - \left(\frac{T_s}{RC}\right)^2 \cdot \frac{1}{2}\right]}{\frac{VT_s}{RC}}$

$$= \frac{\frac{VT_s}{RC}\left(1 - \left(1 + \frac{T_s}{RC}\cdot\frac{1}{2}\right)\right)}{\frac{VT_s}{RC}}$$

$$= \frac{T_s}{RC}\cdot\frac{1}{2}$$

$$\boxed{e_s = \frac{T_s}{2RC}}$$

$$= \frac{1}{2}\left(\frac{T_s}{RC}\right)$$

$$\boxed{e_t = \frac{1}{2}(e_s)}$$

c) Displacement error (e_d):-

The maximum displacement error between the actual sweep and the linear sweep which passes through the begining and end points of actual sweep amplitude occurs at $t = \frac{T_s}{2}$ and $V_s' = \frac{V_s}{2}$

$$e_d = \frac{V_s - V_s'}{V_s}$$

$$V_0 = V(1 - e^{-t/RC})$$

at $t = \frac{T_s}{2}$ $\quad V_s = V\left(1 - e^{-T_s/2RC}\right)$

$$V_s = V\left[1 - \left(1 - \frac{T_s}{2RC} + \frac{T_s^2}{8R^2C^2} - \cdots\right)\right]$$

$$V_s = V\left[\frac{T_s}{2RC} - \left(\frac{T_s}{2RC}\right)^2 \cdot \frac{1}{2}\right]$$

$$V_s = V\left[\frac{T_s}{2RC} - \left(\frac{T_s}{RC}\right)^2 \cdot \frac{1}{8}\right]$$

$$V_s' = \frac{V_s}{2}$$

$$= \frac{V}{2}\left[\frac{T_s}{2RC} - \left(\frac{T_s}{RC}\right)^2 \cdot \frac{1}{8}\right]$$

$$V_s' = \frac{V}{4}\left[\frac{T_s}{RC} - \left(\frac{T_s}{RC}\right)^2 \cdot \frac{1}{2}\right]$$

Now for transmission error initial slope V_s' is at

$$e_d = \frac{V_s}{2}$$

$$V_s' = \frac{V}{2}\left(1 - e^{-t/RC}\right)$$

$$\frac{dV_s'}{dt}\bigg|_{t=0} = \frac{V}{2}\left(\frac{1}{RC}\right)$$

$$V_s' = \frac{V}{2}\left[\frac{T_s}{RC} - \left(\frac{T_s}{RC}\right)^2 \cdot \frac{1}{2}\right]$$

$$V_s' = \frac{V}{2RC}$$

The pulse amplitude

$$V_s = \frac{V \cdot T_s}{RC}$$

Now $e_d = \dfrac{V_s - V_s'}{V_s}$

$$= \frac{V\left[\frac{T_s}{2RC} - \left(\frac{T_s}{RC}\right)^2 \cdot \frac{1}{8}\right] - \frac{V}{2RC}}{\frac{V \cdot T_s}{RC}}$$

$$= \frac{\frac{V}{RC}\left[\frac{T_s}{2} - \frac{T_s^2}{8R^2C^2} - \frac{1}{2}\right]}{\frac{V}{RC}(T_s)}$$

$$= \frac{V\left[\frac{T_s}{2RC} - \left(\frac{T_s}{RC}\right)^2 \cdot \frac{1}{8}\right] - \frac{V}{2}\left[\frac{T_s}{RC} - \left(\frac{T_s}{RC}\right)^2 \cdot \frac{1}{2}\right]}{\frac{VT_s}{RC}}$$

$$e_d = \frac{\frac{VT_s}{RC}\left[\frac{1}{2} - \frac{T_s}{RC}\cdot\frac{1}{8} - \frac{1}{2} + \frac{T_s}{4RC}\right]}{\frac{VT_s}{RC}}$$

$$= \frac{T_s}{4RC} - \frac{T_s}{8RC}$$

$$= \frac{T_s}{RC}\left[\frac{1}{4} - \frac{1}{8}\right]$$

$$= \frac{T_s}{4RC}\left[1 - \frac{1}{2}\right]$$

$$= \frac{T_s}{4RC}\left(\frac{1}{2}\right]$$

$$= \frac{T_s}{8RC}$$

$$= \frac{T_s}{RC}\left(\frac{1}{8}\right) = \boxed{\frac{e_s}{8} = e_d}$$

$$e_d = \frac{T_s}{2RC}\left(\frac{1}{4}\right) = \boxed{\frac{e_t}{4} = e_d}$$

∴ The relation between e_s, e_t and e_d is

$$\boxed{e_d = \frac{e_s}{8} = \frac{e_t}{4}}$$

(or)

$$\boxed{8e_d = e_s = 2e_t}$$

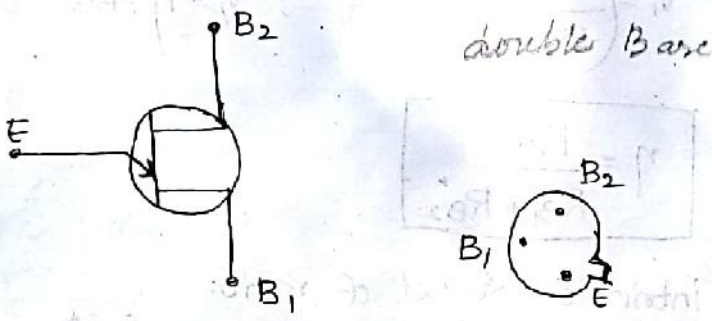
UJT SWEEP CIRCUIT (OR) UJT RELAXATION OSCILLATOR

UJT- Uni Junction Transistor

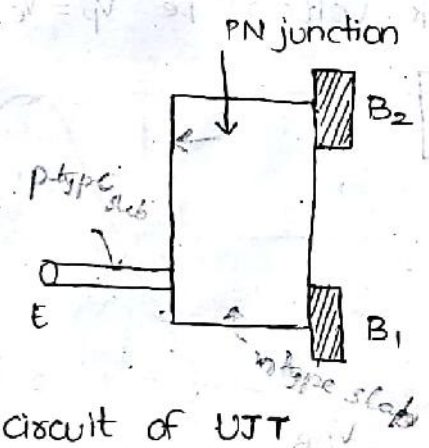
It has only one PN junction

double Base diode

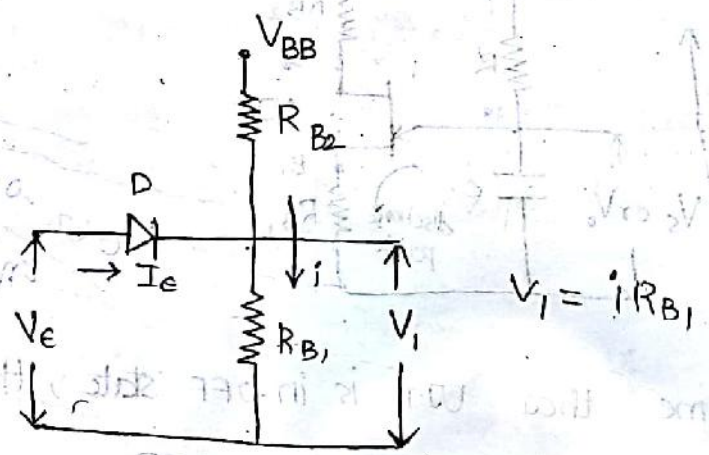
symbol:



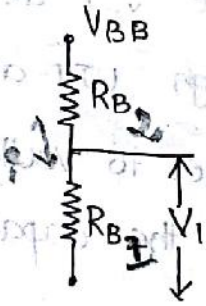
construction:



Equivalent circuit of UJT



If $I_E = 0$ equivalent circuit is



$V_1 = i R_{B_1}$

where $i = \frac{V_{BB}}{R_{B_1} + R_{B_2}}$

$$V_1 = \left(\frac{V_{BB}}{R_{B_1} + R_{B_2}}\right) R_{B_1} \; ; \; V_1 = \eta V_{BB}$$

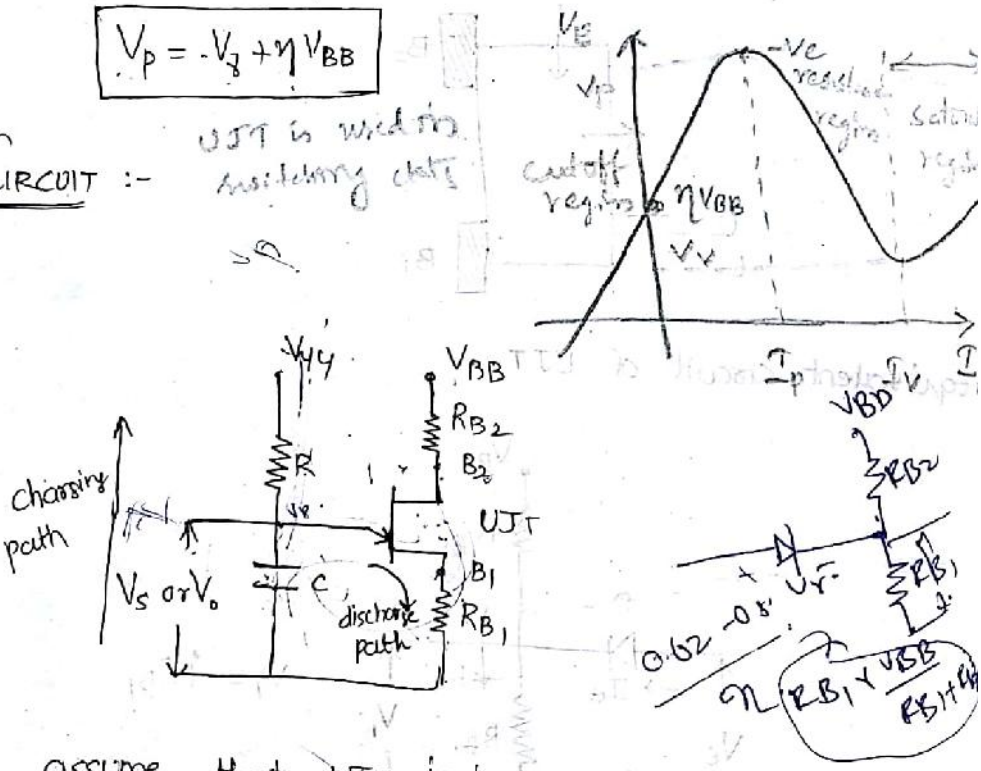
* $$\boxed{\eta = \frac{R_{B_1}}{R_{B_1} + R_{B_2}}}$$

η is intrinsic stand of ratio. range of η is 0.62 - 0.86 / 0.64 - 84

The value of emitter voltage which makes the diode conducts is termed as peak voltage i.e $V_p = V_E = V_\gamma + V_1$

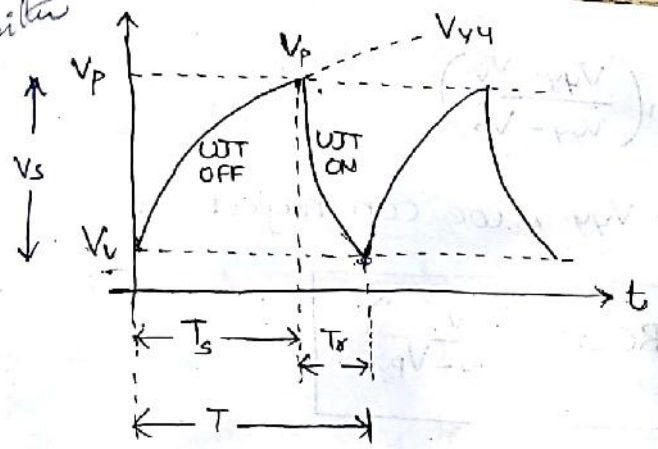
$$\boxed{V_p = V_\gamma + \eta V_{BB}}$$

SWEEP CIRCUIT :- UJT is widely switching chart



* Let us assume that UJT is in OFF state, the capacitor C charges towards V_{YY} through resistor R.
* When charged to peak voltage V_p, the UJT turns ON, now the capacitor discharges through UJT and R_{B_1}
* When the capacitor discharges to valley voltage V_v, the UJT turns OFF and again the capacitor starts charging and cycle repeats.

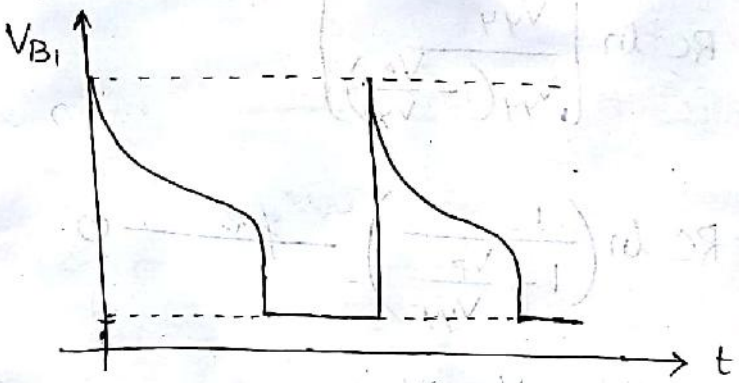
At Emitter



$V_{yy} > V_p$.

$V_{yy} > V_{BB}$.

At Base B_1



Small 'C' Restore time is less.

* FREQUENCY OF OSCILLATIONS

Generally, for the capacitor charging equation is given as

$$V_o = V_{fin} - (V_{fin} - V_{ini}) e^{-t/RC}$$

$$V_s = V_{yy} - (V_{yy} - V_{BBV}) e^{-t/RC}$$

at $t = T_s$; $V_s = V_p$

$$V_p = V_{yy} - (V_{yy} - V_v) e^{-T_s/RC}$$

$$\Rightarrow (V_{yy} - V_v) e^{-T_s/RC} = V_{yy} - V_p$$

$$e^{-T_s/RC} = \frac{V_{yy} - V_p}{V_{yy} - V_v}$$

$$\frac{-T_s}{RC} = \ln\left(\frac{V_{yy} - V_p}{V_{yy} - V_v}\right)$$

$$\frac{T_s}{RC} = \ln\left(\frac{V_{yy} - V_v}{V_{yy} - V_p}\right)$$

$$T_s = RC \cdot \ln\left(\frac{V_{yy} - V_v}{V_{yy} - V_p}\right)$$

Since $V_v << V_{yy}$, we can neglect V_v

$$\therefore \boxed{T_s = RC \ln\left(\frac{V_{yy}}{V_{yy} - V_p}\right)}$$

$$T_s = RC \ln\left[\frac{V_{yy}}{V_{yy}\left(1 - \frac{V_p}{V_{yy}}\right)}\right]$$

$$T_s = RC \ln\left(\frac{1}{1 - \frac{V_p}{V_{yy}}}\right) \quad \text{——— ①}$$

Also w.k.t $V_p = V_\gamma + \eta V_{BB}$

V_{BB} and V_{yy} are both supply voltages

$$V_{yy} \simeq V_{BB}$$

$$V_p = V_\gamma + \eta V_{yy}$$

Since $V_\gamma << V_{yy}$, neglecting V_γ

$$V_p = \eta V_{yy}$$

$$\therefore \frac{V_p}{V_{yy}} = \eta \quad \text{——— ②}$$

Substituting ② in ①

$$\boxed{T_s = R_C \ln\left(\frac{1}{1 - \eta}\right)}$$

Where η is intrinsic stand of ratio

$$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}}$$

Frequency $f_s = \frac{1}{T_s}$

$$f_s = \frac{1}{RC \ln\left(\frac{1}{1-\eta}\right)}$$

Total time period $T = T_s + T_\gamma$

T_γ is very less and hence

$$T = T_s$$

$V = V_{yy} - V_V$

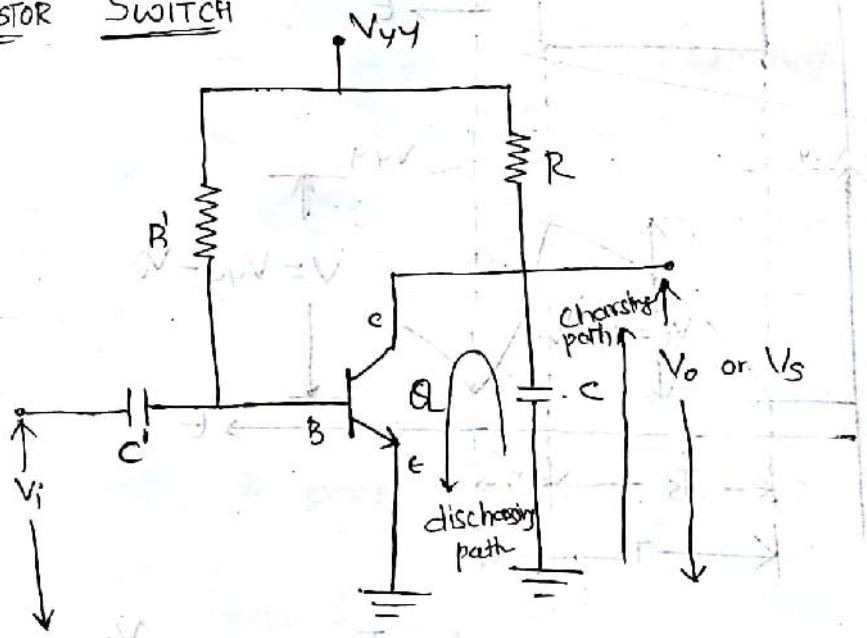
$V_S = V_p - V_V$

$e_s = \frac{T_s}{RC}$ & $\frac{V_S}{V_S}$

$e_t = \frac{T_s}{2RC}$

$e_d = \frac{T_s}{8RC}$

TRANSISTOR SWITCH SWEEP CIRCUIT OR) SWEEP CIRCUIT USING TRANSISTOR SWITCH



The input gating waveform V_i may be output of monostable circuit as it may be output of Astable circuit where we get a free running sweep circuit.

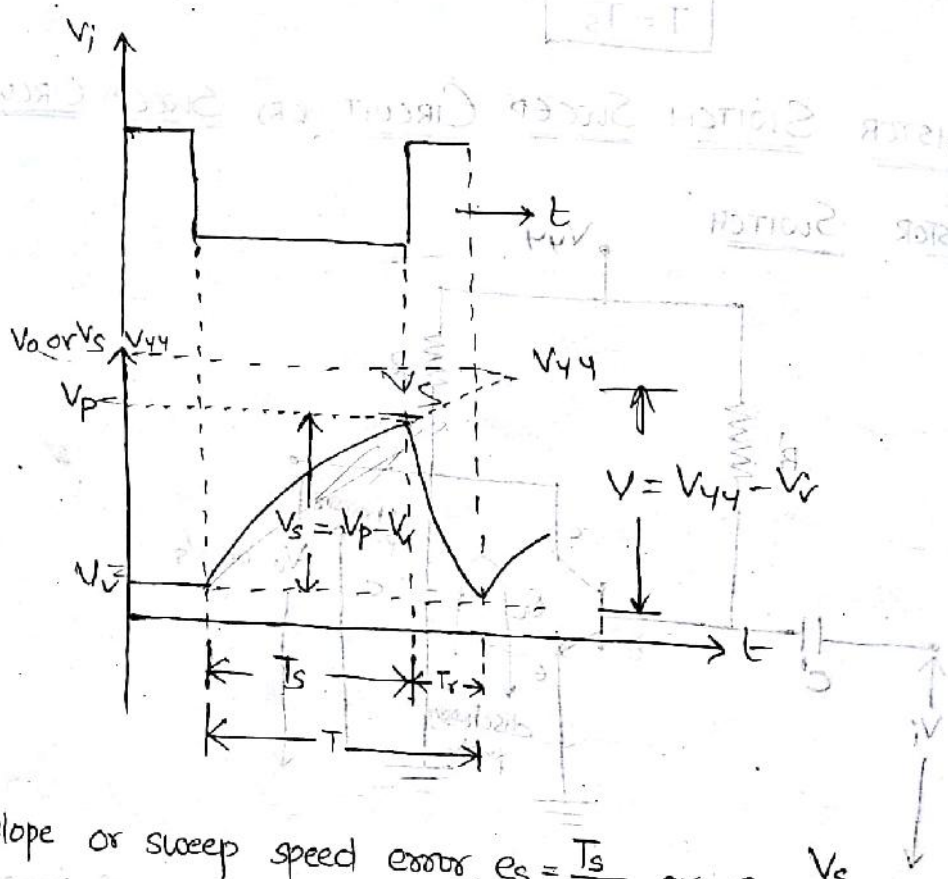
OPERATION

* For $t<0$, the transistor gets enough base drive from V_{yy} through R', the transistor is ON, goes to saturation region so the output is lowest magnitude = V_{CE} sat = V_V
* For $0<t<T_s$, the transistor remains in cutoff, then it goes to OFF, the capacitor C charges through R towards

V_{YY} with time constant RC

* at $t = T_s$, the output is its peak value V_p
* For $t > T_s$, the capacitor C discharges and reaches to valley voltage V_v

Input and output waveforms



The slope or sweep speed error $e_s = \frac{T_s}{RC}$ or $e_s = \frac{V_s}{V}$

where $V = V_{YY} - V_v$

$V_s = V_p - V_v$

V_p – peak voltage

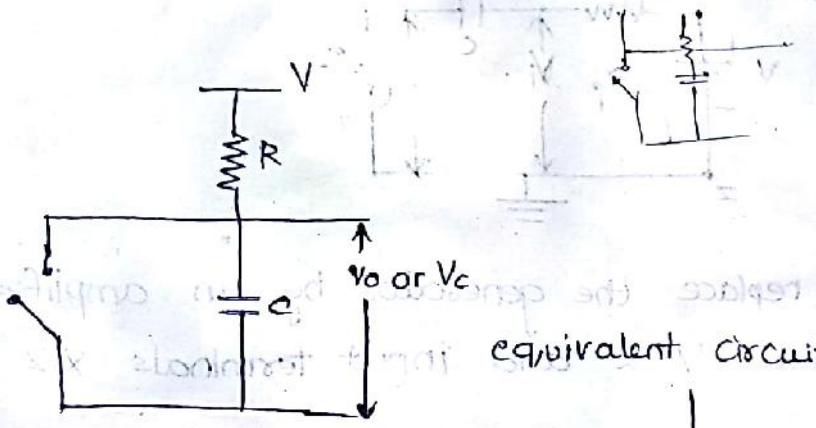
V_r – Valley voltage

V_s – Sweep voltage

V_{YY} – Supply voltage

BASIC PRINCIPLES

* The linearity of the time base waveforms may be improved by using circuits involving feedback
* The basic exponential sweep circuit cannot generate linear sweep ie, the slope of the output waveform decreases.



equivalent circuit is

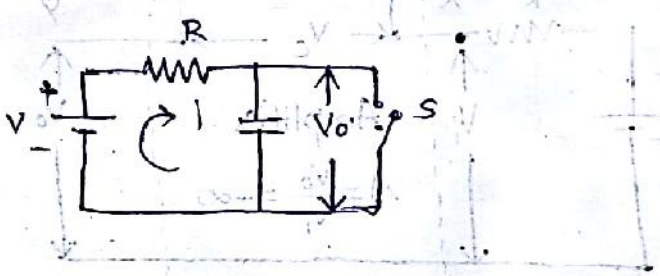


fig:- The current decreases exponentially with time.

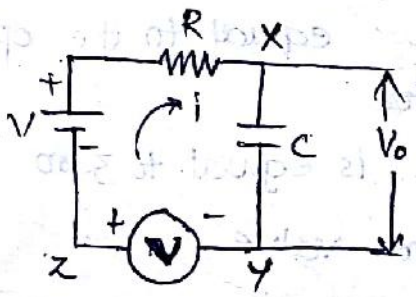
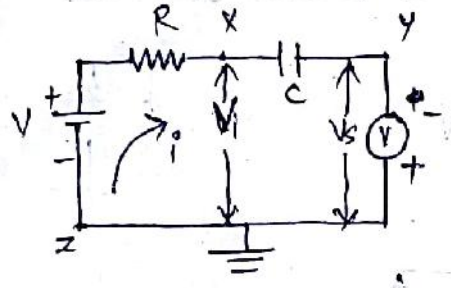


Fig:- Current remains constant

* A perfect linear output can be obtained if the initial charging current $i = \frac{V}{R}$ is maintained constant
* It is achieved by introducing an auxiliary voltage generator V whose generated voltage is always equal to and opposite to the voltage across the capacitor

MILLER

* Suppose the point z is grounded, the linear sweep will appear between the points Y and ground and increases in negative direction.



* Now, replace the generator by an amplifier with output terminals Y, Z and input terminals X, Z

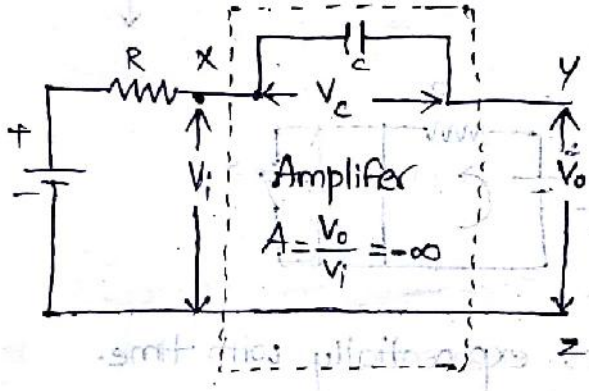


Fig: Miller Integrated Circuit

* The generated voltage is always equal to the opposite to the voltage across capacitor
* The voltage between x and z is equal to zero i.e $V_i = 0$ and output is infinite negative value
* It is achieved by using an operational integrator with a gain of infinity with negative going ramp is called Miller sweep circuit.

BOOT STRAP

* Suppose the point Y is grounded, the output is taken at Z
* The linear sweep will appear between Z and ground and will increase in the positive direction.
* By replacing the generator with an amplifier with input terminals X and Y, and output terminals Z and Y

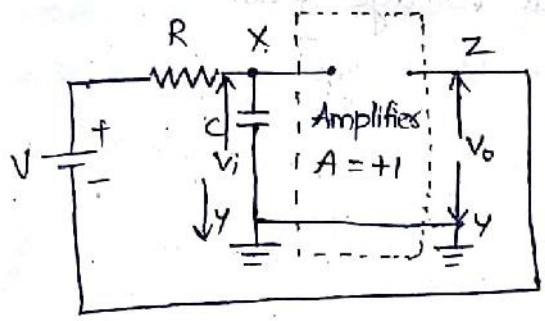


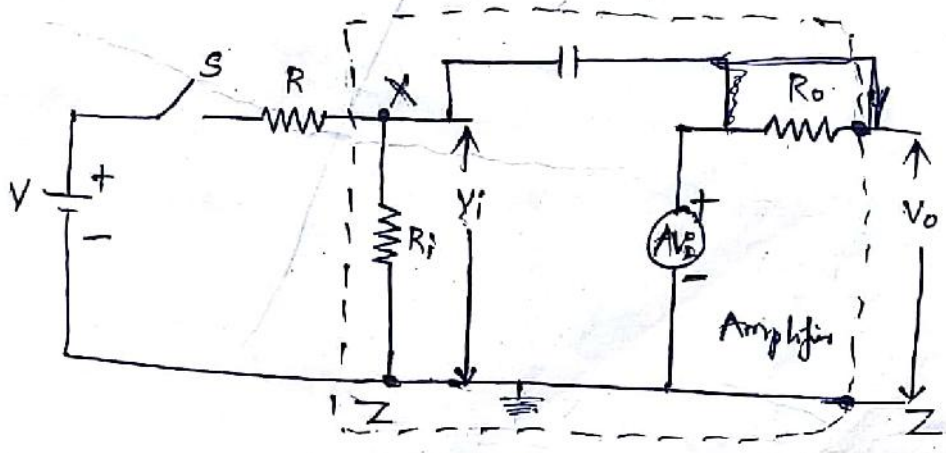
Fig: Bootstrap sweep circuit

* The generator voltage V at any instant is equivalent to the voltage across the capacitor, then V_o must be equivalent to V_i and amplifier voltage gain must be equal to unity with positive going Ramp.

$$A_v = \frac{V_o}{V_i} = +1$$

* This circuit is called as Bootstrap sweep circuit

MILLER SWEEP CIRCUIT:-

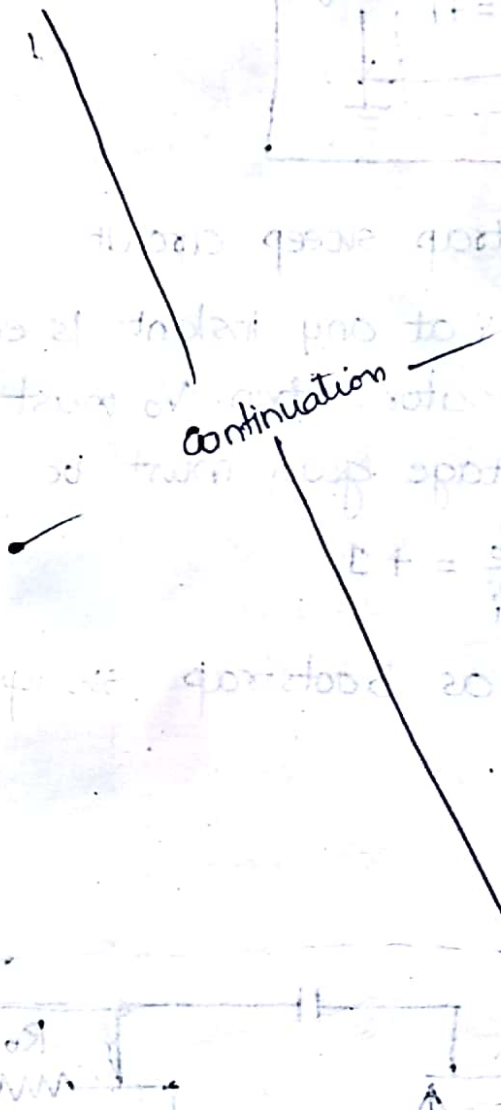


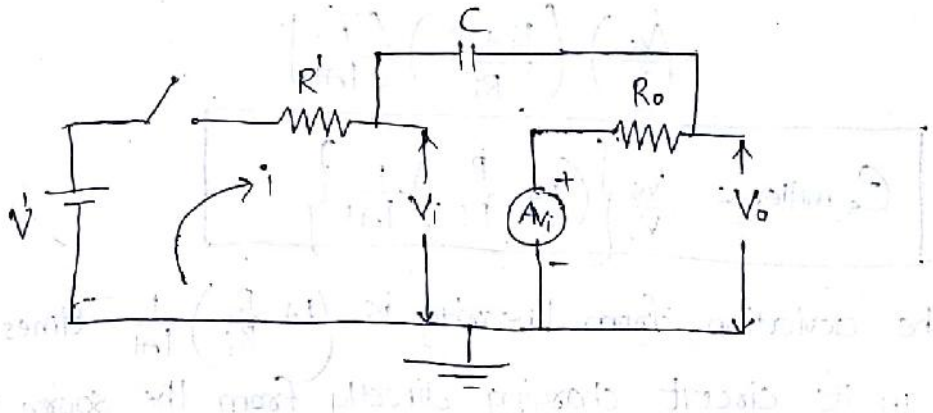
* A switch 's' at the closing of which the sweep starts included

* The basic amplifier has been replaced at the input side by its input resistance R_i and the output side by its Thevinin's circuit (voltage source with series resistance)

Where R_o – output resistance

A – Open circuit voltage gain.





* The above figure is obtained by replacing V, R, R_i in the input side by voltage source V' in series with the resistor R'

where $V' = V\left(\frac{R_i}{R+R_i}\right)$

$$R' = R \| R_i = \frac{R \cdot R_i}{R+R_i}$$

* If switch S is closed at t=0, if the initial voltage across the capacitor is zero then $V_o = 0$, this indicates that the sweep starts from zero. shat called

* At $t=\infty$, the capacitor acts as an open circuit and no current flows.

$V_i = V'$ and output $V_o = AV_i = AV_i'$ ——— (1)

* Thus the output is in exponential, sweep is negative going ramp since A is negative number.

* slope or sweep speed error $e_s = \frac{V_s}{V} = \frac{V_s}{V_o}$

where V_s – Sweep Amplitude

V_o – peak to peak value of output

∴ The slope for Miller circuit

$$e_{s\,miller} = \frac{V_s}{AV'}$$

$$= \frac{V_s}{A\left[\frac{R_i}{R+R_i}\right]V} \quad \left(\because V_i' = V\left(\frac{R_i}{R+R_i}\right)\right.$$

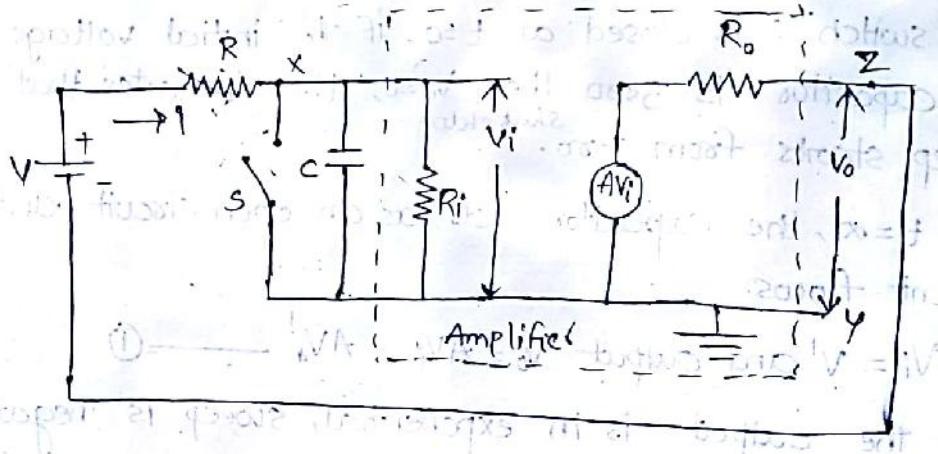
$$= \left(\frac{V_s}{V}\right)\left(\frac{R_i + R}{R_i}\right)\left(\frac{1}{|A|}\right)$$

$$C_{s\,miller} = \frac{V_s}{V}\left\{\left(1 + \frac{R}{R_i}\right)\frac{1}{|A|}\right\}$$

∴ The deviation from linearity is $\left(1 + \frac{R}{R_i}\right)\frac{1}{|A|}$ times that of an RC circuit charging directly from the source V.

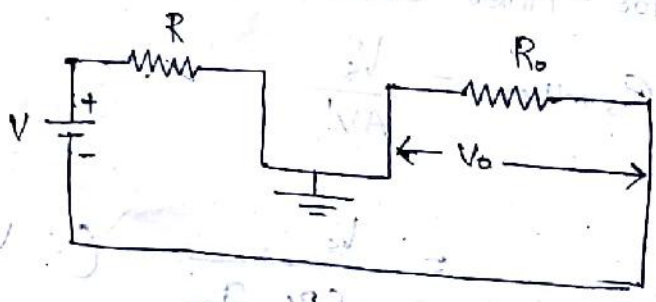
* Hence improvement in the linearity can be obtained with Miller circuit.

BOOTSTRAP SWEEP CIRCUIT

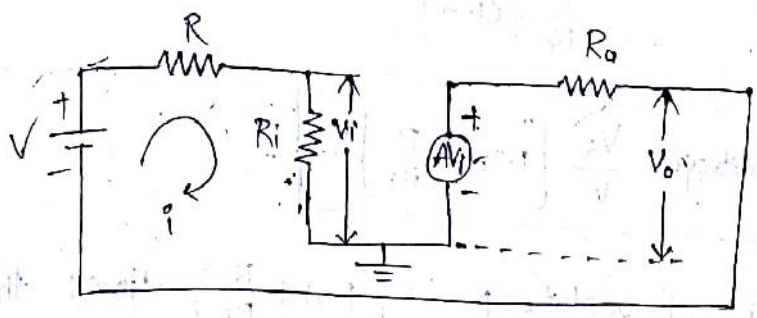


* At t=0, the switch was closed, the voltage across the capacitor cannot change instantaneously since the capacitor is short circuited

* As $V_i = 0$, $AV_i = 0$, the output voltage can be obtained in the following circuit



* At $t=\infty$, the capacitor acts as an open circuit, then the circuit can be redrawn as follows.



$V_i = iR_i$ and $V_o = AV_i - iR_o$

$V_o = AiR_i - iR_o$

$V_o = (AR_i - R_o)\, i$

Applying the KVL to above circuit

$$V = iR + iR_i - AV_i + iR_o$$

$$= iR + iR_i - AiR_i + iR_o$$

$$= i\,(R + R_i - AR_i + R_o)$$

$$= i\,(R + R_o + R_i(1-A))$$

$$i = \frac{V}{R + R_o + R_i(1-A)}$$

$$\therefore V_o = \frac{V}{R + R_o + (1-A)R_i}\,(AR_i - R_o)$$

Since Bootstrap has a unity gain and R_o is neglected

$$V_o = \frac{R_i \cdot V}{R + (1-A)R_i}$$

$$V_o = \frac{V}{\frac{R}{R_i} + (1-A)}$$

The slope or sweep speed error

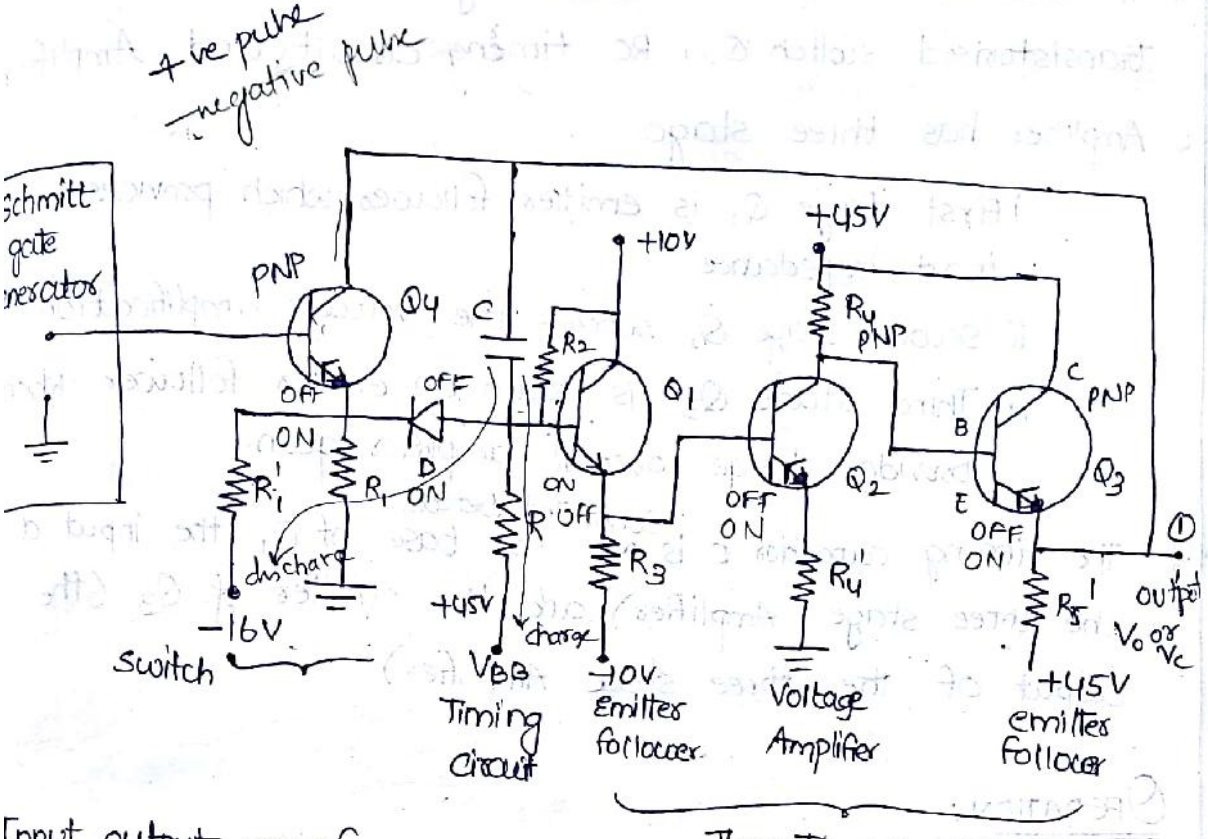
$$e_{s\ \text{Bootstrap}} = \frac{V_s}{V_o}$$

$$e_{s(Bootstrap)} = \frac{V_s}{\frac{V}{\frac{R}{R_i} + (1-A)}}$$

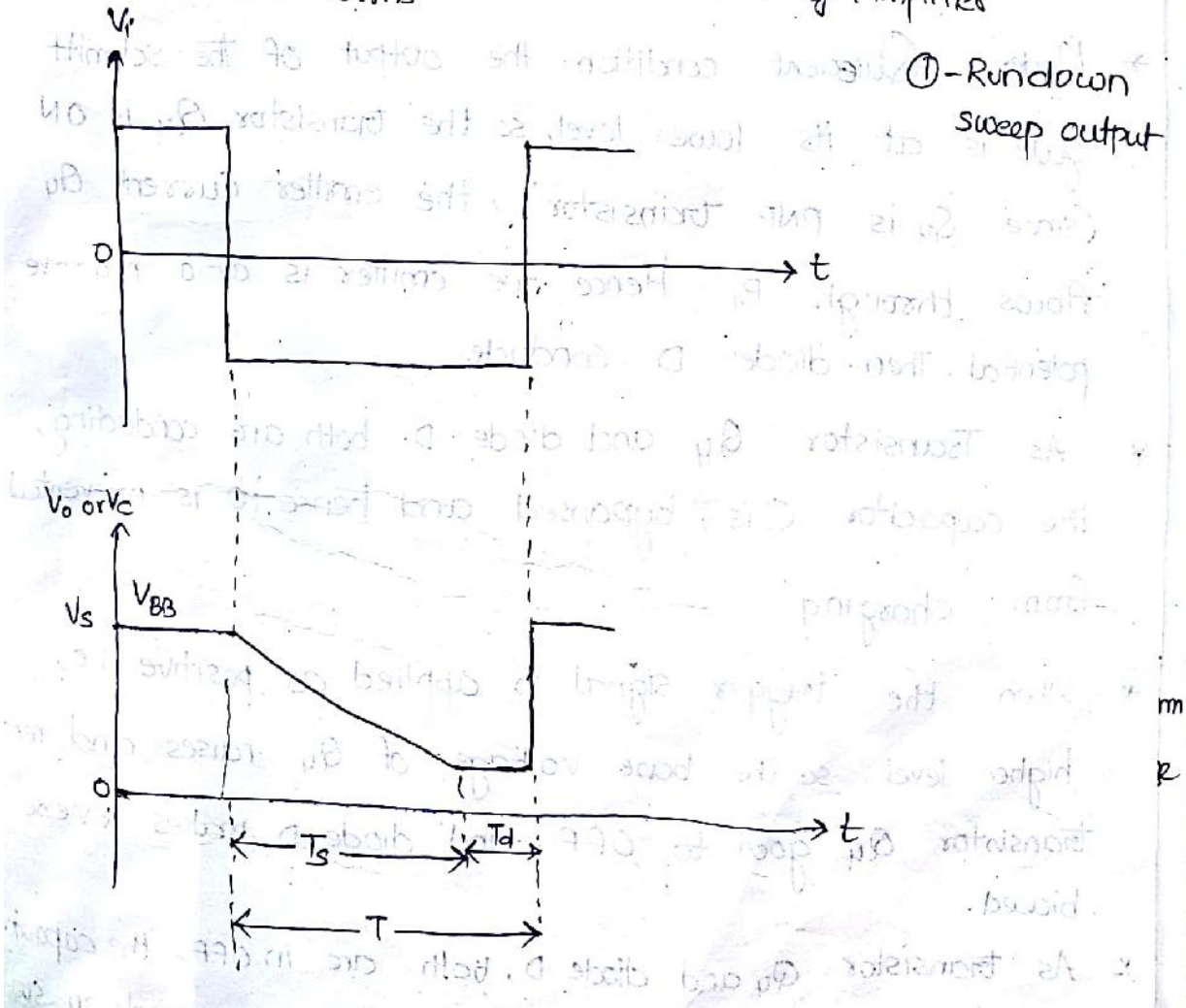
$$\boxed{e_{s\ Bootstrap} = \frac{V_s}{V}\left[1 - A + \frac{R}{R_i}\right]}$$

The slope error of bootstrap is $\left(1-A+\frac{R}{R_i}\right)$ times the capacitor charges directly from V through resistor R. Hence linearity improvement can be obtained with Bootstr sweep circuit

TRANSISTORISED MILLER TIME BASE GENERATOR



Input output waveforms



CONSTRUCTION

* The transistorised miller time base generator consists of transistorised switch Q_4, RC timing circuit and Amplifier
* Amplifier has three stages
  - i First stage Q_1 is emitter follower which provides high input impedance
  - ii second stage Q_2 supplies the voltage amplification.
  - iii Third stage Q_3 is again an emitter follower which provides large overall amplifier gain.
* The timing capacitor C is connected between the base of Q_1 (the input of the three stage Amplifier) and the emitter of Q_3 (the output of the three stage Amplifier)

OPERATION:

* Under Quiecient condition, the output of the schmitt gate is at its lower level; so the transistor Q_4 is ON (since Q_4 is PNP transistor), the emitter current Q_4 flows through R_1. Hence the emitter is at a negative potential. Then diode D conducts.
* As Transistor Q_4 and diode D both are conducting, the capacitor C is byparsed and hence it is prevented from charging

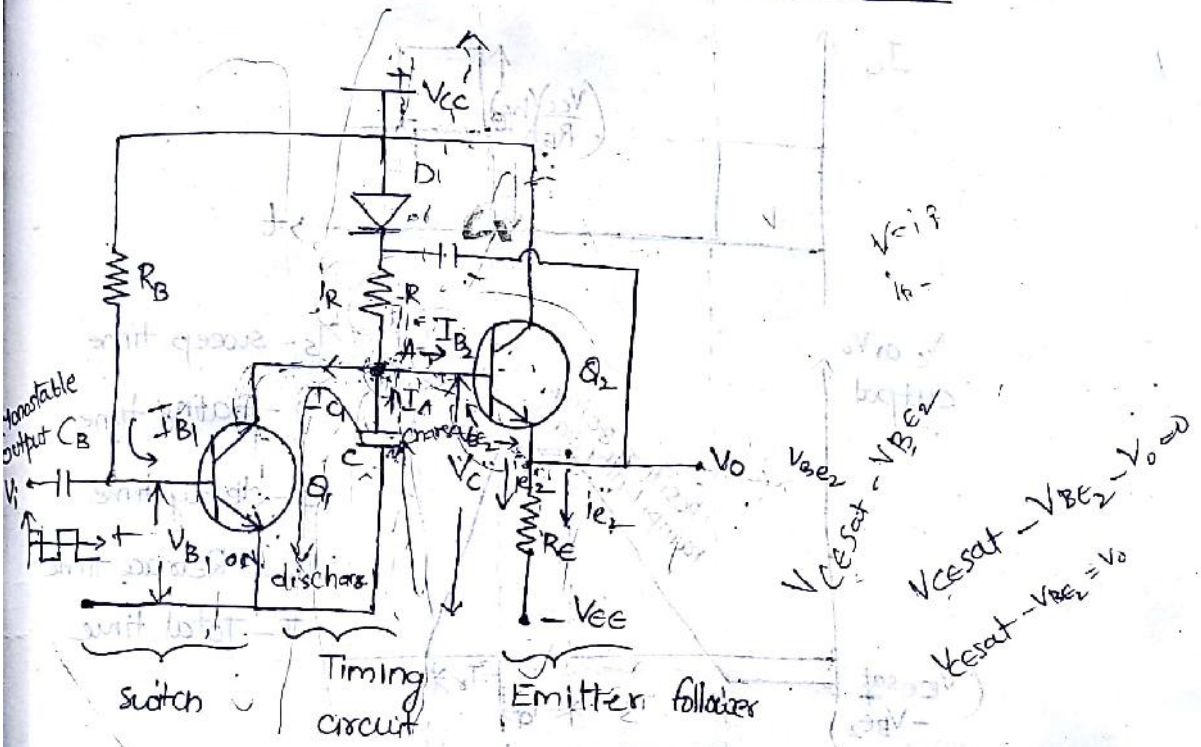
When the trigger signal is applied as positive i.e; higher level, so the base voltage of Q_4 raises and hence transistor Q_4 goes to OFF, and diode D makes reverse biased.

As transistor Q_4 and diode D, both are in OFF, the capacitor C gets charged from V_{BB} through R. Hence a rundown sweep

is obtained at the emitter of Q_3.

* At the end of the sweep, the capacitor C discharges through diode D and transistor Q_4.
* The charging speed or sweep speed depends on values of R and C and also depends on V_{BB}

TRANSISTORISED BOOTSTRAP TIMEBASE GENERATOR



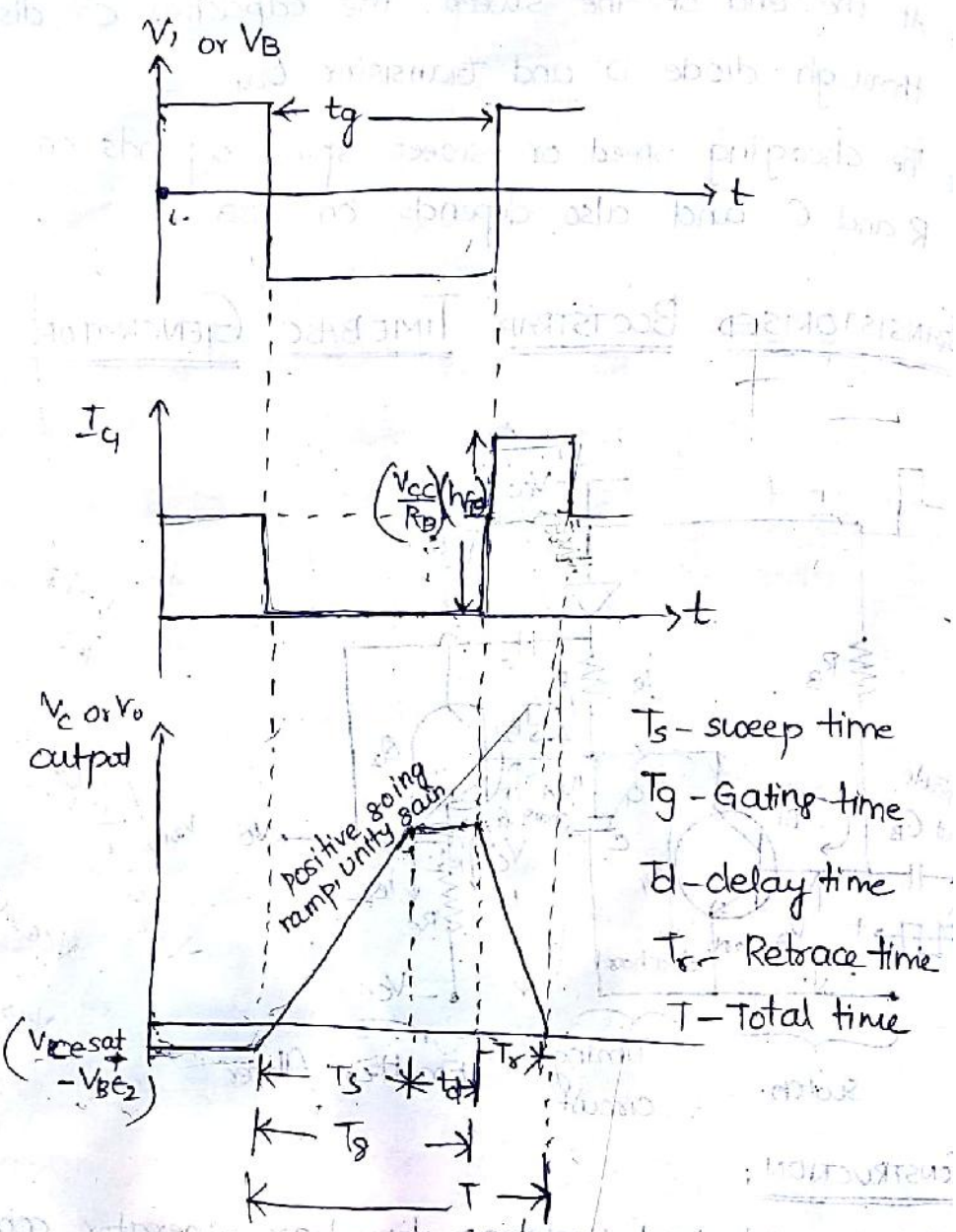
CONSTRUCTION;

* The transistorised bootstrap timebase generator consists of switch, timing circuit and emitter follower
* The input of transistor Q_1 is gating waveform from Monostable Multivibrator CIt is a repetetive wave like a square wave)

OPERATION;

* Q_1 is Under Quiecent condition, at t=0, the gating waveform is positive voltage, then the transistor Q_1 is ON, so the voltage across the capacitor which is also voltage at the collector of Q_1
* Since Q_2 is emitter follower, the voltage at the emitter of Q_2 is the output voltage i.e. $V_o = V_{CEsat} - V_{BE_2} \simeq$ negative voltage

Input-output waveforms



* So the capacitor cannot charge instantaneously
* V_o is a small negative voltage, if we neglect this voltage as well as small drop across diode D, then capacitor C_1, the current $I_R = \frac{V_{cc}}{R}$
* The emitter current of Q_2 $I_{E_2} = \frac{V_{ee}}{R_e}$
* At point A, applying KCL, i.e

$$I_R = I_{C_1} + I_{B_2}$$

I_{B_2} is very small than I_{C_1} then $I_R \simeq I_{C_1} = \frac{V_{cc}}{R}$, ($I_{C_1} = h_{fe} I_B$)

* As Q_1 is ON, the base current $I_{B_1} = \frac{V_{cc}}{R_B}$. It must be equal to $I_{B_1} = \frac{I_{C_1}}{h_{fe}} = \frac{V_{cc}}{R_B h_{fe}} \Rightarrow I_{C_1} = \frac{V_{cc}}{R_B} \cdot h_{fe}$.

$I_C = \beta I_B$
$= h_{fe} I_B$
$I_B = \frac{I_C}{h_{fe}} \cdot \frac{V_{cc}}{R_{th}}$

FORMULATION OF SWEEP

* When a negative Gate waveform is applied, the Transistor Q_1 becomes OFF, now the current I_{C_1} flows through the capacitor C, so the voltage across the capacitor raises according to the following equation.

$$V_c = \frac{1}{C}\int i\,dt$$

$$= \frac{1}{C}\int I_{C_1}\,dt$$

$$= \frac{1}{C}\int \frac{V_{cc}}{R}\,dt$$

$$= \frac{V_{cc}}{RC}\int dt$$

$$\boxed{V_c = \frac{V_{cc}}{RC}(t)}$$

* Since Q_2 is Emitter follower which has a unity voltage gain, then $V_o = V_c = \frac{V_{cc}}{RC}(t)$

at $t = t_s = T_s$

$$\therefore \boxed{V_s = \frac{V_{cc}}{RC} T_s}$$

RETRACE INTERVAL

* At $t > T_G$, the transistor Q_1 becomes ON, the capacitor C discharges through Q_1 transistor.
* So Emitter follower Q_2, V_c falls then V_o also falls by same
* Applying the KCL at point A and neglecting I_{B_2}

$$I_{C1} = I_R + I_A$$

$$I_A = I_{C1} - I_R$$

$$= \frac{V_{CC}}{R} - I_R$$

$$= h_{fe} I_{B1} - I_R$$

$$I_A = h_{fe} \frac{V_{CC}}{R_B} - \frac{V_{CC}}{R}$$

If the Retrace time is T_r, then the charge lost by the Capacitor $Q = I_A \cdot T_r$.

$$C \cdot V_S = I_A \cdot T_r \qquad V_S - \text{sweep voltage}$$

$$\boxed{V_S = \frac{I_A \cdot T_r}{C}}$$

$$T_r = \frac{C V_S}{I_A}$$

$$= \frac{C V_S}{h_{fe} \frac{V_{CC}}{R_B} - \frac{V_{CC}}{R}}$$

$$T_r = \frac{C V_S}{V_{CC}\left[\frac{h_{fe}}{R_B} - \frac{1}{R}\right]}$$

$$\boxed{T_r = \frac{C V_S / V_{CC}}{\left[\frac{h_{fe}}{R_B} - \frac{1}{R}\right]}}$$

Recovery Process

Total time period $T = T_g + T_r$.

Slope or Sweep Speed error

slope or sweep speed error e_s is given as

$$e_s = \frac{V_s}{V_{cc}}\left(1 - A_v + \frac{R}{R_i} + \frac{C}{C_1}\right)$$

V_s – Sweep Voltage

R_i – Input Impedance

$$1 - A_v = \frac{h_{ie}}{R_i}$$

$$R_i = h_{ie} + A_i R_E$$

$$A_i = \frac{-h_{fe}}{1 + h_{oc} R_E}$$

R_E – load

$$h_{fe} = -(1 + h_{fe}) \; ; \; h_{oc} = h_{oe}$$

(or) $$A_i = \frac{+(1 + h_{fe})}{1 + h_{oe} R_E}$$

⇒ The transistorised Bootstrap sweep circuit has following parameters, $V_{cc} = 10V$ $V_{EE} = -10V$, R_B – Base Resistance $= 30K\Omega$, $R = 10K\Omega$, $R_E = 5K\Omega$, $C = 0.002\mu F$, $C_1 = 0.25\mu F$, $h_{fe} = 60$, $h_{ie} = 2K\Omega$ $\frac{1}{h_{oe}} = 10K\Omega$, $h_{re} = 10^{-4}$. The input gate has an amplitude of 1 volt, and width of 50 μsec.

a) Plot the input voltage, collector current I_{C_1}, output voltage V_0

b) Find the sweep speed time T_s

c) Find the Retrace time

d) Find the slope or sweep speed error e_s.

Given data

$V_{cc} = 10V$ $R = 10K\Omega$

$V_{EE} = -10V$ $R_E = 5K\Omega$ $C_1 = 0.25\mu F$

$R_B = 30K\Omega$ $C = 0.002\mu F$ $h_{fe} = 60$ $h_{ie} = 2K\Omega$,

$\frac{1}{h_{oe}} = 10K\Omega$, $h_{re} = 10^{-4}$

b) Sweep speed time T_s ⇒

W.K.T $V_s = \frac{V_{cc}}{RC} T_s$

$$\frac{V_{cc}}{R_C} = \frac{10}{10\times10^{3}\times 0.002\times10^{-6}}$$

$$\frac{V_{cc}}{R_c} = 5\times10^{5}$$

$V_S = V_{cc}$

$$V_{cc} = 5\times10^{5}\times T_S$$

$$\frac{10}{5\times10^{5}} = T_S$$

$$20\times10^{-6} = T_S$$

$$\boxed{T_S = 20\,\mu sec}$$

Retrace time

$$T_r = \frac{C\, V_S / V_{cc}}{\frac{h_{fe}}{R_B} - \frac{1}{R}}$$

$V_S = V_{cc} \Rightarrow$

$$T_r = \frac{C}{\frac{h_{fe}}{R_B} - \frac{1}{R}}$$

$$= \frac{0.002\times10^{-6}}{\frac{60}{30\times10^{3}} - \frac{1}{10\times10^{3}}}$$

$$T_r = 1.05\times10^{-6}$$

$$\boxed{T_r = 1.0526\,\mu sec}$$

Slope

$$e_S = \frac{V_S}{V_{cc}}\left(1 - A_v f \frac{R}{R_i} + \frac{C}{C_1}\right)$$

$V_S = V_{cc}$ $\quad e_S = \left(1 - A_v f \frac{R}{R_i} + \frac{C}{C_1}\right.$

$$A_i = \frac{1+h_{fe}}{1+h_{oe}R_e}$$

$$= \frac{1+60}{1+\left(\frac{1}{10\times10^3}\right)5\times10^3}$$

$$= \frac{61}{1+\frac{1}{2}}$$

$$= \frac{61\times2}{3}$$

$$\boxed{A_i = 40.66}$$

$$R_i = h_{ie} + A_i R_e$$

$$= 2\times10^3 + (40.66)(5\times10^3)$$

$$\boxed{R_i = 205.3\ k\Omega}$$

$$e_s = \left[1 - 40.66 + \frac{10k\Omega}{205.3k\Omega} + \frac{0.0024F}{0.25\times10^6}\right]$$

$$= -39.603$$

$$|e_s| = 1 - 39.603$$

$$\boxed{e_s = 39.60}$$

$$1 - A_v = \frac{h_{ie}}{R_i}$$

$$-A_v = \frac{h_{ie}}{R_i} + 1$$

$$e_s = \left[1 - 0.9902 + \frac{10\ k\Omega}{205.3k\Omega} + \frac{0.0024F}{0.25\mu F}\right]$$

$$A_v = 1 - \frac{h_{ie}}{R_i}$$

$$= 1 - \frac{2k\Omega}{205.3k\Omega}$$

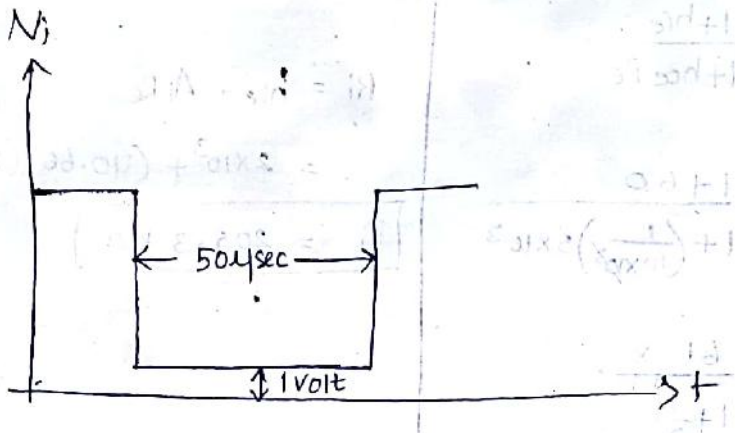
$$A_v = 0.9902$$

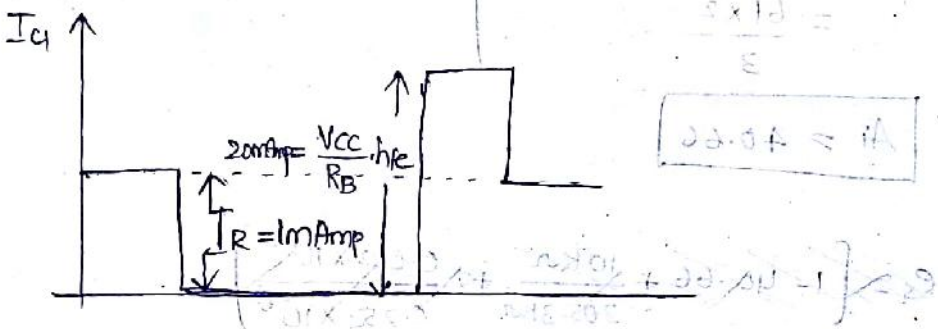
$$= 0.0665$$

$$\boxed{e_s = 0.0665}$$

Input Gate voltage is 1 volt

and the width in 50 μsec

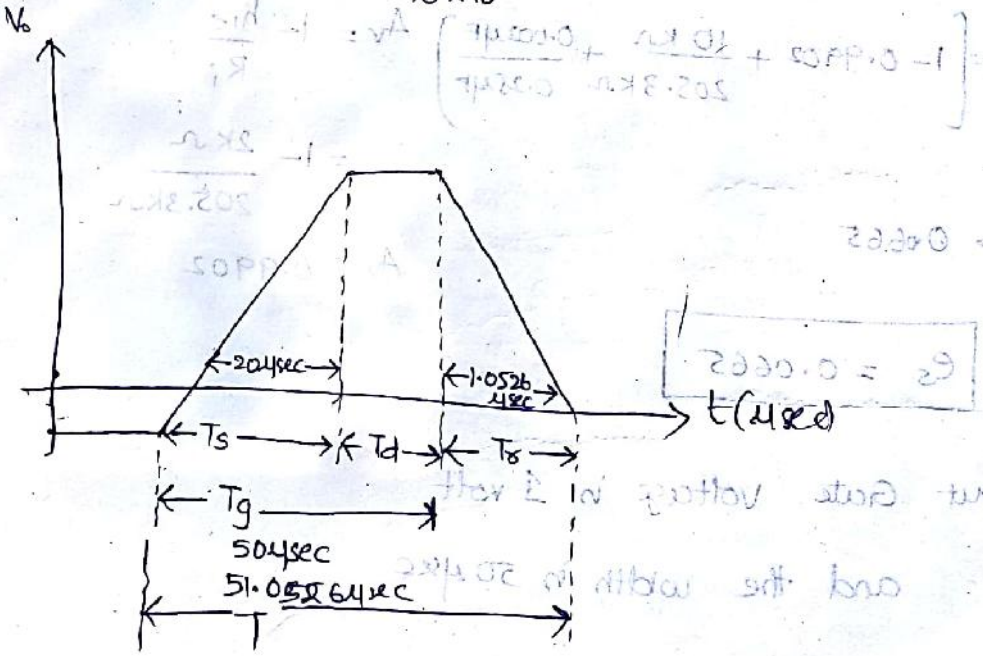




$$I_{C1} = \frac{V_{CC}}{R_B} \cdot h_{fe} = \frac{10}{30\times10^3} \cdot 60$$

$$= 0.02 = 20\text{mAmp}$$

$$I_R = \frac{V_{CC}}{R} = \frac{10}{10\times10^3} = 1\text{mA}$$



⇒ Design a free running UJT sweep wave[illegible] sweep amplitude of 6 volts, the sweep interval [illegible] is expected to be 3 msec with negligible Retrace interval, the slope error $e_s = 0.75$. Determine the values of R_{B1}, R_{B2}, V_{BB}, V_{yy}, R and C. Assume $V_v = 2$ volts

Given, $V_s = 6$ volts, $T_s = 3$ msec, $T_r = 0$ (negligible)

$e_s = 0.75$ $\quad V_v = 2V$

peak voltage $V_p = V_s + V_v$ $\quad V_p = 6 + 2 = 8V$

$V_s = V_p - V_v$

Calculation of V_{yy}

$V = V_{yy} - V_B$

$8 = V_{yy} - 2$

$V_{yy} = 10V$

$e_s = \frac{V_s}{V}$

$V = \frac{V_s}{e_s}$

$= \frac{6}{0.75}$

$\boxed{V = 8V}$

Calculation of V_{BB}:

$V_p = \eta \cdot V_{BB} + V_\gamma$

approximately $\boxed{\eta = 0.75}$

$8 = 0.75 V_{BB} + 0.7$

$\frac{8 - 0.7}{0.75} = \boxed{V_{BB}}$

$\boxed{V_{BB} = 9.73\,V} \simeq \boxed{V_{BB} = 10V}$

Sweep time

$T_s = RC \ln\left(\frac{1}{1-\eta}\right)$

$T_s = RC \ln\left(\frac{V_{yy} - V_v}{V_{yy} - V_p}\right)$

$3 \times 10^{-3} = RC \ln\left(\frac{10-2}{10-8}\right) = RC \ln\left(\frac{8}{2}^{4}\right)$

$3 \times 10^{-3} = Rc \ln(4)$

$\boxed{Rc = 2.164 \text{ mSec}}$

I_p – peak current

I_v – valley current

$$R_{max} = \frac{V_{BB} - V_P}{I_P}$$

$I_P \downarrow$ 2 μA (default)

$$R_{min} = \frac{V_{BB} - V_V}{I_V}$$

$I_V \downarrow$ 1 mA (default)

$$R_{max} = \frac{9.73 - 8}{2\mu A}$$

$9.73 \simeq 10$

$$R_{max} = \frac{10 - 8}{2 \times 10^{-6}}$$

$= 1 M\Omega$

$$R_{min} = \frac{10 - 2}{1 mA}$$

$\simeq 8 k\Omega$

$\therefore$ R value can be taken between 8 kΩ and 1000 kΩ

Thus $R = 100 k\Omega$

$100 k\Omega \times C = 2.164 \times 10^{-3}$

$$C = \frac{2.164 \times 10^{-3}}{100 \times 10^{-3}}$$

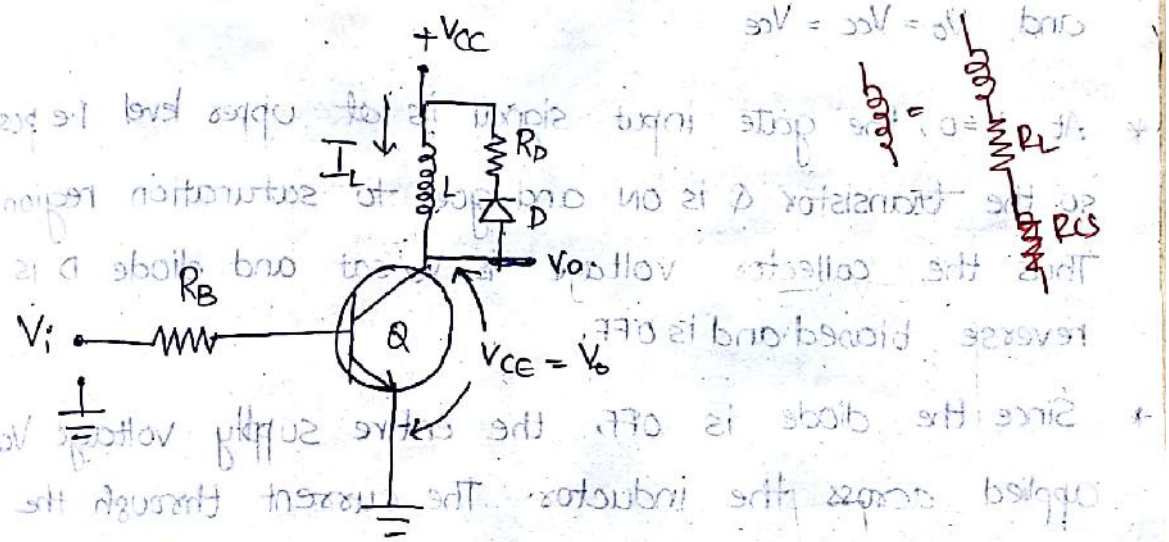
$\boxed{C = 21.6 \text{ nF}}$

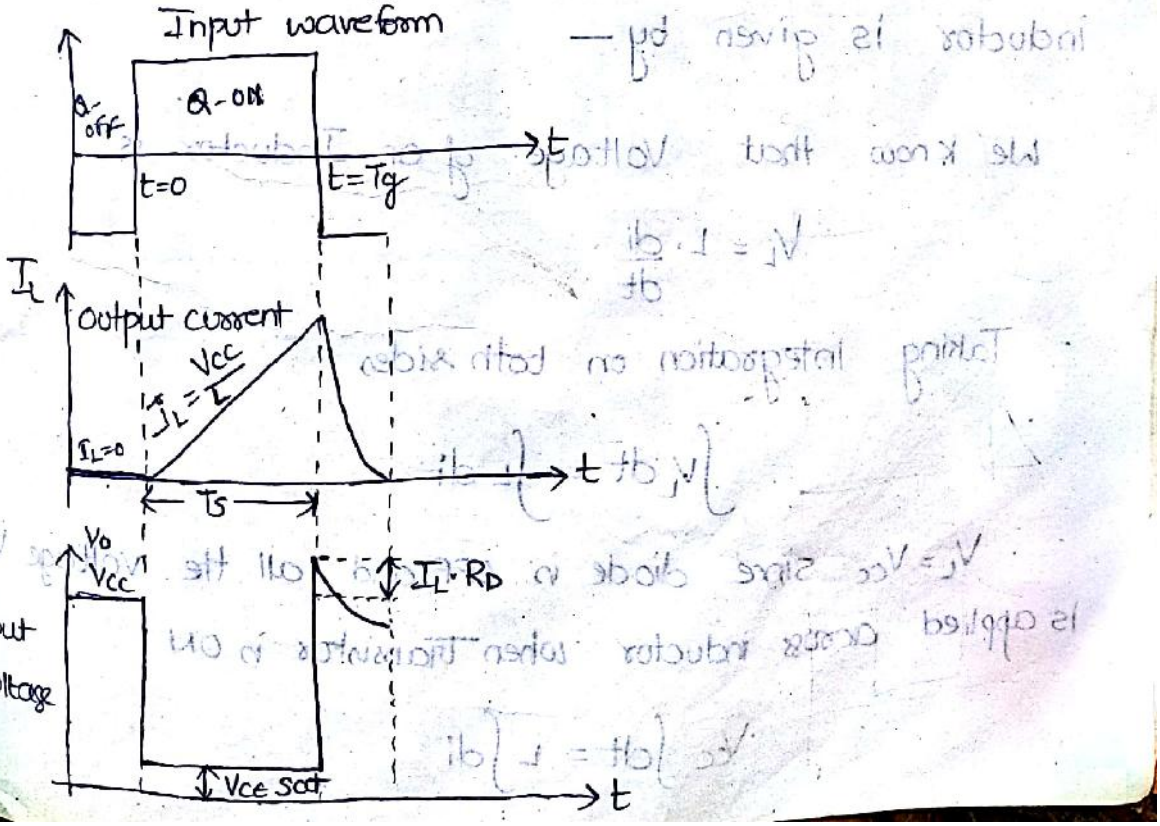
let $R_{B1} = 100\Omega$ and $R_{B2} = 100 k\Omega$

CURRENT TIME BASE GENERATOR

* Current Time base generator is one that provides output current waveform, a portion of which exhibits linear variation with respect to time.
* A linearly varying current waveform can be generated by applying a constant voltage across an inductor.
* Linearly varying current is required for magnetic deflection application.

SIMPLE CURRENT SWEEP CIRCUIT





CONSTRUCTION

* The transistor is used as switch and the inductor L in series with the transistor is bridged across supply voltage V_{cc}

OPERATION

* At $t<0$, the base of the transistor is at lower level (negative). So the transistor Q is OFF goes to CUTOFF region, the diode D is forward biased.
* Thus no current flows in the inductor i.e $I_L = 0$ and $V_o = V_{cc} = V_{ce}$
* At $t=0$, the gate input signal is at upper level i.e positive so the transistor Q is ON and goes to saturation region. Thus the collector voltage is $V_{ce\,sat}$ and diode D is reverse biased and is OFF.
* Since the diode is OFF, the entire supply voltage V_{cc} applied across the inductor. The current through the inductor is given by —

We know that Voltage of an Inductor is

$$V_L = L \cdot \frac{di}{dt}$$

Taking integration on both sides

$$\int V_L\,dt = \int L \cdot di$$

$V_L = V_{cc}$ since diode is OFF and all the voltage V_{cc} is applied across inductor when transistor is ON

$$V_{cc} \int dt = L \int di$$

$$I_L = \frac{V_{cc} \cdot (t)}{L}$$

at $t = T_s$

$$I_L = \frac{V_{cc}(T_s)}{L} \quad \text{---------- (2)}$$

i.e, the current increases linearly with time

* At $t = T_g$, the transistor is in CUTOFF and no current flows through it, the voltage at the collector raises abruptly to $V_{cc} + I_L \cdot R_D$ i.e there is a voltage spike at the collector
* At $t > T_g$, the inductor current decays exponentially to zero with time constant $\tau = \frac{L}{R_D}$
* The inductor L represents generally a physical yoke or choke
* Consider Yoke resistance as R_L and collector saturation resistance as R_{cs}, then the current increases in accordance with the following eq

$$I_L = \frac{V_{cc}}{(R_L + R_{cs})} \left[1 - e^{-[(R_L + R_{cs})/L]t}\right]$$

$$\boxed{I_L = \frac{V_{cc}}{R_L + R_{cs}} \left[1 - e^{-\frac{(R_L + R_{cs})}{L} \cdot t}\right]} \quad \text{---------- (1)}$$

Slope or Sweep Speed Error

$$e_s = \frac{\left.\frac{dI_L}{dt}\right|_{t=0} - \left.\frac{dI_L}{dt}\right|_{t=T_s}}{\left.\frac{dI_L}{dt}\right|_{t=0}}$$

Diff above eq (1) w.r.t t

$$\frac{dI_L}{dt} = \frac{V_{cc}}{R_L+R_{cs}}\left[0 - e^{\frac{-(R_L+R_{cs})}{L}\cdot t}\cdot(-1)\left(\frac{R_L+R_{cs}}{L}\right)\right]$$

$$\frac{dI_L}{dt} = \frac{V_{cc}}{R_L+R_{cs}}\left[e^{\frac{-(R_L+R_{cs})}{L}\cdot t}\cdot\frac{R_L+R_{cs}}{L}\right]$$

$$\frac{dI_L}{dt} = \frac{V_{cc}}{L}\, e^{-\left((R_L+R_{cs})/L\right)t}$$

At $t=0$ $\quad \left.\frac{dI_L}{dt}\right|_{t=0} = \frac{V_{cc}}{L}\left[e^{\frac{-(R_L+R_{cs})}{L}\cdot(0)}\right]$

$$= \frac{V_{cc}}{L}$$

At $t=T_s$ $\quad \left.\frac{dI_L}{dt}\right|_{t=T_s} = \frac{V_{cc}}{L}\left[e^{\frac{-(R_L+R_{cs})}{L}\cdot T_s}\right]$

$$\therefore e_s = \frac{\frac{V_{cc}}{L} - \frac{V_{cc}}{L}\left(e^{\frac{-(R_L+R_{cs})}{L}\cdot T_s}\right)}{\frac{V_{cc}}{L}}$$

$$= \frac{\frac{V_{cc}}{L}\left[1 - e^{\frac{-(R_L+R_{cs})T_s}{L}}\right]}{\frac{V_{cc}}{L}}$$

$$= 1 - e^{-\left(\frac{R_L+R_{cs}}{L}\right)T_s}$$

$$e^{-x} = 1 - \frac{x}{1!} + \frac{x^2}{2!} + \cdots$$

$$e_s = 1 - \left[1 - \frac{R_L+R_{cs}}{L}\cdot T_s + \frac{\left(\frac{R_L+R_{cs}}{L}\cdot T_s\right)^2}{2!} + \cdots\right]$$

Neglecting higher order terms, we get

$$\boxed{e_s = \left(\frac{R_L + R_{CS}}{L}\right) T_s}$$

W.K.T $\quad I_L = \frac{V_{CC} T_s}{L} \quad (\because ②)$

$$\frac{I_L \cdot L}{V_{CC}} = T_s$$

$$\left(\frac{R_L + R_{CS}}{L}\right)\left[\frac{I_L L}{V_{CC}}\right.$$

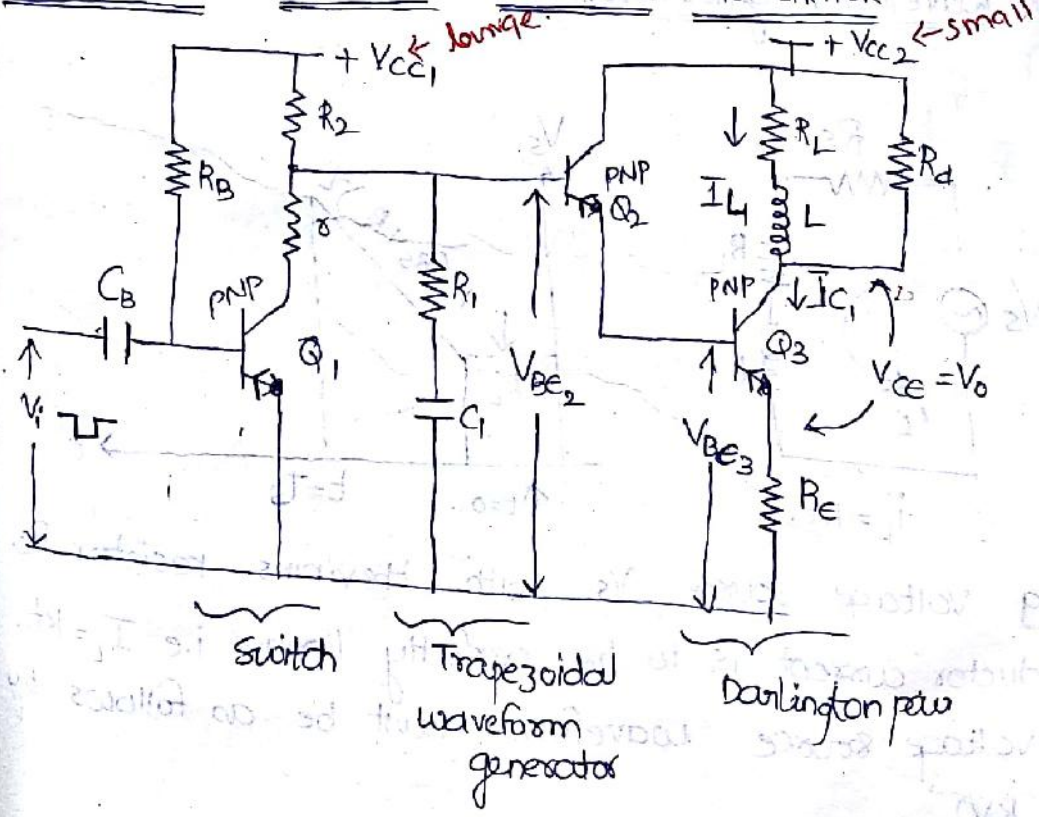
$$\frac{I_L}{V_{CC}} = \frac{T_s}{L}$$

$$\therefore \quad \boxed{e_s = (R_L + R_{CS})\left(\frac{I_L}{V_{CE}}\right)}$$

To maintain the linearity, the voltage across the total circuit i.e.,

$(R_L + R_{CS}) I_L$ must be kept small compared with V_{CC}

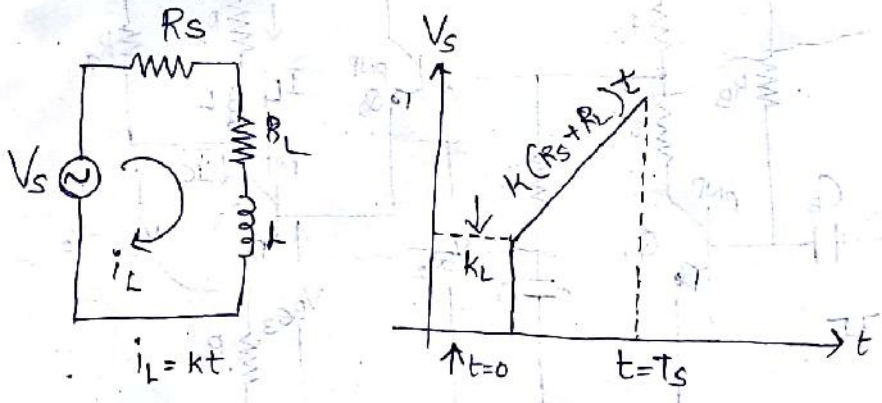
TRANSISTORISED CURRENT TIME BASE GENERATOR



CONSTRUCTION

* It consists of transistorised switch Q_1 followed by trapezoidal waveform generator (R_2, R_1, C_1).
* Transistors Q_2 and Q_3 are connected as Darlington pair to increase the input impedance
* The emitter resistor R_E introduces negative current feedback into the output state and thereby improves the linearity
* The Transistor Q_3 is common emitter circuit with R_E unbypassed resistance, this reduces the non linearity and collector current I_C responds linearly.
* Thus the linearity time varying current is obtained
* For having best linearity, R_E must be selected as high as possible.
* If supply voltage V_{CC_2} is small and V_{CC_1} is large then linearity is produced (ramp)

Trapezoidal Waveform generation:



* The driving voltage source Vs with thevinins resistor R_s if the inductor current is to be perfectly linear i.e $I_L = kt$, then the voltage source waveform must be as follows by applying KVL

$$V_S = I_L \cdot R_S + I_L \cdot R_L + L \cdot \frac{dI_L}{dt}$$

$$V_S = Kt \cdot R_S + KtR_L + L \cdot \frac{dKt}{dt}$$

$$V_S = Kt(R_S + R_L) + L \cdot K$$

$$V_S = KL + K(R_S + R_L)t$$

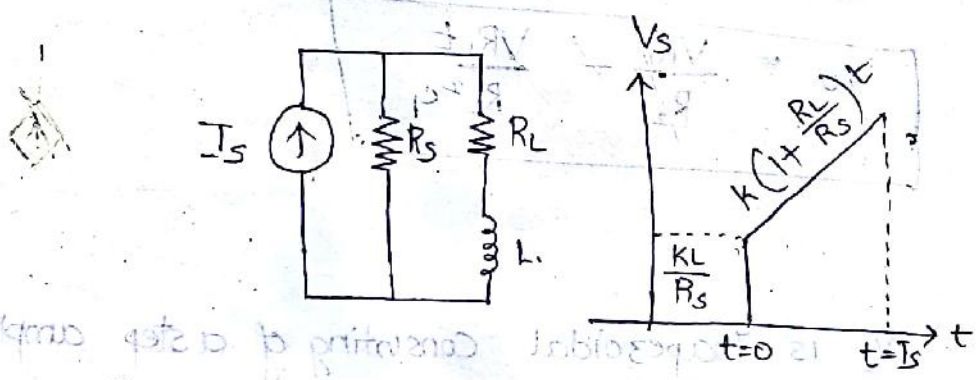
$$V_S = K\left[L + (R_S + R_L)t\right]$$

* This supplied voltage waveform consists of step (and its amplitude is KL) followed by a ramp (amplitude is $K(R_S+R_L)$] such a waveform is called as trapezoidal waveform.

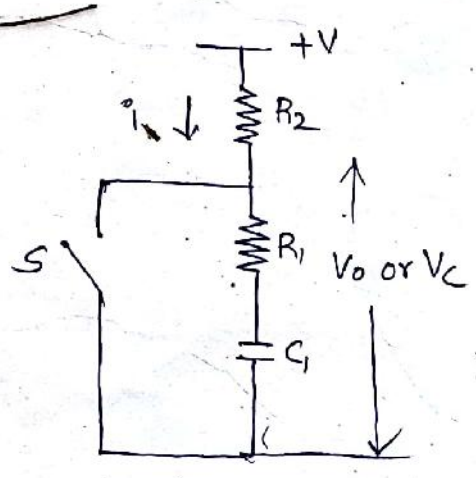
* If the voltage source V_S in series with resistance R_S is replaced by a current source I_S in parallel with resistance R_S is given by $I_S = \frac{V_S}{R_S} = \frac{KL + K(R_S+R_L)t}{R_S}$

$$\boxed{I_S = \frac{KL}{R_S} + K\left[1 + \frac{R_L}{R_S}\right]t}$$

i.e



MODIFIED SWEEP CIRCUIT FOR GENERATING TRAPEZOIDAL WAVEFORM



A Resistor R_1 in series with C, to generate a trapezoidal voltage, waveform if the switch S is open at t=0

$V_0 + iR_2 = V$

* The output voltage $V_0 = V - iR_2$ where $i = \frac{V}{R_1+R_2} \cdot e^{-t/(R_1+R_2)C}$

$$i = \frac{V}{R_1+R_2}\left(1 - \frac{t}{(R_1+R_2)C_1} + \frac{1}{2!}\left[\frac{t}{(R_1+R_2)C_1}\right]^2 - \cdots\right)$$

But $V_0 = V - iR_2$

$$= V - \frac{VR_2}{R_1+R_2}\left(1 - \frac{t}{(R_1+R_2)C_1} + \frac{1}{2!}\left[\frac{t}{(R_1+R_2)C_1}\right]^2 - \cdots\right)$$

$$= \frac{VR_1}{R_1+R_2}\left[1 - \frac{t}{(R_1+R_2)C_1} + \frac{t^2}{2(R_1+R_2)^2C_1^2} - \cdots\right]$$

$\frac{VR_1 + VR_2}{R_1+R_2}$

$R_2 >>> R_1$ and $R_1 + R_2 \simeq R_2$

$$V_0 = \frac{VR_1}{R_2}\left[1 - \frac{t}{R_2C_1} + \frac{t^2}{2R_2^2C_1^2} - \cdots\right]$$

$$\boxed{V_0 = \frac{VR_1}{R_2} - \frac{VR_1 t}{R_2^2 C_1}}$$

V_0 is trapezoidal consisting of a step amplitude $\frac{VR_1}{R_2}$ o which superimposed by a ramp of slope $\frac{VR_1}{R_2^2C_1}$

— * —