అమ్మ

Unit - 3

Bipolar Junction Transistor

Syllabus: Transistor construction - BJT operation - BJT symbol - Transistor amplifying action - Common Emitter configuration, Common Base and Common Collector configurations - Limits of operation - BJT Specifications.

Introduction:

On 23rd December, 1947, William Shockley, Walter H. Brattain, John Barden invented "Transistors" in Bell Laboratory. A Semiconductor device that can amplify electronic signals such as Radio and Television signals.

Before Transistors Vaccuum tubes were used as an amplifier. They are being used even now in microwaves in microfrequencies and in micro oscillators.

Now a days vaccum tubes are replaced by Transistors because of following Advantages of Transistors.

Advantages of Transistors:

* Small Size.
* Less weight.
* Low Cost.
* Rugged construction
* No heat loss.
* Higher Efficiency.
* Power observed by device is less.
* Low Operating voltages are possible.
* Does not require any filament power.

Applications of Transistors:

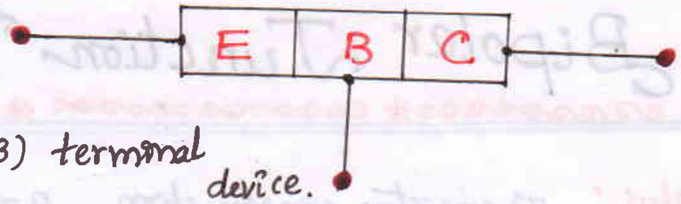
Transistors are used in

→ Amplifiers.

→ Oscillators.

→ Switching Circuits.

Transistor :



→ Transistor is a three (3) terminal device.

ie Emitter, Base, Collector.

* It can be operated in 3 configurations Common base, Common Emitter & Common Collector.

* According to configuration it can be used for voltage as well as current amplification.

* The input signal of a small amplitude is applied at the base to get the magnified output signal at the collector. Thus provides an amplification of the signal.

* The amplification in the transistor is achieved by passing input current signal from a region of low resistance to a region of high resistance.

This concept of transfer of resistance has given the name "TRANSISTOR".

In transistor, the output current is controlled or the input current & hence It is a "Current Controlled Device".

Types :

There are two types of Transistors.

1. Unipolar Junction Transistor. (UJT).
2. Bipolar Junction Transistor (BJT).

In UJT the current conduction is only due to one type of carriers ie Majority carriers.

In BJT the current conduction is because of bothe the types of charge carriers, holes & Electrons.

Hence It is called Bipolar Junction Transistor.

It is also of two types.
1. n-p-n type.
2. p-n-p type.

ie In Transistor an opposing type of semiconductor material is sandwitched between two same type of semiconductor materials.

Emitter :

→ Emitter emits charge carriers either p or n.

→ It must be heavily dopped compared to base & collector.

→ The emitter region is moderate. ie The size is moderate.

→ It emitts holes in pnp & electrons in npn.

Base :

→ It is the region between emitter and Collector.

→ It is n-type in pnp and p-type in npn transistor.

→ It is Lightly dopped.

→ It is very thin compared to E & C.

→ The charge carriers emitted by the emitter must travel through the base to reach collector.

→ The base material is opposite of both Emitter & Collector.

→ To avoid the recombination of charge carriers emitted by the Emitter the base is lightly dopped.

→ The base section is very thin to make the charge carriers emitted by Emitter to recide or Cross base region in a short time, again to reduce the recombination.

Collector :

→ Collector is the region where the charge carriers which have been emitted by the emitter are collected.

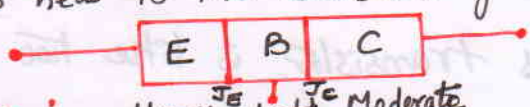
→ Collector & Emitter are of same type materials.

→ Collects holes in pnp, collects electrons in npn.

→ Collector is Moderately dopped.

→ Collector region is wide or large compared to B & E. Since the collector collects the same type of charge carriers.

→ In collector because of the collision of charge carriers heat will be generated. To decepate this heat to the surroundings the collector region is made large.



J_E - Emitter Junction

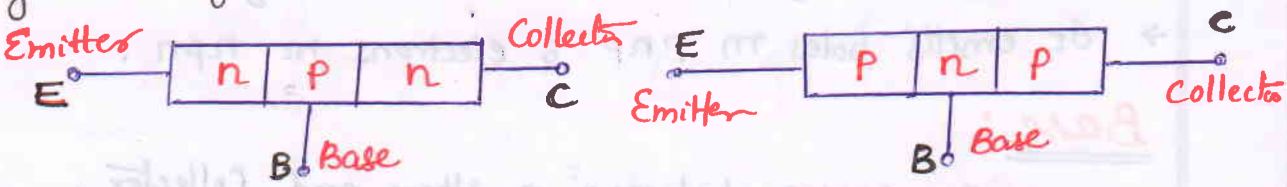
J_C - Collector Junction

i.e.

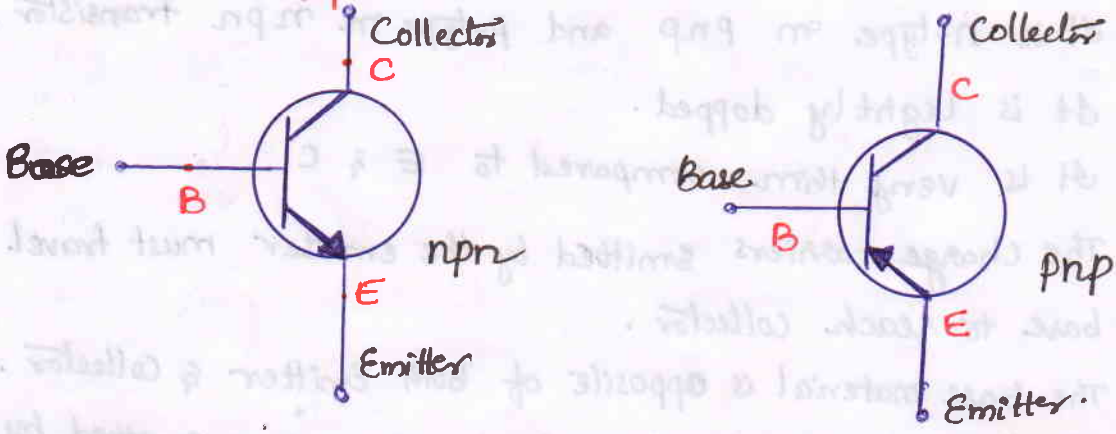
	E	B	C
dopping :	Heavy	Light	Moderate
Size :	Moderate	Small	Large

Symbol of Transistor :

When a transistor is formed by sandwiching a single p-region between two n-regions → n-p-n type Transistor. and A single n-region between two p-regions → p-n-p-type Transistor.

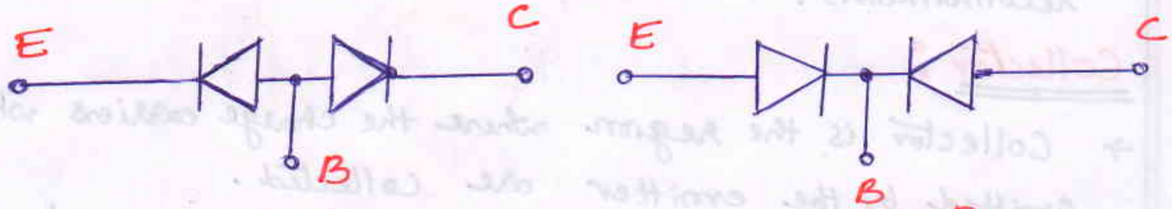


(a) n-p-n (b) p-n-p



ie Base is drawn ⊥r to a line, Emitter, Collector must be drawn as slanted lines touching the reference line.

The Emitter & Collector must be distinguished by placing an arrow on the emitter. The arrow indicates the flow of conventional current.



a) npn b) p-n-p

A Transistor has two p-n junctions

1. Junction between the Emitter and the base called Emitter base junction or simply the "Emitter Junction" 'J_E'.
2. Junction between the base and the collector called collector-base junction or simply the "collector junction" 'J_C'.

Thus transistor is like two pn junction diodes connected back-to-back as shown in above.

Biasing of Transistor :

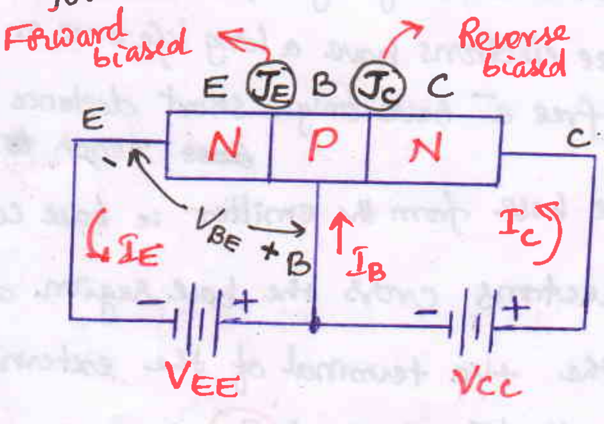
In order to operate transistor properly, it is necessary to correctly bias the two pn junctions with external voltages. Depending upon external bias voltage polarities used, the transistor works in one of the three regions. ie

1. Active region.
2. Cut-off region
3. Saturation region.

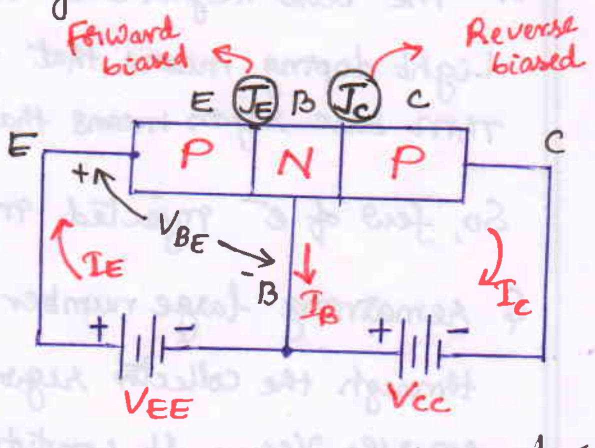
SL NO	Emitter Junction	Collector Junction	Region (Name)	Application.
1.	Forward biased	Forward biased	Saturation Region	ON Switch
2.	Forward biased	Reverse biased	Active region	Amplifier
3.	Reverse biased	Reverse biased	Cutoff region	OFF-Switch
4.	Reverse biased	Forward biased.	Inverted region	Not recommended.

ie Transistor should not be biased in the inverted region otherwise the transistor gets damaged.

To bias the transistor in its active region, the Emitter base junction is forward biased while the collector-base junction in reverse biased.



a) npn transistor



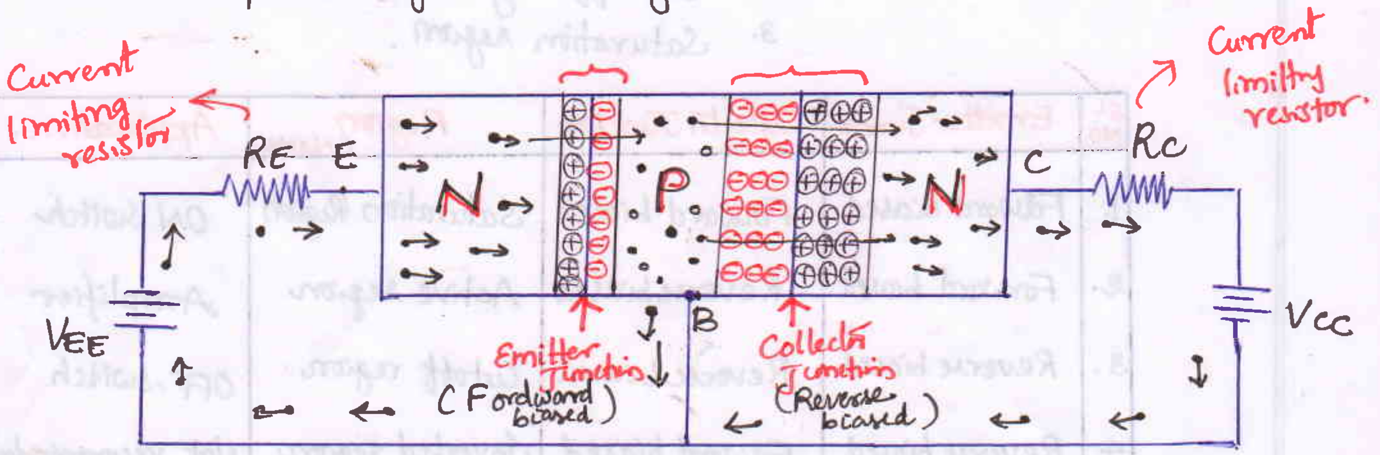
b) p.n.p transistor.

where V_{EE} & V_{CC} are the externally applied bias voltages.

The operation of the pnp & npn is same except that the roles of the electrons & holes, the bias voltage polarities and the current directions are all reversed. In both cases the Emitter junction J_E is in forward biased & collector junction J_C is reversed biased.

Operation / Working of a Transistor :

NPN Transistor: The base to Emitter junction is forward biased by the d.c source V_{EE}. Thus the depletion region at this junction is reduced. The collector to base junction is reverse biased by the d.c source V_{CC}. Thus the depletion region at this junction is increased.



The forward biased Emitter base junction causes the electrons in the n-type Emitter to flow towards the base. This constitutes the Emitter current (I_E). As these electrons flow through the p-type base, they tend to combine with holes in p-region (base).

* The base region is very thin and lightly doped.

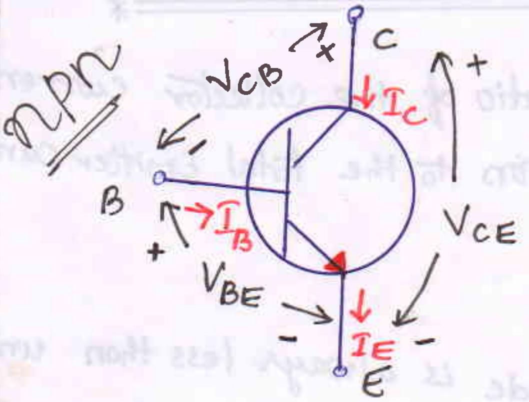
Light doping means that the free electrons have a long life time in base region. Thin base region means that the free e^- have only a short distance to go to ~~base~~ reach collector.

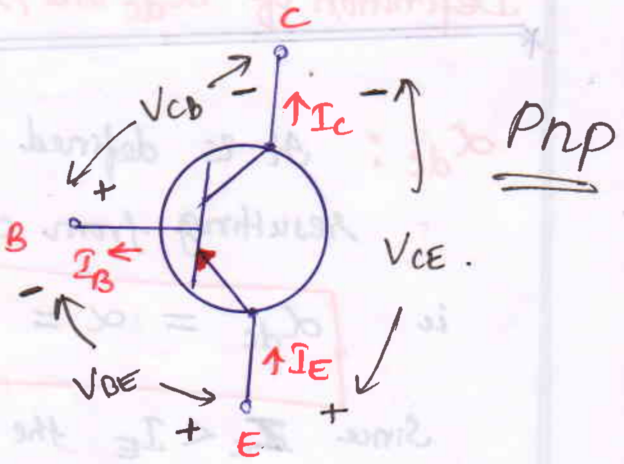
So, few of e^- injected into the base from the emitter ie base current (I_B). & remaining large number of electrons cross the base region and move through the collector region to the +ve terminal of the external dc source Vcc.. It constitutes Collector Current (I_C).

Thus The Electron flow constitutes the dominant current in an npn transistor. So, the collector current is larger than the base current.

PNP Transistor: Here V_{EE} & V_{CC} reversed from those in the npn transistor. The holes in the p-type to flow towards the base & then to collector. Since the current results from electrons in pnp transistor. or from holes in npn transistor.

Transistor Voltages & Currents :





Apply KVL for npn & pnp

$V_{CE} - V_{CB} - V_{BE} = 0$

(or) $\Rightarrow V_{BE} + V_{CB} - V_{CE} = 0$

$\therefore$ $V_{CE} = V_{BE} + V_{CB}$

where

V_{BE} - Base Emitter voltage

V_{CE} - Collector Emitter voltage

V_{CB} - Collector Base voltage.

&

Apply KCL for both npn & pnp.

Here
$V_{CE} = -V_{EC}$
$V_{BE} = -V_{EB}$
$V_{CB} = -V_{BC}$.

$I_E - I_C - I_B = 0$

(or) $-I_E + I_C + I_B = 0$

$\Rightarrow$ $I_E = I_C + I_B$.

where

I_E - Emitter current

I_C - Collector current

I_B - Base Current.

Explanation:

For an npn transistor, electrons are injected into the base. Assume 100 e^- (I_E) are injected into the base region, Since the base is very thin. So, very few of them say 2 in no, recombine with holes in Base. (I_B). The remaining electrons, 98 cross the base jun. & appear on the collector side. (I_C).

$I_E = I_B + I_C$.

Hence. Emitter Current (I_E) is always equal to the sum of the Base current (I_B) and Collector current (I_C).

Junction Voltages:

At 25°C

Sl No	Type	$V_{CE(sat)}$ (V)	$V_{BE(sat)}$ (V)	$V_{BE(act)}$ (V)	$V_{BE(cut\,in)}$ (V)	$V_{BE(cut\,off)}$ (V)
1	Si	0.3	0.7	0.6	0.5	0.0
2	Ge	0.1	0.3	0.2	0.1	-0.1

Definition of α_{dc} and β_{dc} & Relation b/w α_{dc} & β_{dc} :

α_{dc} : It is defined as the ratio of the collector current resulting from carrier injection to the total Emitter current.

ie $$\alpha_{dc} = \alpha = \frac{I_C}{I_E}.$$

Since $I_C < I_E$ the value of α_{dc} is always less than unity.

It ranges from 0.95 to 0.995.

α - represents the current gain in the CB-configuration.

β_{dc} : It is defined as the ratio of the collector current to the base current

ie $$\beta_{dc} = \beta = \frac{I_C}{I_B}.$$

where β represents the current gain in the CE configuration.

Relation : We know $\alpha_{dc} = I_C/I_E$ & $\beta_{dc} = I_C/I_B$.

& we have $I_E = I_C + I_B \Rightarrow I_B = I_E - I_C$.

$$\therefore \beta_{dc} = \frac{I_C}{I_E - I_C}$$

Dividing the Numerator & denominator of RHS by I_E we get

$$\beta_{dc} = \frac{I_C/I_E}{I_E/I_E - I_C/I_E} = \frac{\alpha_{dc}}{1-\alpha_{dc}} \quad \therefore \beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}}$$

$$\Rightarrow \beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}} \quad \text{(or)} \quad \beta = \frac{\alpha}{1-\alpha}.$$

Dividing the RHS & LHS by $(1+\beta_{dc})$ we get

$$\Rightarrow \frac{\beta_{dc}}{1+\beta_{dc}} = \frac{\alpha_{dc}/(1-\alpha_{dc})}{1+\beta_{dc}}$$

$$\Rightarrow \frac{\beta_{dc}}{1+\beta_{dc}} = \frac{\alpha_{dc}/(1-\alpha_{dc})}{1+\frac{\alpha_{dc}}{1-\alpha_{dc}}} \quad (\because \beta = \tfrac{\alpha}{1-\alpha}).$$

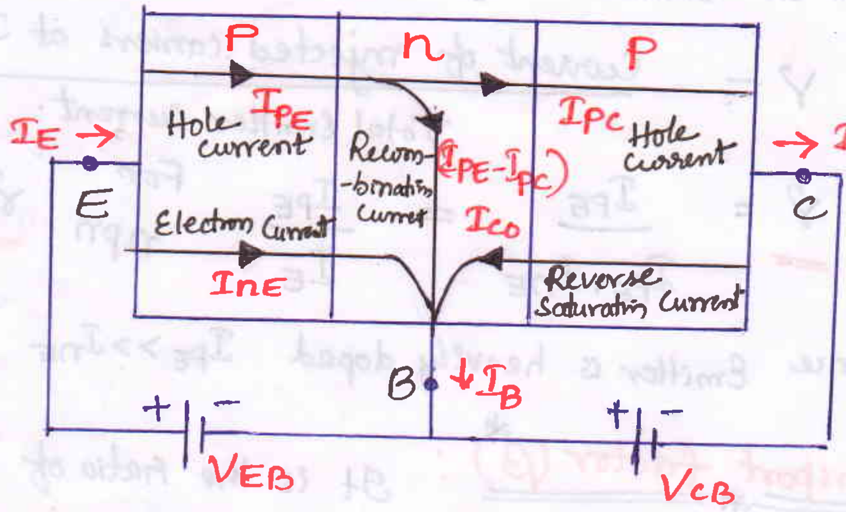
$$\Rightarrow \frac{\beta_{dc}}{1+\beta_{dc}} = \frac{\alpha_{dc}}{1-\alpha_{dc}+\alpha_{dc}} = \alpha_{dc}$$

$$\Rightarrow \alpha_{dc} = \frac{\beta_{dc}}{1+\beta_{dc}}$$

$$\text{(or)} \quad \alpha = \frac{\beta}{1+\beta}.$$

Transistor Current Components:

Consider the pnp transistor which flow across the forward biased Emitter base junction 'J_E' and the reverse biased collector base junction J_C.



where

I_{PE} - hole current (holes crossing from Emitter into base)

I_{nE} - Electron current (Electrons crossing from base into emitter)

I_{PC} - Collector Current (Holes crossing from J_E & reaching to J_C).

⇒ $$I_E = I_{PE} + I_{nE} \longrightarrow (1)$$

All components are +ve for pnp.

→ $(I_{PE} - I_{PC})$ is the recombination current which leaves the base.

$$I_B = (I_{PE} - I_{PC}) I_{nE} \longrightarrow (2)$$

⇒ $$I_C = I_{PC} - I_{CO} \longrightarrow (3)$$

where I_{CO} = Reverse saturation current / Leakage current.

when Emitter is open ckt'd ie $I_E = 0$. hence $I_{PC} = 0$. then I_C - Collector Current equals to the reverse saturation Current I_{CO}

$$I_C = I_{CO}$$

* The ratio of hole current (I_{PE}) to electron current (I_{nE}) crossing the Emitter junction is proportional to conductivity of p-type material to that of conductivity of the n-type material.

$$\therefore \frac{I_{PE}}{I_{nE}} \propto \frac{\text{Conductivity of p-type}}{\text{Conductivity of n-type}} = \frac{\sigma_P}{\sigma_n}.$$

Current Parameters :

Emitter Efficiency (γ) : It is the ratio of current of injected carriers at Emitter base junction 'J_E' to total Emitter Current.

ie
$$\gamma = \frac{\text{Current of injected carriers at } J_E}{\text{Total Emitter Current}}$$

For pnp $\gamma = \frac{I_{PE}}{I_{PE}+I_{nE}} = \frac{I_{PE}}{I_E}$ For npn $\gamma = \frac{I_{nE}}{I_E}$

Since Emitter is heavily doped $I_{PE} >> I_{nE}$ then $\gamma \cong 1$.

Transport factor (β^*) : It is the ratio of injected carrier current reaching at collector base junction J_C to injected carrier current at Emitter base junction J_E.

ie
$$\beta^* = \frac{\text{Injected carrier current reaching at } J_C}{\text{Injected carrier current at } J_E}$$

For pnp $\beta^* = \frac{I_{PC}}{I_{PE}} = \frac{I_C - I_{CO}}{I_B - (I_{nE} - I_{PC})} \cong \frac{\Delta I_C}{\Delta I_B}$

$\Rightarrow$ $\boxed{\beta^* = \frac{\Delta I_C}{\Delta I_B}}$

For npn $\beta^* = \frac{I_{nC}}{I_{nE}}$

Large Signal Current gain (α) : It is the ratio of -ve of collector current due to injected carriers to the total Emitter current.

$$\alpha = + \frac{I_{PC}}{I_E} = \frac{-(I_C - I_{CO})}{I_E} \text{ or } \boxed{\alpha = -\frac{\Delta I_C}{\Delta I_E}}$$

Since I_C & I_E have opposite signs. I_{CO} is very small neglect.

$\therefore$ α is always Positive. $I_C = \alpha I_E + I_{CO}$.

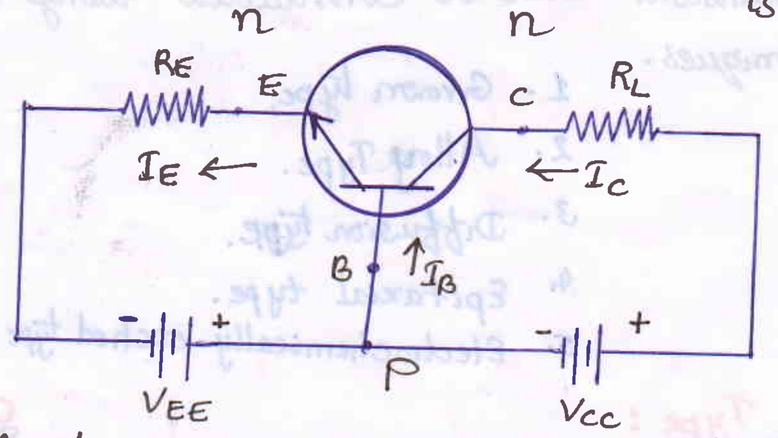
$I_E = I_B + I_C$, $\therefore I_E > I_C$, & $I_C > I_B$.

$\boxed{\alpha < 1}$ $\therefore$ $\boxed{I_E > I_C > I_B}$

$\boxed{\alpha = \beta^* \gamma}$ For both npn & pnp

Transistor acts as an Amplifier:

For Amplifier Emitter junction J_E is forward biased & Collector junction J_C is Reverse biased.



Consider the transistor npn circuit, Here the load resistance R_L is in Series with the collector supply voltage V_{CC}.

We know that Current amplification factor for CB configuration.

$$\alpha = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}} \Rightarrow \Delta I_C = \alpha \Delta I_E \rightarrow (1)$$

at Constant Collector to base voltage.

Multiply both sides of above eqn by R_L

$$\Delta I_C \cdot R_L = \alpha \cdot \Delta I_E \cdot R_L$$

$$\Delta V_0 = \alpha \Delta I_E \cdot R_L \rightarrow (2) \quad (\because V_0 = I_C \cdot R_L)$$

& We know that

$$V_i = r_e \cdot I_E$$

where r_e - dynamic resistance of Emitter junction J_E or input resistance of the transistor.

$$\Rightarrow \Delta V_i = r_e \cdot \Delta I_E. \Rightarrow \Delta I_E = \frac{\Delta V_i}{r_e} \rightarrow (3)$$

From eqn (1) & (3) $\Delta I_C = \alpha \cdot \frac{\Delta V_i}{r_e}$ &

From eqn (2) & (3)

$$\Delta V_0 = \alpha \cdot \frac{\Delta V_i}{r_e} \cdot R_L$$

$$\text{let } A_V = \frac{\Delta V_0}{\Delta V_i} = \frac{\alpha \cdot R_L}{r_e} \rightarrow (4) \quad (\because A = \frac{V_0}{V_i})$$

where A_V - voltage gain or Amplification. $\therefore A_V = \alpha \cdot \frac{R_L}{r_e}$

From eqn (4). α of the transistor is less than 1 r_e is also Low, If R_L is greater than r_e then $A_V >> 1$ ie $\Delta V_0 >> \Delta V_i$.

ie The current in the low resistance input ckt is transferred to the high impedance output circuit.

Hence R_L is selected Such that $R_L >> r_e$ then the transistor will work as an Amplifier. ie $\Delta V_0 >> \Delta V_i$.

Transistor Construction :

The transistor can be constructed using one of the following basic techniques.

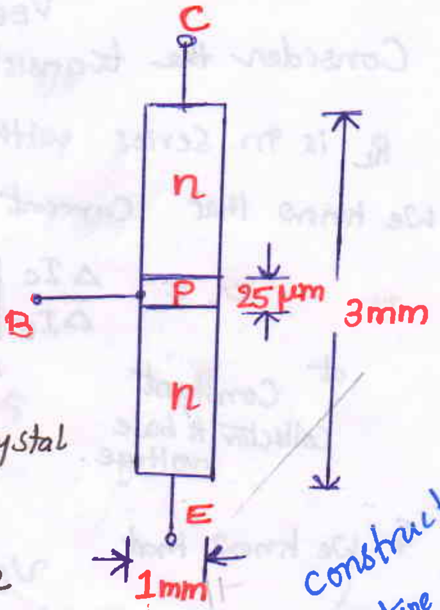
1. Grown type.
2. Alloy Type.
3. Diffusion type.
4. Epitaxial type.
5. Electrochemically etched type.

1) Grown Type :

→ It is used to form the two p-n junctions of a grown-junction transistor.

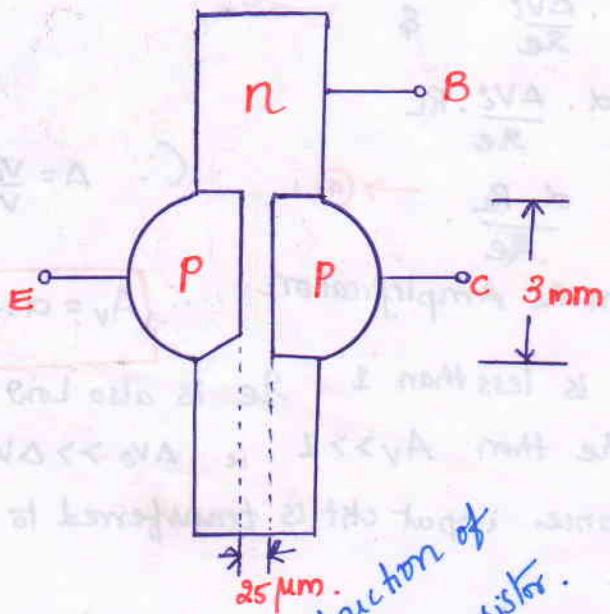
→ Here a single crystal is drawn from a melt of Si or Ge whose impurity concentration is changed during the crystal drawing operation.

→ Crystal decides the base width and the doping levels of the n and p-type materials.



Construction of Grown type Transistor.

2) Alloy Type :



Construction of Alloy Type Transistor.

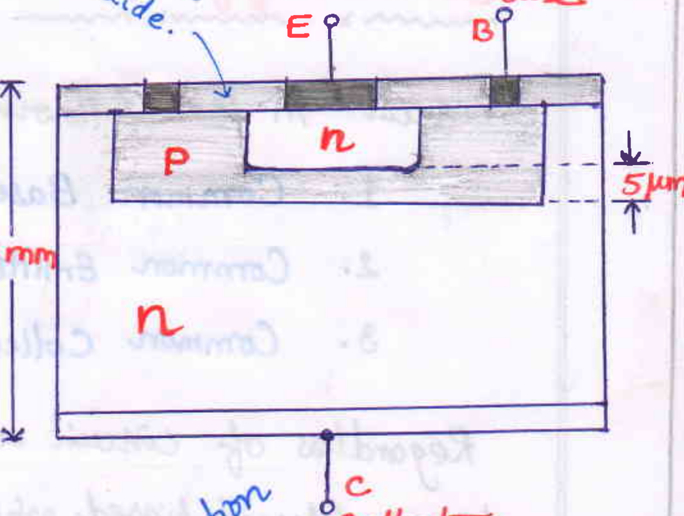
→ It is also known as fused construction.

→ Here the center (base) section is a thin wafer of n type material.

→ Two small dots of indium are attached to opposite sides of the wafer. & the whole structure is raised for a short time to a high temperature, above the melting point of the indium but below that of Ge.

→ The collector is made larger than Emitter to withstand the heavy current. & power dissipation.

3) Diffusion Type :



Construction of Diffusion type Transistor.

→ The most frequently employed method of manufacturing transistors today is the diffusion technique.

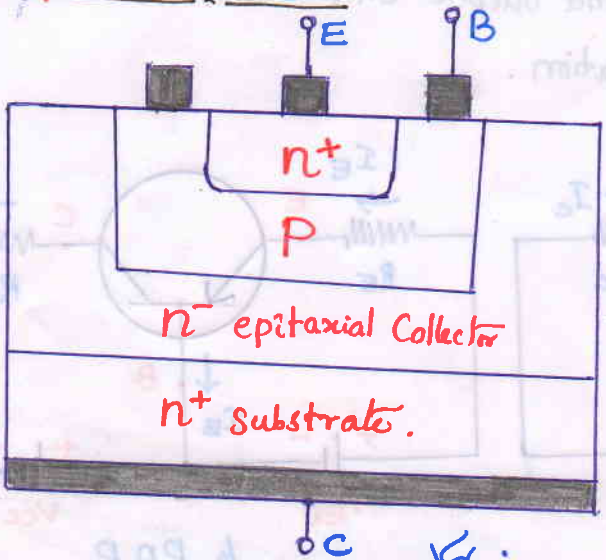
→ It requires more time than the alloy type process but it is relatively inexpensive and can be very accurately controlled.

→ Diffusion is a process by which a heavy concentration of particles will diffuse into a surrounding region of lesser concentration.

→ Here heat is applied in the diffusion only to increase the activity of the elements involved.

* The base-collector junction area is determined by a diffusion mask. Emitter is diffused on the base and a layer of silicon oxide. It aviodes most surface problems & very low leakage current also improves current gain at low currents & the noise figure.

4) Epitaxial Type :



Construction of Epitaxial type Transistor.

→ The term Epitaxial has its derivation from the Greek words. 'Epi' means "upon" and 'taxis' meaning "arrangement".

→ Here a very thin, high purity, single crystal layer of Si or Ge is grown on a heavily doped substrate of the same material.

→ This augmented crystal forms the collector on which the base and emitter may be diffused.

5) Electrochemically Etched Type :

It is also referred as Surface-barrier Transistor. Such devices are no longer of commercial importance.

BJT Configurations :

The transistor can be connected in a circuit in the following three configurations.

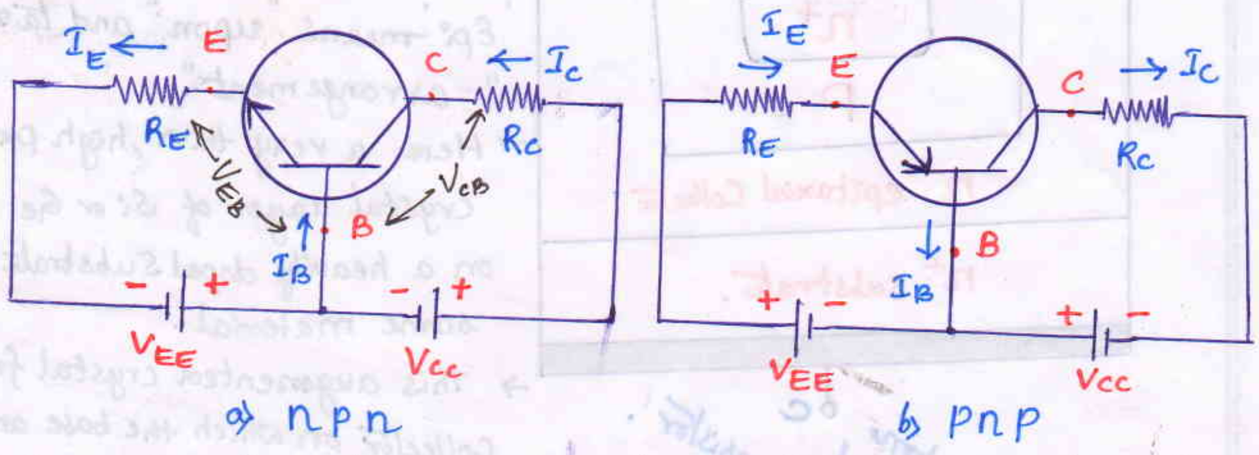
1. Common Base Configuration.
2. Common Emitter Configuration.
3. Common Collector Configuration.

Regardless of circuit configuration, the base Emitter junction is always forward biased while the collector-base junction is always reverse biased, to operate transistor in active region.

* The various currents and voltages relationships can be plotted graphically which are commonly known as the " Characteristics of transistor". The most important charatteristics of transistor in any configuration are input & Output Characteristics.

① Common Base Configuration:

Here input is applied between Emitter and base & Output is taken from the Collector and base. The base of the transistor is common to both input and output ckts and Hence the name Common Base Configuration.



Since the transistor is a three terminal device when a transistor is to be connected in any ckt & System. We need 2 terminals 2 for input, 2 for output. This difficulty may be overcome by making any one lid of transistor common to both input & Output Circuit.

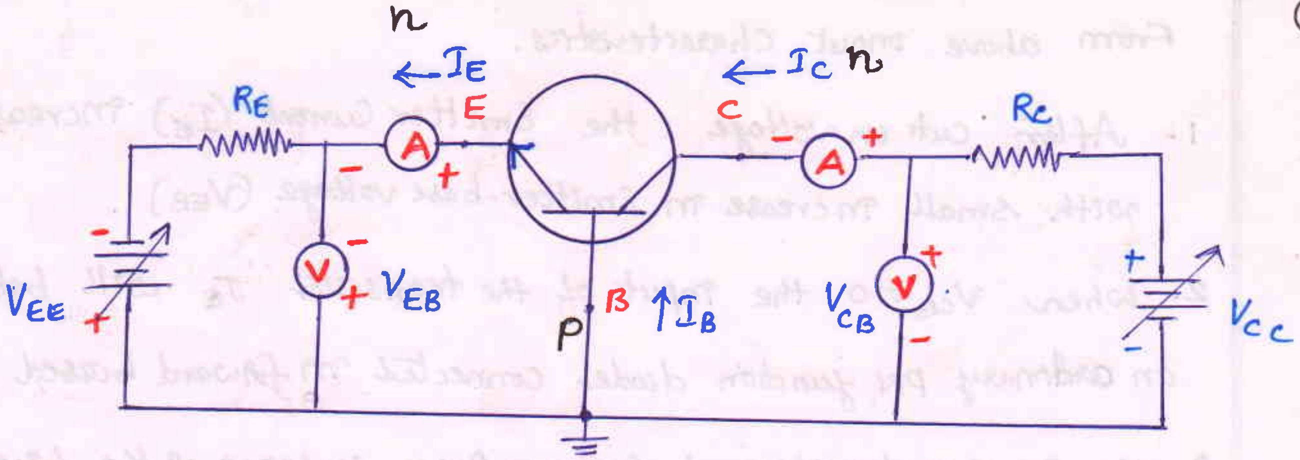


Fig: Ckt to determin CB Static Characteristics.

Circuit Description :

* Base is grounded, Emitter is input, Collector is output.
  V_{EE} → input circuit, V_{CC} → Output Circuit.

Amplification factor $(\alpha) = \dfrac{\text{Change in output current}}{\text{Change in input Current}} = \dfrac{\Delta I_C}{\Delta I_E}$.

Output Current Expression $I_C = -(\alpha I_E + \text{leakage Current})$

$$I_C = -(\alpha I_E + I_{CBO})$$

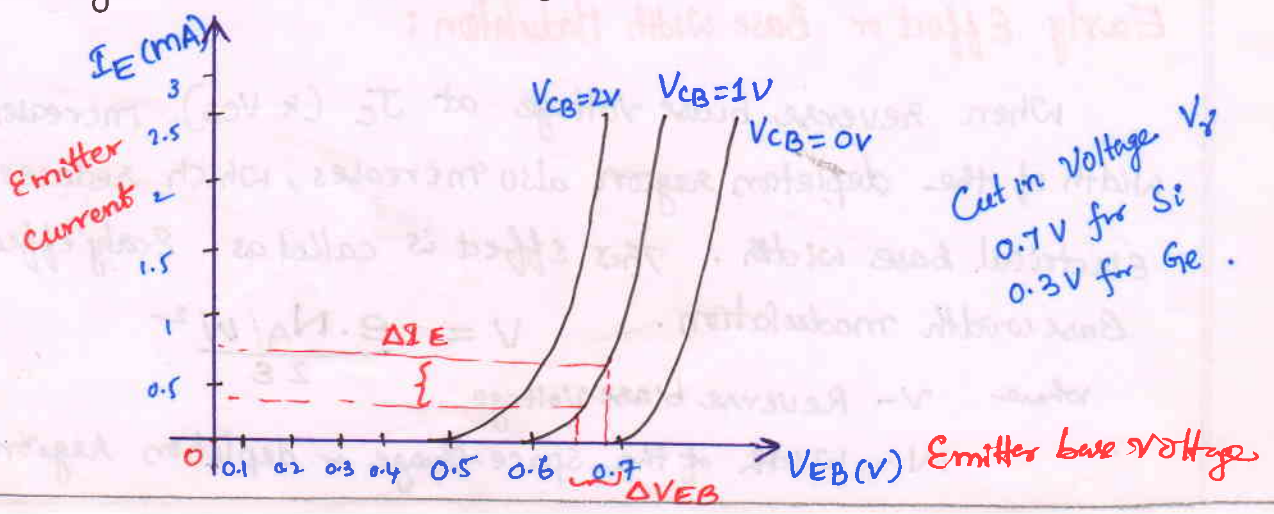
where I_{CBO} is leakage current ie Collector to base current when emitter is open ckted ie.

$$I_C = -(\alpha I_E + I_{CO}(e^{V/\eta V_T} - 1))$$

↳ Reverse Saturation Current.

Input Characteristics :

It is the curve between input current I_E (Emitter Current) and input voltage V_{EB} (Emitter Base voltage) at constant collector-base voltage V_{CB}. ie V_{EB} Vs I_E at V_{CB} constant.



From above input characteristics.

1. After cut in voltage, the Emitter Current (I_E) increases rapidly with small increase in Emitter-base voltage (V_{EB}).

2. When $V_{CB} = 0$ the input of the transistor 'J_E' will behave like an ordinary PN junction diode connected in forward biased region.

3. The i/p characteristics of Common Base is same as the forward bias pn junction diode characteristics.

4. As V_{CB} increases the effective width of the base reduces, recombination of charge carriers decreases ie more no-of charge carriers are available for conduction. Hence current conduction at J_E takes place for lesser voltage.

ie As V_{CB} increases V_{EB} decreases and I_E increases.

Input Impedance: The ratio of change in Emitter base voltage (ΔV_{EB}) to the resulting change in Emitter current (ΔI_E) at constant Collector-base voltage (V_{CB}).

It is also known as dynamic input resistance of the transistor.

$$r_i = \frac{\Delta V_{EB}}{\Delta I_E}\Bigg|_{V_{CB} = \text{constant}}$$

ie

The input resistance of Common Base is very low in the order of 10's of Ohms.

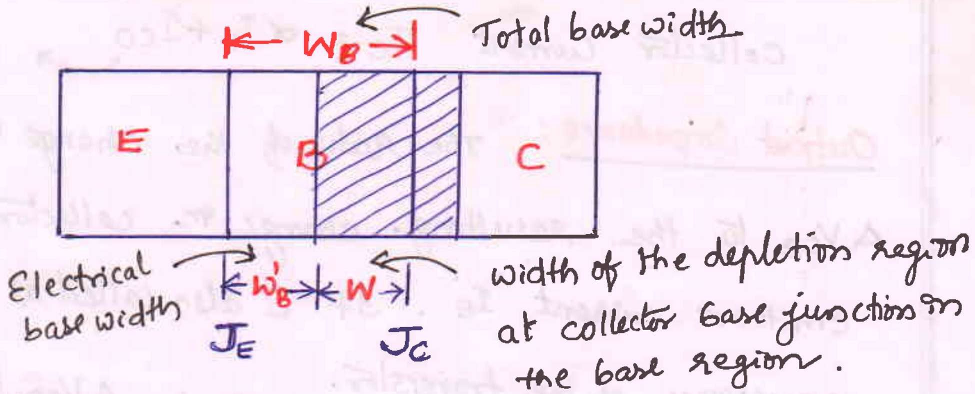
Early Effect or Base Width Modulation:

When reverse biase voltage at J_C (ie V_{CB}) increases, the width of the depletion region also increases, which reduces the electrical base width. This effect is called as Early effect or Base width modulation.

$$V = \frac{e \cdot N_A \cdot W^2}{2\varepsilon}$$

where V - Reverse biase voltage.

W - Width of the space-charge or depletion region.



ie For decrease in base width

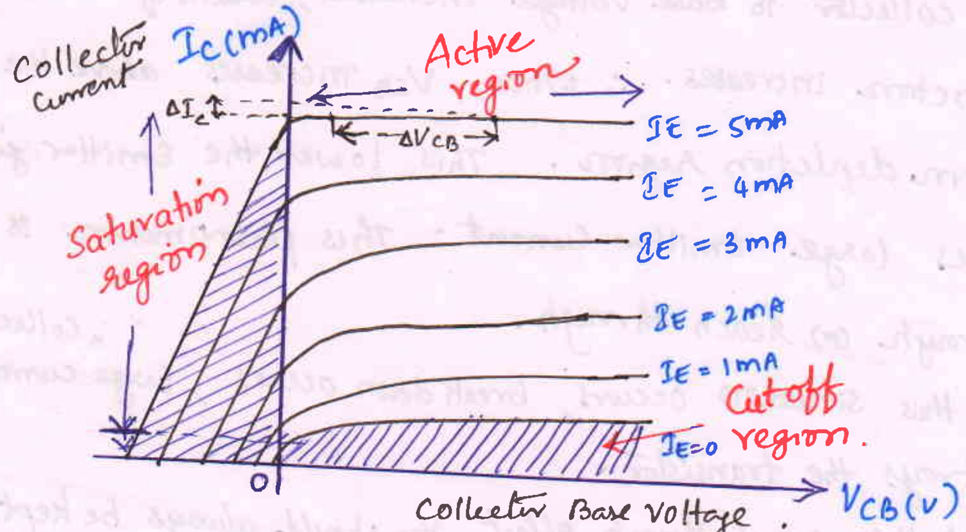
* There is a less chance for recombination within the base region. Hence the transport factor β^* & also α increases with an increase in magnitude of the collector junction voltage.

* The charge gradient is increased within the base & The mean life time of the charge carrier also increases. Due to the above the current of minority carrier injected across the junction increases.

Output Characteristics :

It is the curve between collector current 'I_C' and collector base voltage 'V_{CB}' at constant Emitter Current 'I_E'.

ie V_{CB} Vs I_C at Constant I_E.



The output characteristics has 3 basic regions: Active, Cut-off & Saturation

1. **Active Region :** Here the Emitter junction is forward biased & Collector junction is reverse biased. In this region I_C is equal to I_E and transistor works as an amplifier.

Collector current $I_C = \alpha I_E + I_{CO}$ → leakage current.

Output Impedance: The ratio of the change in collector base voltage ΔV_{CB} to the resulting change in collector current ΔI_C at constant Emitter current I_E. It is also called as Dynamic output resistance of the transistor. It is high value order of 100's of kΩ.

$$R_O = \left.\frac{\Delta V_{CB}}{\Delta I_C}\right|_{I_E = \text{constant}}$$

2. **Saturation region:** In this region the Emitter base junction and Collector-base junctions are both forward biased. Here the characteristics which is to the left of $V_{CB}=0$ and above the $I_E=0$.

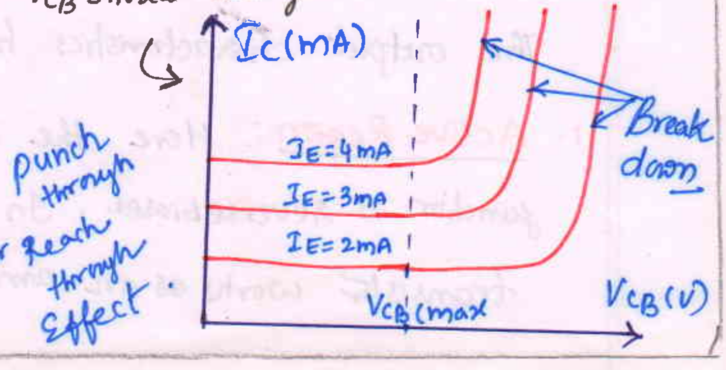
8) The Exponential increase in collector current as the voltage V_{CB} increases towards 0.V.

3 **Cut off Region:** The region below the curve $I_E=0$ is known as cut-off region. where the Collector current is nearly zero and the both Emitter base junction & Collector-base junction are reverse biased.

Punch-through (or) Reach through effect: In the active region, when the collector to base voltage increases, width of the depletion region at the junction increases. ∴ When V_{CB} increases above the $V_{CB(max)}$, increase in depletion region. This lower the Emitter junction voltage and causes large Emitter current. This phenomenon is called as Punch through (or) reach-through.

When this situation occurs, break down occurs, large collector current flows which destroys the transistor.

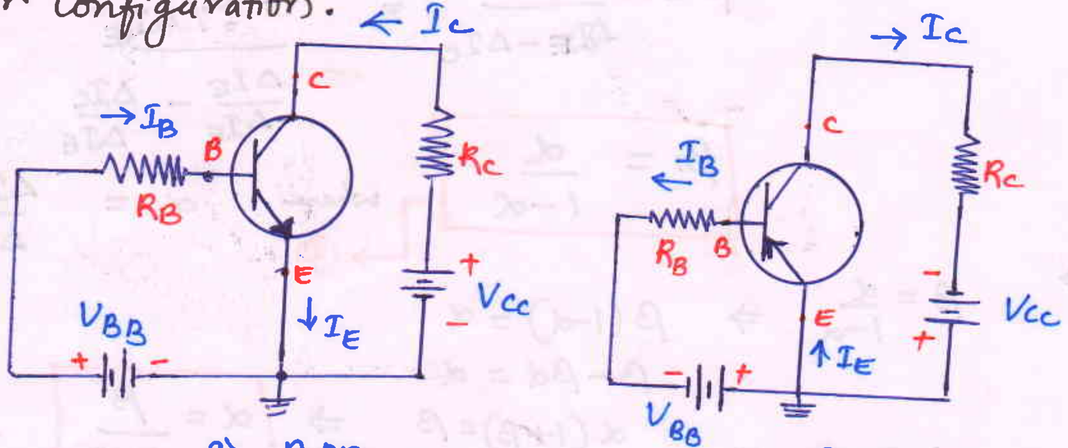
To avoid this punch through effect V_{CB} should always be kept below values



Botaming: The voltage will fall near to the bottom value. Hence This phenomenon is called Botaming.

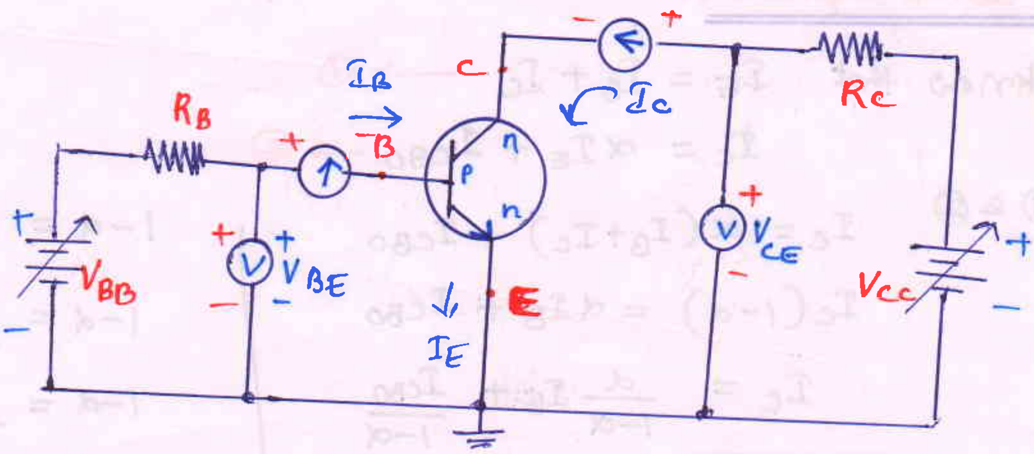
Common Emitter (CE) Configuration:

Here An input is applied between base and Emitter & Output is taken from Collector and Emitter. So, Emitter of the transistor is common to both input & output ckt hence the name Common Emitter configuration.



a) npn b) pnp

The bias voltage V_{BB} forward biases the base emitter junction and V_{cc} is used to reverse bias the collector Base junction.



Circuit Description:

Emitter is grounded, Base is input & Collector is output.

$V_{BB} \rightarrow$ Input ckt, $V_{cc} \rightarrow$ Output ckt.

Amplification factor (β) = $\dfrac{\text{Change in Collector current (o/p)}}{\text{Change in base Current (i/p)}}$

$$\therefore \beta = \frac{\Delta I_c}{\Delta I_B}.$$

A Voltmeter 'V_{BE}' connected b/w V_{BB} & V_{cc}.

[PTO]

Expression for β in terms of α :

We know that $I_E = I_B + I_C$

$$\beta = \frac{\Delta I_C}{\Delta I_B} \rightarrow (1)$$

$$\Delta I_E = \Delta I_B + \Delta I_C$$

$$\Delta I_B = \Delta I_E - \Delta I_C \rightarrow (2)$$

From (1) & (2)

$$\beta = \frac{\Delta I_C}{\Delta I_E - \Delta I_C} = \frac{\Delta I_C / \Delta I_E}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}}$$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}} \rightarrow (3)$$

where $\alpha = \frac{\Delta I_C}{\Delta I_E}$.

$\Rightarrow \beta = \frac{\alpha}{1-\alpha} \Rightarrow \beta(1-\alpha) = \alpha$

$$\beta - \beta\alpha = \alpha$$

$$\alpha(1+\beta) = \beta \Rightarrow \boxed{\alpha = \frac{\beta}{1+\beta}} \rightarrow (4)$$

From eqn (3). It is observed that $\beta > 1$.

From eqn (4). It is observed that $\alpha < 1$.

Output Current Expression:

We know that $I_E = I_B + I_C \rightarrow (1)$

$$I_C = \alpha I_E + I_{CBO} \rightarrow (2)$$

From (1) & (2)

$$I_C = \alpha(I_B + I_C) + I_{CBO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha}$$

$$\boxed{I_C = \beta I_B + I_{CBO}(1+\beta)} \rightarrow (3)$$

$$1-\alpha = 1 - \frac{\beta}{1+\beta}$$

$$1-\alpha = \frac{1+\beta-\beta}{1+\beta}$$

$$1-\alpha = \frac{1}{1+\beta}$$

$$\Rightarrow \frac{1}{1-\alpha} = 1+\beta$$

From the ckt output Current

I_C = amplification factor (input current) + Leakage Current

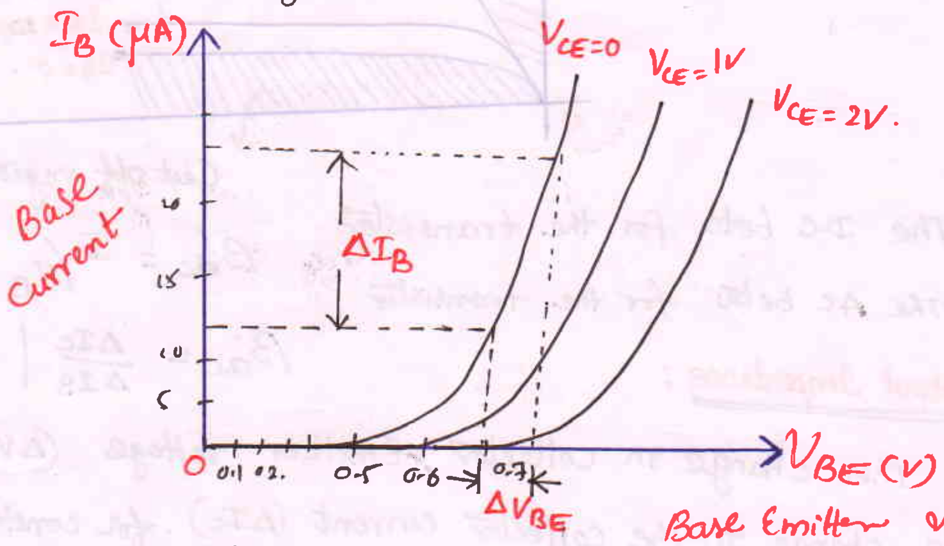
$I_C = \beta I_B + I_{CEO} \rightarrow (4)$ — I_{CEO}: Collector to Emitter Current at Base is open ckted.

From (3) = (4)

$$\Rightarrow \boxed{I_{CEO} = I_{CBO}(1+\beta)}$$

Input Characteristics :

It is the curve between input current I_B (base current) and input voltage V_{BE} (base Emitter voltage) at constant Collector - Emitter voltage 'V_{CE}'.



From above characteristics

After the cut-in voltage the base current (I_B) increases rapidly with small increase in base Emitter voltage (V_{BE}).

Input impedance (r_i) :

The ratio of change in base-Emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector Emitter voltage 'V_{CE}'. ie

$$r_i = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE} = \text{constant}}.$$

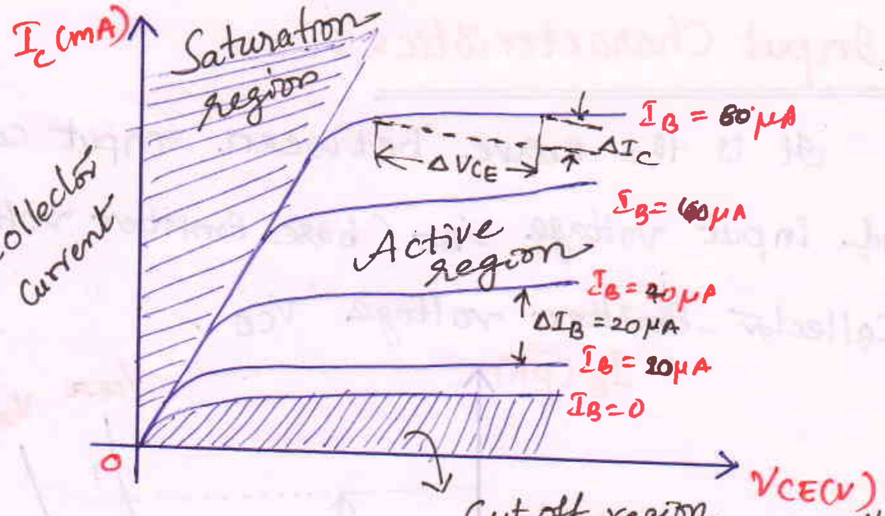
For a fixed value of V_{BE}, I_B decreases as V_{CE} is increased.

A large value of V_{CE} results in a large reverse bias at collector jun.

ie Increases the depletion region & reduces the effective width of the base & reducing the base current I_B.

Output Characteristics :

It is the curve between the collector current 'I_c' and collector voltage 'V_{CE}' for various fixed values of 'I_B'. It shows the output characteristics of CE configuration.



* The D.C beta for the transistor $\beta_{dc} = I_C / I_B \Big|_{V_{CE} = \text{constant}}$.

The AC beta for the transistor $\beta_{ac} = \frac{\Delta I_C}{\Delta I_B} \Big| \Delta V_{CE} = 0$.

Output Impedance :

The change in collector-Emitter voltage (ΔV_{CE}) causes the little change in the collector current (ΔI_C). for constant base current I_B

$$\therefore \quad r_o = \frac{\Delta V_{CE}}{\Delta I_C} \Big|_{I_B = \text{Constant (or) } \Delta I_B = 0}.$$

The output characteristics of common Emitter configuration consists of 3 regions : Active, Saturation and cut-off.

Active Region: In this region, the collector jun is reverse biased. As V_{CE} is increased, reverse bias increases. It causes depletion region to spread more in base than in collector, reducing the chances of recombinations in the base. This causes (early effect) collector current to rise more sharply with increasing V_{CE} in the linear region.

$$I_C = \beta I_B + (1+\beta) I_{CO}$$ where $\beta = \alpha / 1-\alpha$.

Usually $I_B >> I_{CO}$ then $I_C = \beta I_B$.

Saturation region: If V_{CE} is reduced to a small value such as 0.2V. then collector-base junction becomes forward biased. & Emitter base junction is already forward biased.

$\therefore$ The saturation value of V_{CE} ranges from 0.1V to 0.3V.

Cutoff Region: When the input base current is made equal to zero, the collector current is the reverse leakage current I_{CEO}.

The region below $I_B = 0$ is the cut-off region of operation of transistor. Here both junctions are reverse biased.

ie $I_B = 0 \Rightarrow I_C = I_E$ $(\because I_E = I_B + I_C)$

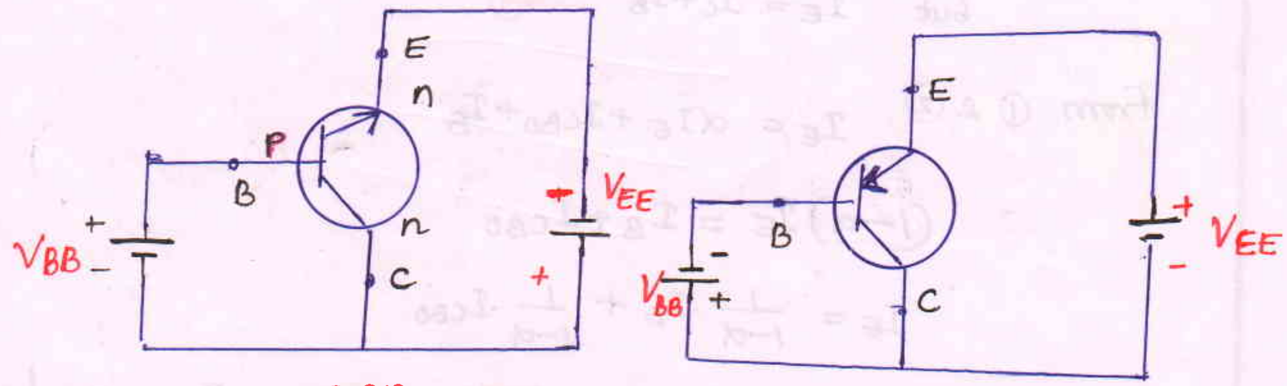
$$\therefore I_C = (1+\beta) I_{CO} = \frac{I_{CO}}{1-\alpha} = I_{CEO}.$$

In the active region the collector jun is reverse biased. The limit on the max. value for reverse bias voltage. If this limit is exceeded the break down occurs. This effect is commonly known as "Punch through effect".

$$I_{CEO} = (1+\beta) I_{CBO}$$

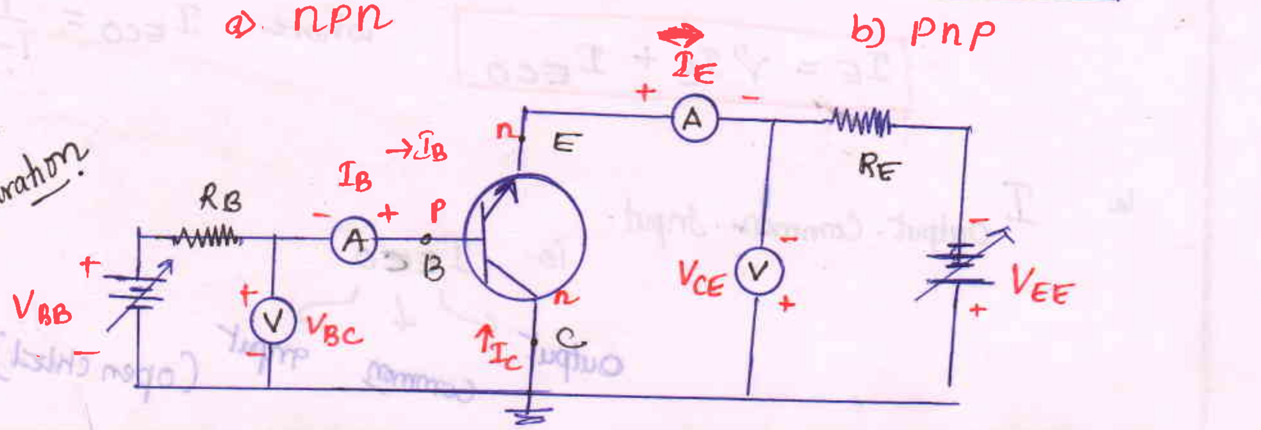
Common Collector (CC) Configuration:

Here an input is applied between base and collector & output is taken from emitter & collector. So collector of the transistor is common to both input & output ckts hence the name common collector configuration.



a) npn   b) pnp

CC configuration



Circuit Description:

Current Amplification factor $\gamma = \frac{\Delta I_E}{\Delta I_B}$ → ①

But we know that $I_E = I_C + I_B$

$$\Delta I_E = \Delta I_C + \Delta I_B$$

$$\Rightarrow \Delta I_B = \Delta I_E - \Delta I_C \longrightarrow ②$$

From ① & ② $\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C} = \frac{\Delta I_E / \Delta I_E}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{1}{1-\alpha}$

$$\therefore \gamma = \frac{1}{1-\alpha}$$

& $1+\beta = \frac{1}{1-\alpha} = \gamma \Rightarrow \gamma = 1+\beta$.

Note:

Relation ship b/w α, β, γ

where

$$\alpha = \frac{\beta}{1+\beta}, \quad \beta = \frac{\alpha}{1-\alpha}, \quad \gamma = \frac{1}{1-\alpha} = 1+\beta.$$

$$\alpha = \beta/\gamma, \quad \beta = \alpha\gamma \quad \& \quad \gamma = \alpha/\beta.$$

Output Current Expression (I_E):

We know that $I_C = \alpha I_E + I_{CBO}$ → ①

but $I_E = I_C + I_B$ → ②

From ① & ② $I_E = \alpha I_E + I_{CBO} + I_B$

$$(1-\alpha) I_E = I_B + I_{CBO}$$

$$I_E = \frac{1}{1-\alpha} I_B + \frac{1}{1-\alpha} \cdot I_{CBO}$$

$$\therefore I_E = \gamma I_B + I_{ECO}$$

where $I_{ECO} = \frac{1}{1-\alpha} I_{CBO}$.

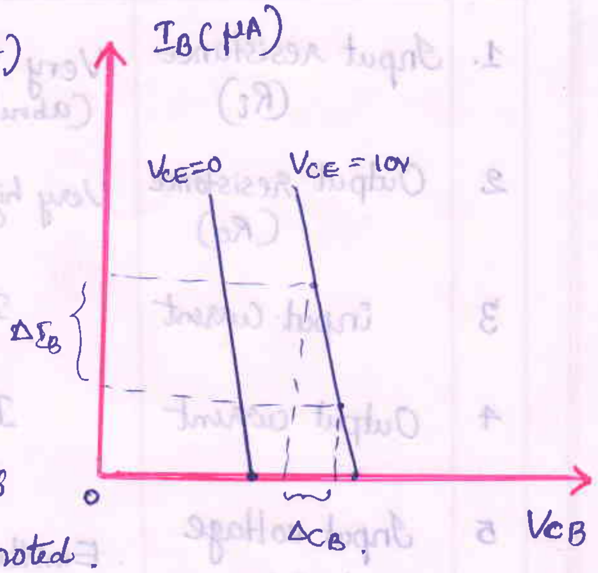
ie $I_{\text{Output} \cdot \text{Common} \cdot \text{Input}}$

ie I_{ECO} → Output, Common, input (Open ckted).

Input Characteristics :

It is the graph of input current 'I_B' ie base current Vs input voltage V_{CB} (collector - base voltage) at constant V_{CE}

ie $R_i = \left.\dfrac{\Delta V_{CB}}{\Delta I_B}\right|_{\Delta V_{CE} = K \text{ (constant)}}$



$V_{CE} = V_{CB} - V_{BE}$

$\Rightarrow V_{CB} = V_{CE} + V_{BE}$.

& $|V_{BE}| < |V_{EC}|\ V_{BC}|$

$I_B < I_C < I_E$.

The V_{CB} is increased in equal steps and the corresponding increase in I_B is noted.

Output Characteristics :

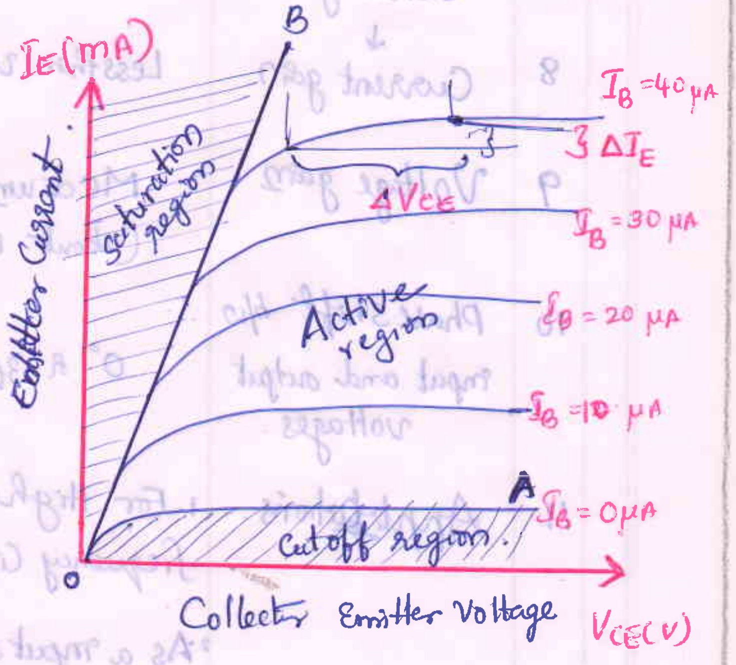
It is the graph between Emitter current I_E and collector to emitter voltage V_{CE} at constant base current I_B

Since $I_C \cong I_E$ ie the CC output characteristics are similar to those of the CE output characteristics.

ie $|V_{EC}| = |V_{CE}|$

$I_E = I_C + I_B \cong I_C$

$R_o = \left.\dfrac{\Delta V_{EC}}{\Delta I_E}\right|_{I_B = \text{constant}}$.



Cutoff region is below $I_B = 0$.

Above OA & left to OB is saturation region,

Above OA & right to OB is Active region.

Hence $V_{i/p} = f_1(V_{CB}, I_B)$

$V_{o/p} = f_2(V_{EC}, I_E)$.

Comparision of Transistor Configurations : ***

SL NO	Parameter (or) Characteristic	Common Base CB	Common Emitter CE	Common Collector CC
1.	Input resistance (R_i)	Very low (about 100Ω)	Moderate (about 1 KΩ)	Very High (about 500KΩ)
2	Output resistance (R_o)	Very high (1MΩ)	Moderate (about 40KΩ)	Low (about 25Ω)
3	input current	I_E	I_B	I_B
4	Output current	I_C	I_C	I_E.
5	Input voltage applied between	Emitter & Base	Base and Emitter	Base and Collector.
6	Output voltage taken between	Collector and Base	Collector and Emitter	Emitter and Collector.
7	Current Amplification factor (α) Current gain ↓	$\alpha = \frac{\Delta I_C}{\Delta I_E}$	$\beta = \frac{\Delta I_C}{\Delta I_B}$	$\gamma = \frac{\Delta I_E}{\Delta I_B}$.
8	Current gain	Less than unity	High (20 to few hundreds)	High (20 to few hundreds)
9	Voltage gain	Medium (about 150).	High (about 500)	less than unity.
10	Phase shift b/w input and output voltages.	0° & 360°	180°	0° & 360°.
11.	Applications.	1. For High frequency Circuits 2. As a input stage of multistage amplifier.	For audio frequency Circuits	1. For impedance matching. 2. For buffer.

Limits of Operation (Breakdown in Transistors) :

There is a possibility of voltage breakdown in the transistor at high voltages even though the rated dissipation of the transistor is not exceeded. ∴ There is an upper limit to the max. allowable collector junction voltage.

Two types of breakdown in transistor.

1. Avalanche breakdown
2. Reach through or punch through.

① Avalanche Breakdown :

When a diode is reverse biased there is a limit on the voltage that can be applied which is avalanche voltage.

lly. In the transistor, the max. reverse biasing voltage which may be applied before breakdown between the collector and base terminals with the emitter open is called breakdown voltage BV_{CBO}.

∴ The limit is set on the collector voltage V_{CB} by avalanche breakdown in the reverse biased collector junction.

An order of limits V_{CB} to a max. of several tens of volts.

Breakdown may occur because of Avalance multiplifaction of current I_{CO} that crosses the collector junction.

$$\therefore M = \frac{1}{1-\left(\frac{V_{CB}}{V_{CBO}}\right)^{n}}$$

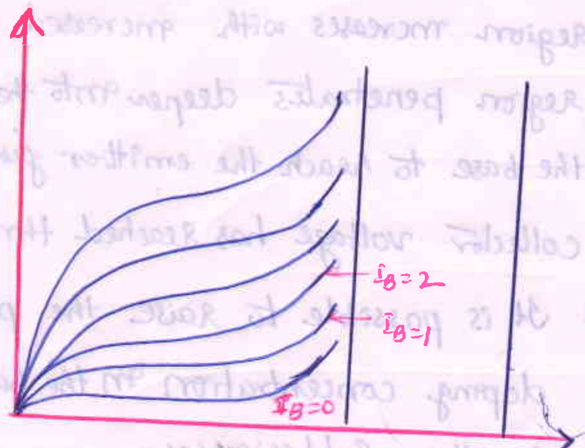


Fig: CE Characteristics in the breakdown region

where $n \rightarrow$ Empirical Constant

For CE.
$n=4$, N-type
$n=2$, P type of Si.

$$BV_{CEO} = BV_{CBO}\sqrt[n]{1/h_{fe}}$$

This is the upper limit of V_{CE} that can be placed across the transistor without damaging it.

Continued →

Why CE Configuration is widely used in Amplifier Circuits ?

1. CE configuration which provides both voltage gain as well as current gain greater than unity. In case of CB - current gain < 1 and CC voltage gain < 1.
2. The power gain (is a product of voltage gain and current gain) of the CE is greather than the power gain of CB & CC configuration.
3. In a CE, the ratio of output resistance to input resistance is small may range from 10Ω to 100Ω. It makes configuration an ideal for coupling between various transistor stages.

Typical transistor Junction Voltages :

At 25°C.

Type	$V_{CE(sat)}$	$V_{BE(sat)}$	V_{BE} (act)	V_{BE} (cut in)	V_{BE} (cutoff)
Si	0·3	0·7	0·6	0·5	0
Ge	0·1	0·3	0·2	0·1	−0·1

→ Continue

② Reach through & Punch through :

* According to Early effect, the width of the collector junction transition region increases with increased collector junction voltage. then transition region penetrates deeper into the base and will have spread completely across the base to reach the emitter junction as the base is very thin. Thus the collector voltage has reached through the base region as called Reach-through
* It is possible to raise the punch-through voltage by increasing the doping concentration in the base, but this automatically reduces the Emitter Efficiency.
* Punch through takes place at a fixed voltage between collector and Base and is not dependent on ckt configuration where as avalanche multiplication takes place at different voltages depending upon the circuit configuration.

Simple Problems:

① If a transistor has α of 0.97. find the value of β. If $\beta = 200$ find the value of α.

Sol
$$\alpha = \frac{\beta}{1+\beta} \quad \& \quad \beta = \frac{\alpha}{1-\alpha}$$

If $\alpha = 0.97$ $\beta = \frac{\alpha}{1-\alpha} = \frac{0.97}{1-0.97} = 32.33 \Rightarrow$ $\boxed{\beta = 32.33}$

If $\beta = 200$ $\alpha = \frac{\beta}{1+\beta} = \frac{200}{1+200} = 0.995 \Rightarrow$ $\boxed{\alpha = 0.995}$

② Determine the values of I_B & I_E for the transistor ckt if $I_C = 80mA$ and $\beta = 170$.

Sol
$I_C = 80mA$

$\beta = 170$ $\quad \beta = \frac{I_C}{I_B} \Rightarrow I_B = \frac{I_C}{\beta} = \frac{80\times10^{-3}}{170} = 0.47mA$

$\therefore$ $\boxed{I_B = 0.47mA}$

$I_E = I_B + I_C$

$\Rightarrow I_E = 80mA + 0.47mA = 80.47mA \Rightarrow$ $\boxed{I_E = 80.47mA}$

③ Calculate the collector current and Emitter for a transistor with $\alpha_{dc} = 0.99$ and $I_{CBO} = 50\mu A$. when the base current is $20\mu A$.

Sol Given $\alpha_{dc} = 0.99$

$I_{CBO} = 50\mu A$ $\quad \& \quad I_B = 20\mu A$.

$I_C = \alpha I_E + I_{CBO}$ $\quad \& \quad I_E = I_B + I_C$.

$I_C = \alpha(I_B + I_C) + I_{CO}$.

$(1-\alpha) I_C = \alpha I_B + I_{CO}$.

$$I_C = \frac{\alpha I_B + I_{CO}}{(1-\alpha)}$$

$I_C = \frac{0.99 \times 20\times10^{-6} + 50\times10^{-6}}{1-0.99} = 6.98mA$ $\quad \therefore$ $\boxed{I_C = 6.98\,mA}$

$I_E = I_B + I_C = 20\times10^{-6} + 6.98\times10^{-3} = 7\times10^{-3}A = 7mA$

$\therefore$ $\boxed{I_E = 7\,mA}$

(4) The reverse leakage current of the transistor when connected in CB configuration is 0.2 μA while it is 18 μA when the same transistor is connected in CE configuration. Calculate α_{dc} & β_{dc} of the transistor?

Sol Given $I_{CBO} = 0.2\,\mu A$

$I_{CEO} = 18\,\mu A$.

$\Rightarrow I_{CEO} = (1+\beta) I_{CBO} \Rightarrow \beta = \frac{I_{CEO}}{I_{CBO}} - 1$

$\beta = \frac{18}{0.2} - 1 = 89$

$\therefore \boxed{\beta_{dc} = 89}$

$\alpha_{dc} = \frac{\beta}{1+\beta} = \frac{89}{1+89} = 0.988$ $\therefore \boxed{\alpha_{dc} = 0.988}$.

(5) A transistor operating in CB configuration has $I_C = 2.98$ mA, $I_E = 3$ mA & $I_{CO} = 0.01$ mA. What current will flow in the collector ckt of this transistor when connected in CE configuration with a base current of 30 μA?

Sol Given. $I_C = 2.98$ mA, $I_E = 3$ mA, $I_{CO} = 0.01$ mA.

For CB. $I_C = \alpha I_E + I_{CO} \Rightarrow \alpha = \frac{I_C - I_{CO}}{I_E} = \frac{2.98m - 0.01m}{3m} = 0.99$

$\therefore \boxed{\alpha = 0.99}$

$\beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-0.99} = 99$ $\therefore \boxed{\beta = 99}$

For CB

$I_C = \beta I_B + (1+\beta) I_{CO}$, where $I_B = 30\,\mu A$ (Given).

$= 99 \times 30 \times 10^{-6} + (1+99) \times 0.01 \times 10^{-3}$.

$I_C = 3.97$ mA $\therefore \boxed{I_C = 3.97\text{ mA}}$

(6) The reverse saturation current in a transistor is 8 μA. If the transistor common base current gain is 0.979. Calculate the collector and Emitter current for 40 μA base current.

Sol $I_{CO} = 8\,\mu A$ $\alpha = 0.979$. $I_B = 40\,\mu A$.

$I_C = \alpha I_E + I_{CO}$, $I_E = I_B + I_C$.

$(1-\alpha) I_C = \alpha I_B + I_{CO}$

$\therefore I_C = \frac{\alpha I_B + I_{CO}}{1-\alpha} = 2.25$ mA. $\therefore \boxed{I_C = 2.25\text{ mA}}$

& $I_E = I_C + I_B$

$= 2.25m + 40\mu$

$I_E = 2.29$ mA

$\therefore \boxed{I_E = 2.29\text{ mA}}$