Institute Vision

To emerge as a Centre of Excellence for Learning and Research in the domains of engineering, computing and management.

Institute Mission

IM1: Provide congenial academic ambience with state -of -art of resources for learning and research.

IM2: Ignite the students to acquire self-reliance in the latest technologies.

IM3: Unleash and encourage the innate potential and creativity of students.

IM4: Inculcate confidence to face and experience new challenges.

IM5: Foster enterprising spirit among students.

IM6: Work collaboratively with technical Institutes / Universities / Industries of National and International repute

DEPARTMENT VISION

To become a centre of excellence in Electronics and Communication Engineering and provide necessary skills to the students to meet the challenges of industry and society.

DEPARTMENT MISSION

- Provide congenial academic ambience with necessary infrastructure and learning resources
- Inculcate confidence to face and experience new challenges from industry and society.
- Ignite the students to acquire self-reliance in State-of-the-Art Technologies
- Foster Enterprising spirit among students

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

After few years of graduation the, graduates of Electronics and Communication Engineering shall

PEO1: Have Professional competency through the application of knowledge gained from subjects like Mathematics, Physics, Chemistry, Inter-Disciplinary and core subjects like Signal Processing, VLSI, Embedded Systems, Communication and Automation.**(Professional Competency)**

PEO2: Exc*el in one's career by critical thinking towards successful services and growth of the organization or as an entrepreneur or through higher studies.* **(Successful Career Goals)**

PEO3: Enhance knowledge by updating *advanced technological concepts* for facing the *rapidly changing world and contribute to society through innovation and creativity.* **(Continuing Education and Contribution to Society)**

PROGRAMME OUTCOMES (PO's)

On Successful completion, the graduate will be able to,

PO1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2. **Problem analysis**: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11. **Project management and finance**: Demonstrate knowledge and understanding of the Engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12. **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of Technological change.

PROGRAM SPECIFIC OUTCOMES (PSO's)

On Successful completion, the graduate will be able to,

PSO1: Apply the knowledge obtained in core areas for the analysis and design of components in Signal Processing, VLSI, Embedded Systems, Communication and Automation.

PSO2: Adapt Innovation, Creativity and design to develop products which meet industrial and societal needs.

ACADEMIC REGULATIONS

(SITAMS - R20)

(M.Tech Regular-Full Time Two year degree program)

(For the batches admitted from the Academic Year 2020-2021)

(CHOISE BASED CREDIT SYSTEM)

1. ELIGIBILITY FOR ADMISSION

Admission of the M.Tech program shall be made subjects to the eligibility qualifications and Specialization prescribed by the University for each Program from time to time. Admission shall be made either on the basis of Merit/ Rank Obtained by the Qualifying candidates in PGCET or otherwise specified whichever is relevant.

2. AWARD OF M.Tech. DEGREE

A student will be declared eligible for the award of the M.Tech. Degree if he/she fulfils the following academic regulations:

Pursues a course of study for not less than two academic years and in not more than four academic years.

Registers for 68 credits and secure all 68 credits.

Semester	Course Particulars					Number of Credits
	Theory Courses	Practical Courses	MOOC / Open Elective	Audit Course	Project Work	
I-I	15	4	-	1	-	20
I-II	18	4	-	-	-	22
II-I	-	-	2	-	10	12
IV-I	-	-	-	-	14	14
Total Credits Allotted						**68**

3. ACADEMIC REQUIREMENTS

Students, who fail to fulfil all the academic requirements for the award of the degree within four academic years from the year of their admission, shall forfeit their seat in M.Tech. Course and their admission stands cancelled.

4. CURRICULUM AND COURSE STRUCTURE

The curriculum shall comprise Engineering Science (ES), Professional Core (PC), Core Elective (CE), Open Elective (OE), Project Work (PW), and Mandatory Audit Course (MAC).

5. CONTACT PERIODS

Depending on the complexity and volume of the course, the number of contact hours per week will be assigned. Each Theory and Laboratory course carries credits based on the number of hours / week as follows.

- Contact classes (Theory): 1 credit per lecture hour per week.
- Laboratory Hours (Practical): 1 credit for 2 Practical hours, per week.
- Project Work: 1 credit for 2 hours of project work per week

6. SUPPLEMENTARY EXAMINATIONS

The student eligible to appear the supplementary external examinations if he was absent for it or failed in it or not registered.

7. DISTRIBUTION AND WEIGHTAGE OF MARKS

The performance of a student in each semester shall be evaluated subject–wise with a maximum of 100 marks for theory and 100 marks for practical subject. In addition, project work shall be evaluated for100 marks.

- For theory subjects the distribution shall be 40 marks for Internal Evaluation and 60 marks for the End-Examination.
- For practical subjects the distribution shall be 40 marks for Internal Evaluation and 60 marks for the End- Examination.

Internal Examinations

For theory subjects, during the semester, there shall be two mid-term examinations. Each mid-term examination consists of subjective paper for 30 marks with duration of 1hour 50 minutes. However 10 marks are awarded for a Technical Seminar presentation (Preferably case study topics on the particular course). Technical Seminar is presented from the students before term end examinations (preferably before practical examination) for every theory subjects.

Note 1: The theory subjective paper shall contain 3 questions of equal Weightage of 10 marks and the marks obtained for 3 questions shall be condensed to 30 marks; any fraction shall be rounded off to the next higher mark.

Note 2: If the student is absent for the internal examination, no re-exam or make up shall be conducted and internal marks for that examination shall be considered as zero.

Note 3: First midterm examination shall be conducted for 50% of the syllabus and second midterm examination shall be conducted for the remaining 50% of the syllabus.

Note 4: Final Internal marks shall be arrived at by considering the marks secured by the student in both the mid examinations with 80% weightage to the better mid exam and 20% to the other.

For Example:

Marks obtained in first mid: 20 Marks obtained in Second mid: 20

Internal Marks: (20x0.8) + (20x0.2) = 20

Final internal marks= Internal Marks+ Technical Seminar Presentation

Note 5: If the student is absent for any one midterm examination, the final internal marks shall be arrived at by considering 80% Weightage to the marks secured by the student in the appeared examination and zero to the other.

Note 6: For practical subjects there shall be a 40 sessional marks (20 marks allotted for one internal practical examination to be conducted before the last working day and 20 marks for Day-to- day work in the laboratory shall be evaluated by the concerned laboratory teacher based on the regularity / record / viva-voce) and end examination shall be for 60 marks.

End Examinations

End examinations (Theory courses)

End examination of theory subjects shall have the following pattern:

i. End examination shall be for 60 marks.
ii. There shall be either-or type questions for 12 marks each. Student shall answer any one of them.
iii. Each of these questions covers one unit of the syllabus.

End examinations (Practical courses)

End examination of practical course shall have the following pattern:

i. End examination shall be for 60 marks.
ii. The end examination shall be conducted by the concerned laboratory teacher and senior expert in the same subject of the department.

8. MASSIVE ONLINE OPEN COURSE'S (MOOC'S) AND OPEN ELECTIVE

i. The CBCS, also called as Open Electives (OEs) will be implemented in the college. The CBCS provides choice for students to select from the prescribed courses. In which students can take courses of their choice, learn at their own pace and adopt an interdisciplinary approach to learning.

ii. The college in line with the developments in Learning Management Systems (LMS) intends to encourage the students to do online courses in MOOCs, offered nationally / internationally. The main intension to introduce MOOCs is to obtain enough exposure through online tutorials, self- learning at one's own pace, attempt quizzes, discuss with professors from various universities and finally to obtain certificate of completion of the course from the MOOCs providers.

iii. Institution intends to encourage the students to do one MOOC in II year I Semester of the M.Tech. Programme. The respective departments shall give a list of standard MOOCs providers among NPTEL, edx, Udacity, Coursera, or any other standard providers, whose credentials are endorsed by the HoD. Each department shall appoint Coordinators / Mentors and allot the students to them who shall be responsible to guide students in selecting online courses and provide guidance for the registration, progress and completion of the same.

iv. A student shall choose an online open elective course, except his / her program of study from the given list of MOOCs providers, as endorsed by the teacher concerned, with the approval of the HOD.

v. Students may be permitted to register one online course (which is provided with certificate) in II year I semester and they should produce the course completion certificate of that course to the controller of Examination to become eligible for fulfillment of the degree before the end of II year II semester of their study.

vi. If, the student is unable to complete the certified MOOC within the stipulated period of time and if the candidate selected the MOOC has discontinued from the standard MOOC provider, the college has to conduct the equivalent examination (on the same MOOC syllabus) internally with the approval from the

head of the department on the request of students along with separate examination fee.

9. CORE ELECTIVES

Students have to choose core electives (CE-I and CE-II) in I year I semester and core electives (CE-III and IV) in I year II semester, from the list of core electives courses given. However, the students may opt for core elective subjects offered in the related area.

10. PROJECT WORK

i. The project work for M.Tech. Programmes consist of Phase–I and Phase–II.

ii. The Phase–I is to be undertaken during II year I semester and Phase–II, which is a continuation of Phase–I is to be undertaken during II year II semester.

iii. If Candidates not completing Phase-I of project work successfully, the candidates can undertake Phase-I again in the subsequent semester. In such cases the candidates can enroll for Phase-II, only after successful completion of Phase-I.

iv. Project work shall be carried out under the supervision of a "senior teacher" in the Department. In this context "senior teacher" means the faculty member possessing (a) PG degree with a minimum of 5 years experience in teaching or (b) Ph.D. degree.

v. A candidate may, however, in certain cases, be permitted to work on projects in an Industrial/Research Organization, on the recommendations of the Head of the Department Concerned. In such cases, the Project work shall be jointly supervised by a supervisor of the department and an expert, as a joint supervisor from the organization and the student shall be instructed to meet the supervisor periodically and to attend the review committee meetings for evaluating the progress.

vi. The Project work (Phase II) shall be pursued for a minimum of 16 weeks during the final semester.

vii. The deadline for submission of final Project Report is 60 calendar days from the last working day of the semester in which project / thesis / dissertation is done.

However, the Phase-I of the Project work shall be submitted within a maximum period of 30 calendar days from the last working day of the semester as per the academic calendar published by the Institution.

11. EVALUATION OF PROJECT WORK

- The evaluation of Project Work for Phase-I & Phase-II shall be done independently in the respective semesters and marks shall be allotted as per the weightages given in Clause 11.1.
- There shall be three internal assessments during the Semester by a review committee.
- The Student shall make presentation on the progress made before the Committee.
- The Head of the Department shall constitute the review committee.
- The total marks obtained in the three assessments shall be converted to 40 marks and rounded to the nearest integer (as per the Table given below).
- Project Work for Phase-I, there will be a Viva-voce Examination during End of the Semester conducted by a Committee consisting of the supervisor, two internal examiners (Preferably one Senior Teacher and Head of the Department).
- Project Work for Phase-II, there will be a Viva-voce Examination during End Semester Examinations conducted by a Committee consisting of the supervisor, one internal examiner and one external examiner.
- The internal examiner and the external examiner shall be appointed by the Principal / Chief Examiner.
- As per the guidelines given the project report must be prepared and submitted to the Head of the department before the Viva-Voce Examination.
- The distribution of marks for the internal assessment and End semester examination is given below:

11.1 Project-Work:

<table>
<tr><th colspan="7">Phase I</th></tr>
<tr><th colspan="3">Internal Assessment (40 Marks)</th><th colspan="4">End Semester Examination (60 Marks)</th></tr>
<tr><td rowspan="2">Review - I</td><td rowspan="2">Review - II</td><td rowspan="2">Review - III</td><td colspan="4">Project Work Phase I Viva – Voce
(60 Marks)</td></tr>
<tr><td>Thesis Submission (Project Review Committee)</td><td>Supervisor Examiner</td><td>Internal Examiner 1</td><td>Internal Examiner 2</td></tr>
<tr><td>10</td><td>15</td><td>15</td><td>15</td><td>15</td><td>15</td><td>15</td></tr>
<tr><th colspan="7">Phase II</th></tr>
<tr><th colspan="3">Internal Assessment (40 Marks)</th><th colspan="4">End Semester Examination (60 Marks)</th></tr>
<tr><td rowspan="2">Review - I</td><td rowspan="2">Review - II</td><td rowspan="2">Review - III</td><td colspan="4">Project Work Phase II Viva – Voce
(60 Marks)</td></tr>
<tr><td>Thesis Submission (External Examiner)</td><td>Supervisor Examiner</td><td>Internal Examiner</td><td>External Examiner</td></tr>
<tr><td>10</td><td>15</td><td>15</td><td>15</td><td>15</td><td>15</td><td>15</td></tr>
</table>

- In case of Industrial Project, Students are encouraged to go to Industrial Internship for at least 2-3 months and should be organized by the Head of the Department for every student.
- At the end of the Industrial Project, the candidate shall submit a certificate from the organization where he/she has undergone industrial training and also a brief report. The evaluation for 100 marks will be carried out internally based on this report and a Viva-Voce Examination will be conducted by a Departmental Committee constituted by the Head of the Institution.
- If the candidate fails to obtain 50% of the internal assessment marks in the Phase–I and Phase–II / final project viva-voce, he/she will not be permitted to submit the report for that particular semester and has to re-enroll for the same in the subsequent semester.

- At the end of the Phase – II Project Work, the candidate has to incorporate the plagiarism report in their thesis and it should be less than 30% (Excluding the references).
- The candidate has to publish at-least one research paper on their project topic in either Scopus indexed or Web of Science indexed journal (UGC listed journal) and details of the acceptance of the paper(s) / published paper(s) should be incorporated in the thesis.
- If a candidate fails to submit the project report on or before the specified deadline, he/she is deemed to have failed in the Project Work and shall re-enroll for the same in a subsequent semester. This applies to both Phase–I and Phase–II project work.
- If a candidate fails in the end semester examinations of Phase–I, he/she has to resubmit the Project Report within 30 days from the date of declaration of the results. If he / she fails in the End semester examination of Phase–II of Project work, he/she shall resubmit the Project Report within 60 days from the date of declaration of the results. The resubmission of a project report and subsequent viva-voce examination will be considered as reappearance with payment of exam fee. For this purpose the same Internal and External examiners shall evaluate the resubmitted report.
- A copy of the approved Project Report after the successful completion of viva-voce examinations shall be kept in the library of the Institution.

12. ATTENDANCE REQUIREMENTS

- A student shall be eligible to appear for University examinations if he / she acquires minimum of 75% of attendance in aggregate of all the subjects in a semester.
- Shortage of Attendance below 65% in aggregate shall in NO case be condoned.
- Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester may be granted by the College Academic Committee.

- Students whose shortage of attendance is not condoned in any semester are not eligible to take their end examination of that class and their registration shall stand cancelled.
- A student will not be promoted to the next semester unless he satisfies the attendance requirements of the present semester. They may seek readmission for that semester when offered next.
- A stipulated fee shall be payable towards Condonation of shortage of attendance to the College.

13. COURSE PATTERN

- The entire course of study is for two academic years. All years shall be on semester pattern. A student eligible to appear for the end examination in a subject, but absent or has failed in the end examination may appear for that subject at the next supplementary examination whenever it offered.
- When a student is detained due to shortage of attendance he may be re-admitted when the semester is offered after fulfillment of academic regulations. In such case, he / she shall be in the academic regulations into which he / she is readmitted.

14. WITH-HOLDING THE RESULT

- If the candidate has any dues not paid to the institution or if any case of indiscipline or malpractice is pending against him, the result of the candidate shall be withheld and he will not be allowed / promoted into the next higher semester. The issue of awarding degree is liable to be withheld in such cases.

15. GRADING

- After each subject is evaluated for 100 marks, the marks obtained in each subject will be converted to a corresponding letter grade as given below, depending on the range in which the marks obtained by the student fall.
- Table – Conversion into Grades and Grade Points assigned

Range in which the Marks In the Subject Fall	**Grade**	**Grade Points** Assigned
≥ 90	S	10
80 ≥ 89	A	9
70 ≥ 79	B	8
60 ≥ 69	C	7
50 ≥ 59	D	6
< 50	F (Fail)	0
Absent	Abs (Absent)	0

- A student obtaining Grade F shall be considered failed and will be required to reappear for that subject when the next supplementary examination offered.
- For non credit courses "Pass" shall be indicated instead of the letter 'P' and this will not be counted for the computation of SGPA/CGPA.

16. SEMESTER GRADE POINT AVERAGE (SGPA) AND CUMULATIVE GRADE POINT AVERAGE (CGPA)

- The Semester Grade Point Average (SGPA) is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e.

$$SGPA = \Sigma (Ci \times Gi) / \Sigma Ci$$

Where, Ci is the number of credits of the ith subject and Gi is the grade point scored by the student in the ith course.

- The Cumulative Grade Point Average (CGPA) will be computed in the same manner taking into account all the courses undergone by a student over all the semesters of a program, i.e.

  $CGPA = \Sigma (Ci \times Si) / \Sigma Ci$

  Where Si is the SGPA of the ith semester and Ci is the total number of credits in that semester.
- Both SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts.
- SGPA will be given to those who cleared all the subjects in that semester
- GRADE POINT: It is a numerical weight allotted to each letter grade on a 10-point scale.
- LETTER GRADE: It is an index of the performance of students in a said course. Grades are denoted by letters S, A, B, C, D and F.

17. AWARD OF CLASS

- After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of B. Tech. Degree he shall be placed in one of the following four classes:

Class Awarded	**CGPA Secured**
First Class with Distinction	≥ 7.5
First Class	$\geq 6.5 < 7.5$
Second Class	$\geq 5.5 < 6.5$

18. TRANSITORY REGULATIONS

- Discontinued, detained, or failed candidates are eligible for readmission as and when the semester is offered after fulfillment of academic regulations.

19. MINIMUM INSTRUCTION DAYS

- The minimum instruction days including exams for each semester shall be 90 days.

20. REVALUATION

- A candidate can apply for revaluation of his / her end examination answer paper in a theory courses. The examination section shall issue a notification inviting applications for the revaluation after publishing the results. The application forms can be obtained from the examination section. A candidate can apply for revaluation of answer scripts in not more than 5 subjects at a time.
- No revaluation for comprehensive Examination, practical and project work.

21. CONDUCT AND DISCIPLINE

i. Students shall conduct themselves within and outside the precincts of the Institute in a manner befitting the students of an Institute of National importance

ii. As per the order of the Hon'ble Supreme Court of India, ragging in any form is banned: acts of ragging will be considered as gross indiscipline and will be severely dealt with.

iii. The following additional acts of omission and /or commission by the students within or outside the precincts of the college shall constitute gross violation of code of conduct and are liable to invoke disciplinary measures

a. Ragging
b. Lack of courtesy and decorum: indecent behavior anywhere within or outside the campus.
c. Willful damages or stealthy removal of any property /belongings of the Institute / Hostel or of fellow students
d. Possession, consumption of distribution of alcoholic drinks or any kind of hallucinogenic drugs
e. Mutilation or unauthorized possession of library books
f. Hacking in computer systems
g. Furnishing false statements to the disciplinary committee, or willfully withholding information relevant to an enquiry

h. Organizing or participation in any activity that has potential for driving fellow students along lines of religion caste batch of admission hostel or any other unhealthy criterion.
i. Resorting to noisy and unseemly behavior, disturbing studies of fellow students
j. Physical or mental harassment of fresher through physical contact or oral abuse
k. Adoption of unfair means in the examination
l. Organizing or participating in any group activity except purely academic and scientific Programmers in company with others in or outside campus without prior permission of the Principal
m. Disturbing in drunken state or otherwise an incident in academic or students function or any other public event.
n. Not obeying traffic rules in campus not following safety practices or causing potential danger to oneself or other persons in any way.
o. Any other act or gross indiscipline

iv. Commensurate with the gravity of the offence the punishment may be reprimand fine and expulsion from the hostel debarment from an examination rustication for a specified period or even outright expulsion from the College
v. The reprimanding Authority for an offence committed by students in the Hostel and in the Department or the classroom shall be respectively, the managers of the Hostels and the Head of the concerned Department
vi. In all the cases of offence committed by students in jurisdictions outside the purview of clause (21.v) the Principal shall be the Authority to reprimand them.
vii. All Major acts of indiscipline involving punishment other than mere reprimand shall be considered and decided by the Principal Students Disciplinary Committee appointed by the Principal.
viii. All other cases of Indiscipline of Students like adoption of unfair means in the examinations shall be reported to the Vice-Principal for taking appropriate action and deciding on the punishment to be levied.
ix. In all the cases of punishment levied on the students for any offence committed

the aggrieved party shall have the right to appeal to the Principal who shall constitute appropriate Committees to review the case.

22. TRANSFER DETAILS

Student transfers shall be as per the guidelines issued by the Government of Andhra Pradesh from time to time.

23. GENERAL

- The academic regulations should be read as a whole for purpose of any interpretation. Malpractices rules- nature and punishments are appended.
- Where the words “he”, “him”, “his”, occur in the regulations, they also include “she”, “her”, “hers”, respectively.
- The college may change or amend the academic regulations or syllabi at any time and the changes or amendments shall be made applicable to all the students on rolls with effect from the dates notified by the college.

M.TECH VLSI SYSTEM DESIGN: CURRICULUM and SYLLABUS – 2020

I Year M.Tech. I Semester

S.No	Subject Code	Subject	Subject Category	Scheme of Instructions Hours per Week				Scheme of Examination Maximum Marks		
				L	T	P/D	C	I	E	Total
1.	**20MVSD11**	CMOS VLSI and Digital IC Design	PC	3	-	-	3	40	60	100
2.	**20MVSD12**	Analog IC Design	PC	3	-	-	3	40	60	100
3.	**20MVSD13**	FPGA and HDL Programming	PC	3	-	-	3	40	60	100
4.	**20MVSD14**	Core Elective - I	CE	3	-	-	3	40	60	100
5.	**20MVSD15**	Core Elective - II	CE	3	-	-	3	40	60	100
6.	**20MVSD16**	Research Methodology and IPR	ES	3	-	-	1	40	60	100
7.	**20MVSD17**	Analog IC Design Lab	PC	-	-	3	2	40	60	100
8.	**20MVSD18**	HDL Programming Lab	PC	-	-	3	2	40	60	100
Contact Hours per week				18	-	6	-	-	-	-
Total Hours per week							-	-	-	-
Total credits							20	-	-	-
Total Marks								320	480	800

I Year M.Tech. II Semester

S.No	Subject Code	Subject	Subject Category	Scheme of Instructions Hours per Week				Scheme of Examination Maximum Marks		
				L	T	P/D	C	I	E	Total
1.	**20MVSD21**	Low Power VLSI Design	PC	3	-	-	3	40	60	100
2.	**20MVSD22**	ASIC Design	PC	3	-	-	3	40	60	100
3.	**20MVSD23**	Scripting Languages for HDL	PC	3	-	-	3	40	60	100
4.	**20MVSD24**	CAD for VLSI	PC	3	-	-	3	40	60	100
5.	**20MVSD25**	Core Elective - III	CE	3	-	-	3	40	60	100
6.	**20MVSD26**	Core Elective – IV	CE	3	-	-	3	40	60	100
7.	**20MVSD27**	ASIC Design Lab (CAD Tool)	PC	-	-	3	2	40	60	100
8.	**20MVSD28**	Scripting Language Lab	PC	-	-	3	2	40	60	100
Contact Hours per week				18	-	6	-	-	-	-
Total Hours per week							-	-	-	-
Total credits							22	-	-	-
Total Marks								320	480	800

II year M.Tech. I Semester

S.No	Subject Code	Subject	Subject Category	Scheme of Instructions Hours per Week				Scheme of Examination Maximum Marks		
				L	T	P/D	C	I	E	Total
1.	MOOC01	MOOC	MOOC	-	-	-	2	-	-	-
2.	**20MVSD31**	Project Work Phase -I / Industrial Project*	PC	-	-	-	10	40	60	100
Contact Hours per week							-	-	-	-
Total Hours per week							-	-	-	-
Total credits							12	-	-	-
Total Marks								40	60	100

II year M.Tech. II Semester

S.No	Subject Code	Subject	Subject Category	Scheme of Instructions Hours per Week				Scheme of Examination Maximum Marks		
				L	T	P/D	C	I	E	Total
1.	**20MVSD41**	Project Work Phase -II / Industrial Project*		-	-	-	14	40	60	100
Contact Hours per week								-	-	-
Total Hours per week								-	-	-
Total credits							14	-	-	-
Total Marks								40	60	100

Students are encouraged to go to Industrial Internship for at least 2-3 months.
Students going for Industrial Project will complete these courses through MOOCs.

I year M.Tech. I Sem. (Core Elective-I)

S.No	Subject Code	Subject	Subject Category	Scheme of Instructions Hours per Week				Scheme of Examination Maximum Marks		
				L	T	P/D	C	I	E	Total
1.	**20MVSD14A**	Physics for VLSI Devices	CE	3	-	-	3	40	60	100
2.	**20MVSD14B**	Hardware / Software Co-Design	CE	3	-	-	3	40	60	100
3.	**20MVSD14C**	Mixed Signal Design	CE	3	-	-	3	40	60	100
4.	**20MVSD14D**	Advanced Digital System	CE	3	-	-	3	40	60	100

I year M.Tech. I Semester (Core Elective-II)

S.No	Subject Code	Subject	Subject Category	Scheme of Instructions Hours per Week				Scheme of Examination Maximum Marks		
				L	T	P/D	C	I	E	Total
1.	**20MVSD15A**	Design for Testability and Testing	CE	3	-	-	3	40	60	100
2.	**20MVSD15B**	Digital Signal Processing for VLSI	CE	3	-	-	3	40	60	100
3.	**20MVSD15C**	RF IC Design	CE	3	-	-	3	40	60	100
4.	**20MVSD15D**	Asynchronous System Design	CE	3	-	-	3	40	60	100

I year M.Tech. II Semester(Core Elective-III)

S.No	Subject Code	Subject	Subject Category	Scheme of Instructions Hours per Week				Scheme of Examination Maximum Marks		
				L	T	P/D	C	I	E	Total
1.	**20MVSD25A**	Multi gate Transistors	CE	3	-	-	3	40	60	100
2.	**20MVSD25B**	Nano-scale Transistors	CE	3	-	-	3	40	60	100
3.	**20MVSD25C**	Microelectronics	CE	3	-	-	3	40	60	100
4.	**20MVSD25D**	Modeling and Simulation	CE	3	-	-	3	40	60	100

I year M.Tech. II Sem. (Core Elective-IV)

S.No	Subject Code	Subject	Subject Category	Scheme of Instructions Hours per Week				Scheme of Examination Maximum Marks		
				L	T	P/D	C	I	E	Total
1.	**20MVSD26A**	Memory Design	CE	3	-	-	3	40	60	100
2.	**20MVSD26B**	Advanced Computer Architecture	CE	3	-	-	3	40	60	100
3.	**20MVSD26C**	Fault Tolerant Design	CE	3	-	-	3	40	60	100
4.	**20MVSD26D**	Micro-sensors and Interfacing	CE	3	-	-	3	40	60	100

SUMMARY OF CREDIT ALLOCATION

S.NO	Subject Area	Credits As Per Semester				Total Credits	Percentage – wise Credit Distribution
		I-I	I-II	II-I	II-II		
1.	PC	13	16	-	-	29	42.65
2.	CE	6	6	-	-	12	17.65
3.	OE	-	-	2	-	2	2.95
4.	PW	-	-	10	14	24	35.30
5.	MAC	1	0	-	-	1	1.45
Total	**-**	**20**	**22**	**12**	**14**	68	100

Note: ES – Engineering Science; PC – Professional Core; CE - Core Elective; OE - Open Elective; MOOC – Massive Open Course Online;

I Year M.Tech I Semester

L	T	P	C
3	*0*	*0*	*3*

20MVSD11 CMOS VLSI AND DIGITAL IC DESIGN

Course Educational Objectives:

CEO1: To provide knowledge on Fundamentals of Fabrication Process and electrical properties of MOS transistor
CEO2: To calculate performance parameters of cmos circuits like sheet resistance, power dissipation etc.
CEO3: To develop skill to design SRAM and DRAM using CMOS technology.
CEO4: To develop skill to design and to layout digital circuits using CMOS technology
CEO5: To develop skill to design ALU subsystems like adder and multipliers

UNIT-1:Fabrication Process :: Introduction to IC Technology and IC era – Fabrication process of various types of MOS transistors, Ids Vs. V_{ds} relationships of MOS transistor.

CMOS circuits and Layout tools : MOS Layers, Stick Diagrams, Design Rules and Layout, 2µm, 1.2 µm Design Rules, Rules for Vias and Contacts, Stick Diagrams and Simple Symbolic Encodings for NMOS, PMOS, CMOS and Bi-CMOS Logic Gates. Transistor structures –wire and vias- Scaling of CMOS Circuits. -Layout design tools.

UNIT-2:CMOS Circuit Characterisation and Performance Estimation: Sheet Resistance RS and its Concept to MOS, Area Capacitance Units, Calculations - Delays, Driving Large Capacitive Loads, Delay Estimation, Logical Effort and Transistor Sizing, Power Dissipation, Reliability. CMOS Fault models: need for testing, manufacturing test principle

UNIT-3:
STATIC AND DYNAMIC CMOS DESIGN: Issues in digital IC design ,CMOS inverter, Static and Dynamic characteristics. Static and dynamic cmos design using Domino and Nora logic –Sequential and Combinational circuits..Design of adder , subtractor and multiplier .CMOS memory design: SRAM and DRAM .

UNIT-4: Layout design rules
Need for design rules ,Mead Conway layout design rules for the silicon gate NMOS process – CMOS based design rules-Simple layout examples-Design verification

Unit-5:
SUBSYSTEM DESIGN PROCESS: General arrangement of 4-bit Arithmetic Processor-Design of 4-bit shifter, ALU subsystem: Implementing ALU functions with an adder ,Carry look-ahead adders-Multipliers, Serial –Parallel multiplier –Modified Booths algorithm.

Course Outcomes:

On successful completion of the course the student will be able to,		POs related to COs
CO1	Demonstrate knowledge on fundamentals of fabrication process and electrical properties of MOS transistors	PO1, PO2
CO2	Calculate performance parameters of CMOS circuits like sheet resistance, power dissipation etc.	PO1, PO2, PO3, PO5
CO3	Design SRAM and DRAM using CMOS technology	PO1, PO2, PO3, PO5
CO4	Analyze the layout diagrams for CMOS circuits	PO1, PO2, PO4
CO5	Design the ALU subsystems	PO1, PO4

TEXT BOOKS

1. Kamran Ehraghian, Dauglas A. Pucknell and Sholeh Eshraghiam, "Essentials of VLSI Circuits and Systems" – PHI, EEE, 2005 Edition.
2. CMOS digital Integrated circuits –Analysis & Design ,2/e,1999,Sung-Mo Kang &Yusuf Leblebici, McGraw Hill, New Delhi.

REFERENCES BOOKS:

1. Neil H. E. Weste and David. Harris Ayan Banerjee,, "CMOS VLSI Design" - Pearson Education, 1999.
2. Jan M. Rabaey, "Digital Integrated Circuits" Pearson Education, 2003 3. Wayne Wolf, "Modern VLSI Design ", 2nd Edition, Prentice Hall,1998.
3. Digital Integrated Circuits –A Design Perspective,2/e,1997,Jan M Rabaey, Prentice Hall, New Delhi.
4. Wayne Wolf, "Modern VLSI Design ", 2/e.,, Prentice Hall,1998.
5. Etienne Sicard, Sonia Delmas Bendhia, "Basics of CMOS Cell Design", TMH, EEE, 2005.

CO-PO Mapping

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	-	-	-	-	-	-	-	-	-	-
CO2	2	3	3	-	2	-	-	-	-	-	-	-
CO3	3	2	3	-	3	-	-	-	-	-	-	-
CO4	3	2	-	3	-	-	-	-	-	-	-	-
CO5	2	-	-	3	-	-	-	-	-	-	-	-
CO*	2.6	2.5	3	3	2.5	-	-	-	-	-	-	-

I M.Tech IISemester

L	T	P	C
3	*0*	*0*	*3*

20MVSD12 Analog IC Design

Course Educational Objectives:

CEO1: To acquire knowledge on MOS Devices and Modeling
CEO2: To develop skill to analyze MOS switch current source and current mirrors
CEO3: to obtain basics information in operational amplifier design .
CEO4: To inculcate professional skill in switched capacitor and sampling circuits
CEO5: To obtain knowledge in data convertors and filters

UNIT - 1: MOS Devices and Modeling

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling – Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor

UNIT - 2: Integrated Devices and Modeling and Current Mirror

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT - 3: Operational Amplifier Design and Compensation

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain, Amplifiers Architectures. Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement.

UNIT - 4: Sample and Hold Switched Capacitor Circuits

MOS – CMOS - Bi-CMOS Sample and Hold Circuits - Switched Capacitor Circuits - Basic Operation and Analysis - First Order and Biquard Filters - Charge Injection - Switched Capacitor Gain Circuit - Correlated - Double Sampling Techniques - Other Switched Capacitor Circuits.

UNIT - 5: Data Converters and Filters

Ideal D/A & A/D Converters - Quantization Noise - Performance Limitations - Nyquist Rate D/A Converters - Decoders Based Converters. Binary Scaled Converters. Hybrid Converters. Nyquist Rate A/D Converters: Integrating -Successive Approximation - Cyclic Flash Type - Two Step – Interpolating - Folding and Pipelined - A/D Converters - Over Sampling with and Without Noise Shaping - Digital Decimation Filter - High Order Modulators - Band pass over Sampling Converter - Practical Considerations - Continuous Time Filters.

COURSE OUTCOMES:

On successful completion of the course the student will be able to		**POs related to COs**
CO1	Identifying various issues and design process in MOS Devices and Modelling	PO1, PO2 ,PO3, PO5
CO2	Developing design steps in IC demonstrate the device modeling	PO1, PO2
CO3	Analyze the Operational Amplifier Design concepts	PO1, PO2, PO3, PO5
CO4	Acquire knowledge on biCMOS and other switched capacotors	PO1, PO2, PO4
CO5	Identifying and understanding the concepts in ADC,DAC and filter elements .	PO1, PO4,.

Text Books:

1.Analog Integrated Circuit Design, 2/e, 1997, D.A.John & Ken Martin, John Wiley, New Delhi.
2.Design of Analog CMOS Integrated Circuit, 2/e, 2002, Behzad Razavi Tata Mc GrawHill, Delhi.
3. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

Reference Books:

1.CMOS Analog Circuit Design,2/e, 2002, Philip Allen & Douglas Holberg, Oxford University Press.
2.Analog MOS Integrated Circuits, 2/e, 1986, Gregolian, Temes, John Wiley, NewDelhi.
3. Introduction to CMOS OP-AMPs and comparators, 1/e, 1999, Roubic Gregorian, Wiley, Delhi.
4. Bipolar and MOS Analog integrated circuit design, 2/e, 2002, Alen B. Greben, Wiley-Interscience.
5.Analog Integrated Circuit Design, 2/e, 2012, Tony Chan Carusone, David A.Johns, Kenneth Martin, John Wiley & Sons, United States of America.

CO-PO Mapping

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2	-	3	-	-	-	-	-	-	-
CO2	3	3	-	-	-	-	-	-	-	-	-	-
CO3	3	3	2	-	3	-	-	-	-	-	-	-
CO4	3	2	-	3	-	-	-	-	-	-	-	-
CO5	3	-	-	2	-	-	-	-	-	-	-	-
CO*	3	2.75	2	2.5	3	-	-	-	-	-	-	-

I year M.Tech I Semester

L	T	P	C
3	*0*	*0*	*3*

20MVSD13 FPGA and HDL Programming

Course Educational Objectives:

CEO1: To provide knowledge on Fundamentals of FPGA Architecture, Programming techniques.

CEO2: To acquire knowledge and skills in FSM concepts

CEO3: To be able to understand and use the Verilog HDL programming fundamentals

CEO4: To be able to use the coding styles in designing any hardware using Verilog HDL

CEO5: To understand the need for synthesis for hierarchical design of digital systems.

UNIT - 1: FPGA ARCHITECTURES

FPGA Design Flow, Roles of FPGA in digital design, Hierarchical design, FPGA architectures – Configurable logic blocks - Configurable I/O blocks – Programmable interconnect – clock circuitry – Xilinx FPGA architecture – Programming Technologies: Anti-fuse, SRAM, EPROM,EEPROM.

UNIT - 2: FINITE STATE MACHINES (FSM)

Top Down Design - State Transition Table - State Assignments for FPGAs - Problem of Initial State Assignment for one hot Encoding. Derivations of State Machine Charges - Charts with a PAL - Alternative Realization for State Machine Chart using Microprogramming - Linked State Machines. One hot State Machine - Petrinetes for State Machines – Basic Concepts of State Machine - Case Study - Meta Stability - Synchronization and Debouncing.

UNIT - 3: VERILOG HDL - FUNDAMENTALS

Hardware modeling with the verilog HDL, modeling primitives, different types of description. Logic system, data types and operators for modeling in verilog HDL. Verilog Models of propagation delay and net delay path delays and simulation, nets, register variables, expressions and operators, assignments and compiler directives.

UNIT - 4: VERILOG-MODELING STYLES

Gate level modeling, Switch level modeling, User Defined Primitives. **Behavioral Modeling** - Procedural Assignment - Procedural Continuous Assignments - Procedural Timing Controls and Synchronization - Intra-Assignment - Delay- Blocking Assignment - Intra-Assignment Delay - Non-Blocking Assignment - Simulation of Simultaneous Procedural Assignments - Repeated Intra Assignment Delay - Indeterminate Assignments and Ambiguity - Behavioral Models of Finite State Machines.

UNIT - 5: SYNTHESIS

HDL-based synthesis - technology-independent design, styles for synthesis of combinational and sequential logic, synthesis of finite state machines, synthesis of gated clocks, design partitions and hierarchical structures. Design Examples.

COURSE OUTCOMES:

On successful completion of the course the student will be able to,		POs related to COs
CO1	Translate a software application into hardware logic for FPGA architectures.	PO1, PO2 ,PO3, PO4
CO2	Demonstrate knowledge and design of FSM concepts.	PO1, PO2, PO4
CO3	Understand, analyze and utilize the basics of Verilog HDL in programming.	PO1, PO2, PO4
CO4	Analyze and understand the concepts of Verilog modeling and design a digital system.	PO1, PO2, PO3, PO4
CO5	Understand and apply the concept of synthesis in a system design.	PO1, PO2, PO3, PO4

Text Book:

1. Field Programmable Gate Array Technology, 2/e, 2009, S.Trimberger, Springer, NewDelhi
2. Verilog HDL, 2/e, 2003, Samir Palnitkar, Pearson Education, New Delhi.

Reference Books:

1. Field Programmable Gate Array, 3/e, 2007, S.Brown, R.Francis, J.Rose, Z.Vransic, BSP, Hyderabad.
2. Digital Design Using Field Programmable Gate Array, 2/e, 1994, P.K.Chan & S. Mourad, Prentice Hall.
3. J Bhaskar, "A Verilog HDL Primer (3rd edition)", Kluwer, 2005.
4. M.D.Ciletti, "Modeling, Synthesis and Rapid Prototyping with the Verilog HDL", PHI, 1999.
5. Digital Design Principles and Practices , 3rd Ed., 2005, John F. Wakerly, PHI/ Pearson Education Asia, New Delhi.

CO-PO Mapping

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	-	-	-	-	-	-	-	-
CO2	3	3	-	2	-	-	-	-	-	-	-	-
CO3	3	2	-	2	-	-	-	-	-	-	-	-
CO4	3	3	3	2	-	-	-	-	-	-	-	-
CO5	3	3	3	3	-	-	-	-	-	-	-	-
CO*	3	2.8	3	2.2	-	-	-	-	-	-	-	-

I year M.Tech I Semester

L	T	P	C
3	*0*	*0*	*3*

20MVSD14A Physics for VLSI Devices (Core Elective-I)

Course Educational Objectives:

CEO1: To provide knowledge on basics of Physics
CEO2: To develop skill to analyze electrical properties of devices
CEO3: To develop skill to design the MOSFET's.
CEO4: To inculcate skill in device modeling.
CEO5: To develop skill to apply the concept of bipolar devices.

UNIT - 1: Basic Device Physics

Electrons and holes in silicon, P-N junction, MOS capacitor, High-field effects.

UNIT - 2: MOSFET Devices

Long-channel MOSFETs, Short-channel MOSFETs.
CMOS Device Design: MOSFET Scaling, Threshold voltage, MOSFET channel length.

UNIT-3: CMOS Performance Factors: Basic CMOS circuit elements, Parasitic elements, Sensitivity of CMOS delay to device parameters, Performance factors of advanced CMOS devices.

UNIT-4: Bipolar Devices:

N-P-N Transistors, Ideal current-voltage characteristics, Characteristics of a typical N-P-N transistor, Bipolar device models for circuit and time-dependent analyses, Breakdown voltages.

UNIT-5 Bipolar Device Design:

Design of the emitter design, Design of the base region, Design of the collector design, Modern bipolar transistor structures.

COURSE OUTCOMES:

On successful completion of the course the student will be able to,		**POs related to COs**
CO1	Identify appropriate method and design of electronic devices.	PO1, PO2
CO2	Demonstrate knowledge on fundamentals of devices and cicuits	PO1, PO2
CO3	Analyze the effect for CMOS designing and its parasitic elements	PO1, PO2
CO4	Analyzing the transistors and its V-I Characteristics	PO1, PO2
CO5	Understand and designing of transistors terminals	PO1, PO2

TEXT BOOKS

1. Yuan Taur, Tak.H.Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press.

REFERENCE BOOKS

1. Donald Neamen, Semiconductors Physics and Devices, Tata Mc Graw Hill, 2003.
2. Tyagi, Introduction to Semiconductor Materials and Devices, Wiley Publications, 2002.
3. Semiconductor Devices, Basic Principles Jasprit Singh, Wiley Publications, 2001.
4. S.M. Sze (Ed), Physics of Semiconductor Devices, 2nd Edition, Wiley Publications, 1998.

5. Analysis and Design of Analog Integrated Circuits 4/e, Paul R. Gray, Paul J. Hurst, Robert G Meyer, 2001, Wiley Publications
6. Physics of Semiconductor Devices 3/e S. M. Sze, Wiley Publications, 2007.

CO-PO Mapping

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	-	-	-	-	-	-	-	-	-	-
CO2	2	2	-	-	-	-	-	-	-	-	-	-
CO3	2	2	-	-	-	-	-	-	-	-	-	-
CO4	2	2	-	-	-	-	-	-	-	-	-	-
CO5	3	2	-	-	-	-	-	-	-	-	-	-
CO*	2.4	2	-	-	-	-	-	-	-	-	-	-

I Year M.Tech I Semester

L	T	P	C
3	*0*	*0*	*3*

20MVSD14B Hardware Software Co-Design (Core Elective-I)

Course Educational Objectives:

CEO1: To obtain knowledge on co-design issues and synthesis algorithms.
CEO2: To acquire knowledge and skills on prototyping, emulation and target architectures.
CEO3: To be able to understand tools for processor architecture.
CEO4: To be able to understand and analyze the specification and verification tools.
CEO5: To understand the utilize the object oriented programming for hardware design.

UNIT - 1: Co-Design Issues and Co-Synthesis Algorithms

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology, Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT - 2: Prototyping, Emulation and Target Architecture

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure, Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT - 3: Compilation Techniques and Tools for Embedded Processor Architectures

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT - 4: Design Specification and Verification

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT - 5: Objected Oriented Hardware Design

Motivation for object oriented techniques, object oriented design strategies, modeling hardware components as classes, designing specialized components, data decomposition, and Processor example.

COURSE OUTCOMES:

On successful completion of the course the student will be able to,		POs related to COs
CO1	Acquire the knowledge about Co design issues and algorithms	PO1, PO2
CO2	Able to learn the prototyping, emulation and target architecture	PO1, PO2
CO3	Understand the compilation tools and techniques.	PO1, PO2
CO4	Analyze and utilize design specification and verification.	PO1, PO2, PO3
CO5	Understand, apply the concepts in designing hardware using object oriented techniques.	PO1, PO2, PO3

Text Book:

1. Jorgen Staunstrup, "Hardware / Software Co- Design Principles and Practice", Wayne Wolf , 2009, Springer.
2. Giovanni De Micheli, Mariagiovanna Sami, "Hardware / Software Co- Design", 2002, Kluwer Academic Publishers

Reference Books:

1.Specification and Design of Embedded Systems, 1/e, 2007, Daniel D. Gajaski, Frank Vahid, Sanjiv
2. Narayan, Jie Gong, Pearson Education, New Delhi.
3.Hardware/Software Co-Design, 1/e, 2002, Giovanni De Micheli, Ern st, Wolf, Morgan Kaufmann (Academic Press), San Diego, United States of America.
4.A Practical Introduction to Hardware/Software Codesign, 2/e, 2012, Patrick Schaumont, Springer, New Yark, London.
5.Hardware/software co-design and co-verification, 1/e, 1997, Jean-Michel Bergé, Kluwer Academic Publishers, United States of America.
6.System Level Hardware/Software Co-Design: An Industrial Approach, 1/e, 1997, Joris van den Hurk.

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	-	-	-	-	-	-	-	-	-	-
CO2	3	2	-	-	-	-	-	-	-	-	-	-
CO3	3	3	-	-	-	-	-	-	-	-	-	-
CO4	3	2	2	-	-	-	-	-	-	-	-	-
CO5	3	2	3	-	-	-	-	-	-	-	-	-
CO*	3	2.2	2.5	-	-	-	-	-	-	-	-	-

I year M.Tech I Semester **L T P C**

3 0 0 3

20MVSD14C Mixed Signal Design (Core Elective I)

Course Educational Objectives:

CEO1: To provide knowledge on Switched capacitors Circuits and Operation and Analysis, PLLS.
CEO2: To provide knowledge Data Converter Fundamentals, Nyquist Rate A/D Converters.
CEO3: To analyze the Continuous-Time Filters.
CEO4: To provide knowledge on Data Converter Fundamentals and to design A/D Converters.
CEO5: To develop skill to design Oversampling Converters ,Continuous-Time Filters, CMOS Transconductors Using Triode and Active Transistors and MOSFET-C Filters.

UNIT-1: Switched Capacitor Circuits Design:Introduction to Switched Capacitor circuits-basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT-2: Phased Lock Loop (PLL): Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non- idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT-3: D/A Converter Fundamentals:DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT-4: : A/D Converter Fundamentals Nyquist Rate A/D Converters:Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT-5: Oversampling Converters:Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multi-bit quantizers, Delta sigma D/A.
Continuous-Time Filters:Introduction to Gm-C Filters, Bipolar Transconductors, CMOS transconductors Using Triode and Active Transistors, BiCMOS Tran conductors, MOSFET-C Filters.

Course Outcomes:

On successful completion of the course the student will be able to,		**POs related to COs**
CO1	Demonstrate knowledge on concepts of Switched Capacitor circuits.	PO1, PO2
CO2	Design and analysis of Nyquist Rate A/D Converters	PO1, PO2, PO3, PO5
CO3	Analyze the Continuous-Time Filters.	PO1, PO2, PO3, PO5
CO4	Knowledge on Data Converter Fundamentals and to design A/D Converters	PO1, PO2, PO4
CO5	Design Oversampling Converters, Continuous-Time Filters, CMOS Transconductors Using Triode, Active Transistors and MOSFET-C Filters	PO1,PO2, PO4,PO5

Text Books

1.Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2.Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013.

Reference Books

1. CMOS Mixed-Signal Circuit Design – R. Jacob Baker, Wiley Interscience, 2009.
2. CMOS Analog Circuit Design –Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. P. R. Gray and R. G. Meyer, Analysis and design of Analog Integrated circuits 4th Edition,Wiley Student Edition, 2001.
4. R.Jacob Baker,H.W.Li, and D.E. Boyce CMOS Circuit Design ,Layout and Simulation, Prentice-Hall of India,1998.
5. Mohammed Ismail and Terri Faiz Analog VLSI Signal and Information Process, McGraw-HillBook company,1994.

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	-	-	-	-	-	-	-	-	-	-
CO2	3	3	3	-	2	-	-	-	-	-	-	-
CO3	3	3	2	-	2	-	-	-	-	-	-	-
CO4	3	3	-	2	-	-	-	-	-	-	-	-
CO5	3	2	-	3	2	-	-	-	-	-	-	-
CO*	3	2,8	2.5	2.5	2	-	-	-	-	-	-	-

I year M.Tech I Semester

L	T	P	C
3	*0*	*0*	*3*

20MVSD14D ADVANCED DIGITAL SYSTEM DESIGN (Core Elective-I)

Course Educational Objectives:

CEO1: To provide knowledge on Fundamentals of Digital System Methodology
CEO2: To perform analysis and design of Asynchronous sequential circuits.
CEO3: To develop skill to do the synthesis of combinational circuits.
CEO4: To acquire the ideas in developing a micro-programmed control for digital systems
CEO5: To utilize the design concepts of Verilog for modelling a hardware.

UNIT–1:
INTRODUCTION TO DIGITAL DESIGN METHODOLOGY: Design specifications, partition, simulation, gate level synthesis and technology mapping, post synthesis design validation and timing verification, test generation and fault simulation, placement and routing, physical and electrical design rule checks, parasitic extraction, design sign-off, technology options.

UNIT -2:
ASYNCHRONOUS SEQUENTIALCIRCUIT DESIGN: Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment- transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits.

UNIT -3:
SYNHESIS OF COMBINATIONAL AND SEQUENTIAL LOGIC: Logic and RTL synthesis, synthesis of combinational ,synthesis of sequential logic with latches and flip flops, synthesis of three state devices and bus interfaces, synthesis of explicit state machines.

UNIT -4:
MICROPROGRAMED DESIGN: Classical Microprogramming with Modem Technology; Enhancing the Control Unit; The 2910 Microprogram Sequencer; Choosing a Microprogram Memory; A Development System for Microprogramming; Designing a Micro-programmed Minicomputer.

UNIT –5:
HARDWARE MODELLING WITH VERILOG HDL: Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modeling – compilation and simulation of Verilog code –Test bench -Realization of combinational and sequential circuits using Verilog – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor.

Course Outcomes:

On successful completion of the course the student will be able to,		POs related to COs
CO1	Able to understand the Fundamentals of Digital System Methodology	PO1, PO2
CO2	Ability to analyze and design asynchronous sequential designs.	PO1, PO2, PO3, PO4
CO3	Apply the concepts, analyze and design of combinational and sequential designs.	PO1, PO2, PO3, PO4
CO4	Utilize the techniques to develop a micro-programmed control for digital systems	PO1, PO2, PO3
CO5	Understand, apply the concepts of Verilog to Design Hardwares.	PO1, PO2, PO3

Text books

1.Michael D.Ciletti Advanced digital design with Verilog HDL Pearson 2017
2. Franklin P. Prosser and David E. Winkel, "The Art of Digital Design", Prentice Hall.
3. Roth, “Digital System Design using VHDL”, Mc. Graw Hill, 2000

CO-PO Mapping

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	-	-	-	-	-	-	-	-	-	-
CO2	2	3	3	2	-	-	-	-	-	-	-	-
CO3	3	2	3	2	-	-	-	-	-	-	-	-
CO4	3	2	3	-	-	-	-	-	-	-	-	-
CO5	3	2	3	-	-	-	-	-	-	-	-	-
CO*	2.8	2.2	3	2	-	-	-	-	-	-	-	-

I year M.Tech I Semester

L	T	P	C
3	*0*	*0*	*3*

20MVSD15A Design for Testability and Testing (Core Elective-II)

Course Educational Objectives:

CEO1: To provide knowledge on

- Design for testability
- Fault modeling and simulation
- Test analysis for digital circuits

CEO2: To develop skill to analyze Design strategies for testability

CEO3: Contribute to multidisciplinary scientific work in the field of testing of Stuck at Faults for digital Circuits.

CEO4: To inculcate skill to develop New testing Strategies for digital and mixed signal circuits and systems.

CEO5: To apply appropriate techniques for Modeling of Combinational and Sequential Circuit Testing.

UNIT - 1: Introduction to DFT Fundamentals

Modeling: Modeling Digital Circuits at Logic Level - Register Level and Structural Models - Levels of Modeling. Logic Simulation - Types of Simulation - Delay Models - Element Evaluation - Hazard Detection - Gate Level Event Driven Simulation.

UNIT - 2: Fault Modeling

Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location, Fault Dominance, the Single Stuck-Fault Model, The Multiple Stuck-Fault Model.

UNIT - 3: Fault Simulation

Fault Simulation Applications, General Fault Simulation Techniques, Fault Simulation for Combinational Circuits, Fault Sampling.

UNIT - 4: Testing for Single Stuck Faults

ATG for SSSFs in Combinational Circuits and Sequential Circuits, Testing for bridging faults, Functional Testing With Specific Fault Models, Vector Simulation- ATPG Vectors, Formats Compaction and Compression, Selecting ATPG Tool.

UNIT - 5: Design for Testability

Testability Trade Offs, Techniques, Scan Architectures and Testing, Controllability and Observability by means of Scan Registers, Generic Scan-Based Designs, Full Serial Integrated Scan, Storage Cells for Scan Designs, Board-Level and System-Level DFT Approaches, Boundary Scans Standards, Compression Techniques, Different Techniques, Syndrome Testing and Signature Analysis, Introduction to BIST Concepts.

COURSE OUTCOMES:

On successful completion of the course the student will be able to,		POs related to COs
CO1	Demonstrate advanced knowledge in: The basic faults that occur in digital systems, Testing of stuck at faults for digital circuits, Design for testability	PO1, PO2 ,PO3
CO2	Analyze testing issues in the field of digital system design critically for Conducting Research.	PO1, PO2
CO3	Solve engineering problems by modeling different faults for fault free Simulation in Digital circuits.	PO1, PO2, PO3
CO4	Apply appropriate research methodologies to develop New testing Strategies for digital and mixed signal circuits and systems.	PO1, PO2, PO4
CO5	Apply appropriate techniques, Resources and tools in, Modeling to Complex Engineering activities with an understanding of the limitations.	PO1, PO4, ,PO5

Text Book:

1. MironAbramovici, Melvin A. Breur, Arthur D.Friedman, "Digital Systems Testing and Testable Design", Wiley, 1st Edition, 1994.
2. Alfred L. Crouch, "Design for Test for Digital ICs & Embedded Core Systems", Prentice Hall PTR, 1st Reprint Edition, 1999.

Reference Books:

1. Robert J.Feugate, Jr., Steven M.Mclntyre, "Introduction to VLSI Testing", Prentice Hall, 1st Illustrated Edition,1998.
2. Introduction to VLSI design, International Edition, Eugine D. Fabricus, Mc Graw Hill, New Delhi.

CO-PO MAPPING

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2	-	-	-	-	-	-	-	--	-
CO2	3	2	-	-	-	-	-	-	-	-	--	-
CO3	3	3	2	-	-	-	-	-	-	-	--	-
CO4	3	3	-	2	-	-	-	-	-	-	--	-
CO5	3	-	-	2	2	-	-	-	-	-	--	-
CO*	3	2.8	-	2	2	-	-	-	-	-	--	-

I year M.Tech I Semester

L	T	P	C
3	*0*	*0*	*3*

20MVSD15B DIGITAL SIGNAL PROCESSING FOR VLSI (Core Elective-II)

COURSE EDUCATIONAL OBJECTIVES:

CEO1: To Gain knowledge in DSP system and understand the concept of Pipelining and Parallel processing of FIR filters.
CEO2: To study the concept of Retiming, Algorithmic strength reduction.
CEO3: To understand the concept of Fast Convolution, Pipelining and Parallel processing of IIR filter.
CEO4: To Study Bit-Level Arithmetic Architecture
CEO5: To understand Numerical Strength Reduction, Synchronous, Wave and Asynchronous Pipelining

UNIT 1: INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs – critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT 2 :RETIMING, ALGORITHMIC STRENGTH REDUCTION

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT 3: FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with powerof-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT4: BIT-LEVEL ARITHMETIC ARCHITECTURES

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon‟s bit-serial multipliers using Horner‟s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner‟s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

UNIT 5: NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING

Numerical strength reduction – sub-expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

COURSE OUTCOME:

After successful completion of the course the students will be able to,

CO1: Demonstrate knowledge in DSP systems and Analyze and design pipelining and parallel processing of FIR filters

CO2: Demonstrate and analyze retiming, algorithmic strength reduction.

CO3: Demonstrate knowledge in Fast convolution and Analyze and design pipelining and parallel Processing of IIR filters

CO4: Analyze and develop Bit-level Arithmetic Architecture.

CO5: Apply and develop various techniques required for VLSI signal processing

Text Book

1. Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and implementation", Wiley, Interscience, 2007.

Reference Book:

1. U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004

CO-PO MAPPING

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	-	-	-	--	-	-	-	-	--	-
CO2	3	3	-	2	-	--	-	-	-	-	--	-
CO3	3	3	2	2	-	--	-	-	-	-	--	-
CO4	3	3	2	2	-	--	-	-	-	-	--	-
CO5	3	2	2	2	2	--	-	-	-	-	--	-
CO*	3	2.6	2	2	2	--	-	-	-	-	--	-

I Year M.Tech I Semester

L	T	P	C
3	*0*	*0*	*3*

20MVSD15C RF IC DESIGN (Core Elective-II)

Course Objectives:

CEO1: Build an understanding of the fundamental concepts of RF electronics.
CEO2: Familiarize the student with the basic taxonomy and terminology of the matching and biasing network.
CEO3: Introduce the student to design RF amplifiers.
CEO4: Allow the student to analyze the different noises related RF design.
CEO5: Familiarize the student with different RF circuit measurements.

UNIT 1: RF ELECTRONIC CONCEPTS.

Importance of radio frequency design - materials used for different RF electronic devices - RF Microwave versus DC or AC signals — RF behavior of passive components: R, L, C transformer – Chip components: Circuit board consideration –Chip resistors-Chip capacitors-Surface mounted inductors- resonant circuits - RF behavior of active components: BJT - MOSFET- Basics of RF/Microwave antenna and array - Basics of smith chart calculations – Smith circle.

UNIT 2: MATCHING AND BIASING NETWORK

RF Impedance matching using discrete component – Design of matching circuits using lumped and distributed elements - Frequency response - Quality factor- T and Pi matching networks, micro-strip line matching network - BICMOS biasing networks – Impedance computing using Smith chart : From reflection coefficient to load impedance – Parametric reflection coefficient equation – Graphical representation – Impedance transformation – Admittance transformation

UNIT 3: DESIGN OF AMPLIFIERS AND MIXERS

Amplifier classes of operation and biasing networks-Stability and noise considerations in active network – Rollett's stability factor - Gain considerations in amplifiers – Linear and non linear design of RF amplifiers - Design philosophy of Low noise amplifiers (Qualitative treatment only) – Negative resistance oscillator – Conditions leading to oscillator's stable operation – Basics of mixer circuits and types.

UNIT 4: ELECTROMAGNETIC COMPATIBILITY, EMI AND NOISE

EMC definitions and units of parameters – EMI: Conducted and Radiated EMI emission and Susceptibility – transient EMI- ESD – Radiation hazards – Mismatch related concepts - Radiation losses - Noise: Thermal, shot, flicker, phase noise - IP2- IP3 - Sensitivity- Noise contributions of various structures on RFIC - Non linearities in circuits - Passive inter modulation distortion – Inter Symbol Interference.

UNIT 5: RF CIRCUITS MEASUREMENTS

RF performance metrics : S Parameter Models - Input and output VSWR – Noise Figure - Directivity - Insertion loss – Isolation loss – coupling factor - RF mismatch factor – Sources of Uncertainty — Considerations for attenuation measurements – Noise measurements – Spectrum analyzer measurements - RF antenna measurements.

Course Outcomes:

On successful completion of the course the student will be able to,

CO	On successful completion of the course the student will be able to,	PO
CO.1	Demonstrate knowledge on the basic RF behavior of active and passive components.	P01
CO.2	Design of matching circuits using lumped and distributed elements.	P01,P03
CO.3	Design and investigate Linear and non linear RF amplifiers.	P01,P03, PO4
CO.4	Demonstrate knowledge on noise contributions of various structures on RFIC.	PO1,P04
CO.5	Demonstrate knowledge on RF performance metrics.	P01,P04

TEXT / REFERENCE BOOKS

1. Matthew M. Radmanesh " Radio frequency & Microwave Electronics illustrated", Prentice Hall, 2001.
2. Reinhold Ludwig, Gene Bogdanov, "RF circuit design, theory and applications", Pearson Asia Education, 2nd edition, 2009.
3. RF Microelectronics by Behzad Razavi. Prentice Hall,1997.

CO-PO MAPPING

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	-	-	-	-	-	-	-	-	-	--	-
CO2	3	-	1	-	-	-	-	-	-	-	--	-
CO3	3	-	1	1	-	-	-	-	-	-	--	-
CO4	3	-	-	1	-	-	-	-	-	-	--	-
CO5	3	-	-	1	-	-	-	-	-	-	--	-
CO*	3	-	1	1	-	-	-	-	-	-	--	-

I Year M.Tech I Semester

L	T	P	C
3	*0*	*0*	*3*

20MVSD15D Asynchronous System Design (Core Elective-II)

Course Educational Objectives:

CEO1: This subject introduces the fundamentals and performance of Asynchronous system
CEO2: To familiarize the dependency graphical analysis of signal transmission graphs
CEO3: To learn software languages and its syntax and operations for implementing Asynchronous Designs
CEO4:To develop skill to apply the concept of Sequential Circuit in asynchronous
CEO5:To acquire knowledge on asynchronous hardware synthesis concepts

UNIT - 1: Introduction to Handshake Process Fundamentals: - Handshake protocols Muller C-element, Muller pipeline, Circuit implementation Styles, theory. Static data-flow structures: Pipelines and rings, Building blocks, examples

UNIT - 2: Handshake circuit implementations Simulation Performance: A quantitative view of performance, quantifying performance, Dependency graphic analysis. Handshake circuit implementation: Fork, join, and merge, Functional blocks, mutual exclusion, arbitration and metastability, Function blocks – The basics, MUX and DEMUX

UNIT - 3: Speed-independent control circuits Asynchronous sequential circuits , Speed-independent control circuits: Signal Transition graphs, Basic Synthesis Procedure, Implementation using state-holding gates, Summary of the synthesis Process, Design examples using Petrify. Advanced 4-phase bundled ,data protocols and circuits: Channels and protocols, Static type checking, more advanced latch control circuits.

UNIT - 4: Introduction to Tangram and handshake circuits and High-level languages and tools High-level languages and tools: Concurrency and message passing in CSP, Tangram program examples, Tangram syntax-directed compilation, Martin's translation process, Using VHDL for Asynchronous Design. An Introduction to Balsa: Basic concepts, Tool set and design flow, Ancillary Balsa Tools

UNIT- 5: An Asynchronous Hardware Synthesis System The Balsa language: Data types, Control flow and commands, Binary/Unary operators, Program structure. Building library Components: Parameterized descriptions, Recursive definitions. A simple DMA controller: Global Registers, Channel Registers, DMA control structure, The Balsa description.

COURSE OUTCOMES:

On successful completion of the course the student will be able to,		POs related to COs
CO1	understand the fundamentals of Asynchronous protocols	PO1, PO3,
CO2	analyse the performance of Asynchronous System and implement handshake circuits	PO1,PO2, PO3
CO3	understand the various control circuits and Asynchronous system modules	PO1, PO2, PO3
CO4	gain the experience in using high level languages and tools for Asynchronous Design	PO1, PO2, PO5,P09
CO5	learn commands and control flow of Balsa language for implementing Asynchronous Designs	PO1, PO4,PO5,PO9

Text Book:

1. Asynchronous Circuit Design- Chris. J. Myers, John Wiley & Sons, 2001.
2. Handshake Circuits An Asynchronous architecture for VLSI programming – Kees Van Berkel Cambridge University Press, 2004

Reference Books:

1. Principles of Asynchronous Circuit Design-Jens Sparso, Steve Furber, Kluver Academic Publishers, 2001.
2. Asynchronous Sequential Machine Design and Analysis, Richard F. Tinder, 2009.
3. A Designer's Guide to Asynchronous VLSI, Peter A. Beerel, Recep O. Ozdag, Marcos Ferretti, 2010.
4. Recent literature in Asynchronous System Design.

CO-PO MAPPING

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	-	3	-	-	-	-	-	-	-	--	-
CO2	3	3	2	-	-	-	-	-	-	-	--	-
CO3	3	3	3	-	-	-	-	-	-	-	--	-
CO4	3	3		-	-	-	-	-	-	-	--	-
CO5	3	3	-	2	-	-	-	-	-	-	--	-
CO*	3	3	2.67	2	-	-	-	-	-	-	--	-

I M.Tech I Semester

L	T	P	C
3	*0*	*0*	*1*

20MVSD16 RESEARCH METHODOLOGY AND IPR

Course Educational Objectives:

CEO1: To provide knowledge on various types of Research Problems
CEO2: To acquire knowledge on Plagiarism and Research ethics
CEO3: To be able to understand the basics of Research Proposals
CEO4: To introduce fundamental aspects of Intellectual property Rights to students who are going to play a major role in development of innovative projects in industries
CEO5: To disseminate knowledge on copyrights and its related rights and registration aspects

Unit 1:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

Unit 2:

Effective literature studies approaches, analysis of Plagiarism, Research ethics,

Unit 3 :

Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

Unit 4:

Nature of Intellectual Property: Patents, Designs, Trademarks and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents and Patenting under PCT.

Unit 5 :

Introduction to Copyrights – Principles of Copyright – Subject Matters of Copyright – Rights Afforded by Copyright Law –Copyright Ownership – Transfer and Duration – Right to Prepare Derivative Works –Rights of Distribution – Rights of performers – Copyright Formalities and Registration – Limitations – Infringement of Copyright – International Copyright Law- Semiconductor Chip Protection Act.

COURSE OUTCOMES:

On successful completion of the course the student will be able to,		**POs related to COs**
CO1	Understand and analyze various types of Research Problems	PO1, PO2
CO2	Demonstrate knowledge on Plagiarism and Research ethics	PO1, PO2, PO8
CO3	Understand and analyze the basics of Research Proposals	PO1, PO2, PO8
CO4	Demonstrate knowledge on patent and PCT	PO1, PO2, PO8
CO5	Demonstrate knowledge on copyrights for their innovative works	PO1, PO2, PO8

TEXT BOOKS

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science& engineering students'".
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
3. Robert P. Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property in New Technological Age",2016.
4. Deborah E.Bouchoux: "Intellectual Property". Cengage learning, New Delhi

REFERENCE BOOKS

1. Ranjit Kumar, 2nd Edition , "Research Methodology: A Step by Step Guide for beginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd,2007.
3. Robert P. Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property in New Technological Age",2016.
4. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008.
5. Prabhuddha Ganguli: ' Intellectual Property Rights" Tata Mc-Graw – Hill, New Delhi

CO-PO MAPPING

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	-	-	-	-	-	-	-	-	-	-
CO2	3	2	-	-	-	-	-	2	-	-	-	-
CO3	3	2	-	-	-	-	-	2	-	-	-	-
CO4	3	2	-	-	-	-	-	3	-	-	-	-
CO5	3	2	-	-	-	-	-	3	-	-	-	-
CO*	3	2	-	-	-	-	-	2.5	-	-	-	-

I M.Tech II Semester

L	T	P	C
0	*0*	*3*	*2*

20MVSD17 Analog IC Design Lab

Course Educational Objectives:

- To analyze the characteristics of NMOS and PMOS transistors to understand their behavior.
- Gain the practical hands-on experience on design of CG, CD and CS Amplifiers.
- To design, simulate and analyze the current mirror, Op-Amp and Cascode Amplifiers

List of Experiments:

1. Characteristics of NMOS & PMOS Transistors
2. Design of and analysis of Common Source Amplifier with different Loads
3. Design of and analysis of Common Gate Amplifier
4. Design of and analysis of Common Drain Amplifier
5. Design of Single stage Cascode Amplifiers
6. Design of Current Mirrors
7. Design of Differential Amplifiers with Different Loads
8. Design of Two stage Op-Amp.
9. Design of Telescopic Cascode Op-Amp
10. Design of Folded Cascode Op-Amp

Tools Required:

1. Cadence/ Mentor Graphics/Tanner EDA or any other CAD tools.
2. Personal Computers with Core i Processors with minimum 4 GB RAM.

Course Outcomes:

On successful completion of course the students will be able to		POs related to COs	PSOs
CO1	Demonstrate knowledge of MOS transistors, Op-Amp, Current mirror and Cascode Amp.	PO1	PSO1
CO2	Analyze the behavior of MOS transistors, Op-Amp, Current mirror and Cascode Amp.	PO2	PSO1
CO3	Design the circuits which are used for successful implementation of various Analog ICs	PO3	PSO1
CO4	Conduct investigation on complex analysis of MOS transistors, Op-Amp, Current mirror and Cascode Amp.	PO4	PSO1
CO5	Utilize the appropriate CAD tool to design the Amp.	PO5	PSO2
CO6	Follow ethical principles in analyzing and implementing functionalities of various circuits.	PO8	PSO2
CO7	Do experiments effectively as an individual and as a member in a group.	PO9	PSO2
CO8	Communicate verbally and in written form, the understandings about the experiments.	PO10	PSO2
CO9	Continue to update the skills related to the program for various applications during the life time.	PO12	PSO2

CO-PO MAPPING

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	-	-	-	-	-	-	-	-	-	-	-
CO2	-	3	-	-	-	-	-	-	-	-	-	-
CO3	-	-	3	-	-	-	-	-	-	-	-	-
CO4	-	-	-	3	-	-	-	-	-	-	-	-
CO5	-	-	-	-	3	-	-	-	-	-	-	-
CO6	-	-	-	-	-	-	-	3	-	-	-	-
CO7	-	-	-	-	-	-	-	-	3	-	-	-
CO8	-	-	-	-	-	-	-	-	-	3	-	-
CO9	-	-	-	-	-	-	-	-	-	-	-	3
CO*	3	3	3	3	3	-	-	3	3	3	-	3

I year M.Tech I Semester

L	T	P	C
0	*0*	*3*	*2*

20MVSD18 HDL Programming Lab

Course Educational Objectives:

CEO1: Gain the practical hands-on experience on verilog HDL programming
CEO2: To design, simulate and verify the combinational logic designs using verilog HDL.
CEO3: To design, simulate and verify the sequential logic designs using verilog HDL.

List of Experiments:

1. Adder/ Subtractor
2. Multiplexer/ Demultiplexer
3. Encoder/ Priority Encoder
4. Code Converter
5. Flipflops
6. Shift Register/ Universal Shift Register
7. Comparator
8. Upcounter/ Downcounter
9. UDPs
10. Memory – ROM, RAM
11. Array Multiplier/ Array Multiplier With Pipelining
12. Fir Filter/ Fir Filter With Pipelinig
13. MAC unit
14. Hardware implementation of any experiments using FPGA

Tools Required:

1. Xilinx Vivado/ Altera Tools
2. Personal Computers with Core i Processors with minimum 4 GB RAM.
3. FPGA Hardware

Course Outcomes:

On successful completion of course the students will be able to		POs related to Cos
CO1	Demonstrate knowledge on programming the combinational and sequential circuit designs	PO1
CO2	Analyze the functionality of digital circuits	PO2
CO3	Design the circuits which are used for successful implementation of simple & complex systems	PO3
CO4	Conduct investigation and test the functionality on implementation of combinational and sequential elements.	PO4
CO5	Select appropriate FPGA hardware and procedure to analyze and implement Digital circuits	PO5
CO6	Follow ethical principles in analyzing and implementing functionalities of various circuits	PO8
CO7	Do experiments effectively as an individual and as a member in a group.	PO9
CO8	Communicate verbally and in written form, the understandings about the experiments.	PO10
CO9	Continue to update the skills related to the program for various applications during the life time.	PO12

CO-PO MAPPING

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	-	-	-	-	-	-	-	-	-	-	-
CO2	-	3	-	-	-	-	-	-	-	-	-	-
CO3	-	-	3	-	-	-	-	-	-	-	-	-
CO4	-	-	-	3	-	-	-	-	-	-	-	-
CO5	-	-	-	-	3	-	-	-	-	-	-	-
CO6	-	-	-	-	-	-	-	3	-	-	-	-
CO7	-	-	-	-	-	-	-	-	3	-	-	-
CO8	-	-	-	-	-	-	-	-	-	3	-	-
CO9	-	-	-	-	-	-	-	-	-	-	-	3
CO*	3	3	3	3	3	-	-	3	3	3	-	3

I year M.Tech II Semester

L	T	P	C
3	*0*	*0*	*3*

20MVSD21 LOW POWER VLSI DESIGN

Course Educational Objectives:

CEO1: To obtain knowledge on low power design and Bi-CMOS process
CEO2: To acquire knowledge on low voltage aproaches.
CEO3: To be able to understand the CMOS/Bi-CMOS logic gates.
CEO4: To be able to analyze the latches and flip-flop circuit's behavior.
CEO5: To utilize the special techniques for low power design.

UNIT-1: Low Power Design Over View & BICMOS Processes

Introduction to low voltage & low power design – Limitations - BiCMOS processes - Integration and Isolation considerations - Integrated Analog/Digital CMOS Process - Sources of power dissipation on Digital Integrated circuits.

UNIT-2: Low-Voltage/Low Power CMOS/ BICMOS Processes

Emerging Low power approaches - Deep submicron processes - SOI CMOS - lateral BJT on SOI - future trends and directions of CMOS/Bi-CMOS processes & Introduction to MOSFET models

UNIT-3: CMOS and Bi-CMOS Logic Gates

Conventional CMOS and Bi-CMOS logic gates – Low voltage low power logic circuits - Comparison of advanced Bi-CMOS Digital circuits. ESD free Bi-CMOS - Digital circuit operation and comparative Evaluation - Transistor and gate sizing.

UNIT-4: Low Power Latches and Flip Flops

Evolution of Latches and Flip flops - Quality measures for latches and Flip flops - Design perspective.

UNIT-5: Special Techniques

Power dissipation in clock distribution - Power Reduction in Clock Networks - CMOS Floating Node - Low Power Bus - Delay Balancing - Low Power Techniques for SRAM.

COURSE OUTCOMES:

Course Outcomes		POs related to COs
CO1	Understand the concepts of low power and Bi-CMOS process.	PO1, PO2
CO2	Analyze the low voltage and low power methods	PO1, PO2
CO3	Apply the concepts to design CMOS and Bi-CMOS gates.	PO1, PO2,PO3
CO4	Able to design the low power latch and flip-flop	PO1, PO2, PO3
CO5	Evaluate the special low power Methodologies	PO1, PO2, PO3

Text Books:

1.CMOS/BiCMOS ULSI low voltage low power, 1/e, 2002, Yeo Rofail, Gohl, Pearson Education,NewDelhi.
2. Practical Low Power Digital VLSI Design,1/e, 2002, Gary K. Yeap, KAP, NewDelhi

Reference Books:

1. Basic VLSI Design, 3/e, Douglas A.Pucknell & Kamran Eshraghian, Prentice Hall of ind NewDelhi.
2. Digital Integrated circuits, 1/e, 1996, J.Rabaey, Prentice Hall of india, NewDelhi.
3. CMOS Digital ICs, 3/e, 2003, Sung-mo Kang and yusuf leblebici, Tata McGraw-Hill,New Delhi.
4. Dynamic Power Management Design Techniques and CAD Tools, 1/e, 1998, L. Benini and G. De micheli, Springer, Boston.
5. Low-Power Electronics Design, 1/e, 2005, C. Piguet, CRC Press, Florida.

CO-PO Mapping

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	-	2	-	-	-	-	-	-	-	-
CO2	2	3	-	-	-	-	-	-	-	-	-	-
CO3	2	3	3	-	-	-	-	-	-	-	-	-
CO4	3	2	3	-	-	-	-	-	-	-	-	-
CO5	2	3	3	-	-	-	-	-	-	-	-	-
CO*	2.4	2.6	3	2	-	-	-	-	-	-	-	-

I Year M.Tech I Semester

L	T	P	C
3	*0*	*0*	*3*

20MVSD22 ASIC DESIGN

Course Educational Objectives:

CEO1: To study the design flow of different types of ASIC
CEO2: To learn the Library Design concepts of ASIC
CEO3: To familiarize the different types of programming technologies and logic device
CEO4: To inculcate skill to investigate the ASIC Interconnects and to designing.
CEO5: To develop the skill in physical design, CAD tools, Partitioning.

UNIT - 1: OVERVIEW OF ASIC DESIGN and CMOS LOGIC

Introduction, Types of ASIC- Full custom ASIC- Standard cell-Based ASIC- Gate-Array Based ASIC- Channeled Gate Array- Channelless Gate Array- Structured Gate Array-Programmable Logic Devices, Field Programmable Gate Arrays, ASIC Design flow, CMOS transistors, Design rules, Combinational logic cells, Sequential logic cells, I/O Cells

UNIT - 2: ASIC LIBRARY DESIGN AND PROGRAMMABLE ASICS

Transistors as Resistors, Transistor Parasitic capacitance, Logical Effort, Library cell Design, Gate Array Design, Standard Cell Design, Datapath Cell Design, Static RAM, EPROM and EEPROM Technology

UNIT - 3: PROGRAMMABLE ASIC LOGIC CELLS AND I/O CELLS

Actel ACT, Xilinx LCA-XC3000 CLB, XC4000 Logic block XC5200 logic block, Altera FLEX, Altera MAX, DC output/input, AC output/input, Clock input, Xilinx I/O Block

UNIT - 4: ASIC INTERCONNECT AND DESIGN SOFTWARE

Altera max 5000 and 7000, Altera max 9000, Design systems, Logic synthesis, Half gate Asic, Comparison

UNIT – 5: ASIC CONSTRUCTION

Physical Design, CAD tools, System Partitioning, Estimating ASIC size, Power Dissipation, FPGA Partitioning, Partitioning methods.

COURSE OUTCOMES:

On successful completion of the course the student will be able to,		**POs related to COs**
CO1	Demonstrate Knowledge on different types of ASIC and to study about design rules in different Logic cells	PO1, PO2 ,PO3, PO5
CO2	Develop the different library design, cell design, EPROM and EEPROM Technologies	PO1, PO2
CO3	Analyze the different ASIC logic cell designs and I/O cells	PO1, PO2, PO3, PO5
CO4	Be familiar with ASIC interconnect like Altera Max, Logic Synthesis and Comparison	PO1, PO2, PO4
CO5	To gain knowledge in different partitioning, including circuit extraction of ASIC.	PO1, PO4,.

Text Book:

1. Integrated circuit engineering, 1/e, 1996, L.J.Herbst, OXFORD SCIENCE Publications.

Reference Books:

1. David A.Hodges, Analysis and Design of Digital Integrated Circuits (3/e), MGH 2004
2. H.Gerez, Algorithms for VLSI Design Automation, John Wiley, 1999
3. Jan.M.Rabaey et al, Digital Integrated Circuit Design Perspective (2/e), PHI 2003
4. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley& Sons, Newyork.
5. M.J.S. Smith: Application Specific Integrated Circuits, Pearson, 2003

CO-PO Mapping

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2	-	-	-	-	-	-	-	-	-
CO2	3	2	-	-	-	-	-	-	-	-	-	-
CO3	3	3	2	-	2	-	-	-	-	-	-	-
CO4	3	2	-	2	-	-	-	-	-	-	-	-
CO5	3	2	3	-	2	-	-	-	-	-	-	-
CO*	3	2.4	2.3	2	2	-	-	-	-	-	-	-

I year M.Tech II Semester

L	T	P	C
3	*0*	*0*	*3*

20MVSD23 Scripting Language for HDL

Course Educational Objectives:

CEO1: To understand the basics of PERL language.
CEO2: To gain the knowledge on operators, data structures and modules in PERL.
CEO3: To obtain and analyze the methods of Inter-process communication in PERL.
CEO4: To be able to understand, analyze and simulate the system using PERL debugger
CEO5: To know the other verification languages.

UNIT – 1: Introduction

Overview of Scripting Languages:PERL-CGI-VBScript-Java Script.

UNIT - 2: PERL

PERL Inroduction: Perl overview - Unary and binary operators – Statements : Simple - Compound- If-unless-given- Loop statements and goto. Concept of Pattern Matching - Perl Data Structures - Modules overview - Concept of Objects in Perl-Tied Variables: scalars - arrays-hashes- File handlers.

UNIT - 3: Inter Process Communication

Signals – Files – Pipes - SystemV IPC - Sockets. Concept of Perl Compilation: Lifecycle of Perl program - Compiling your code - Executing your code - Complier back ends - Code generation and tools. Line Interfacing: Command processing-Environment variables.

UNIT – 4: PERL Debugger

Using the Debugger - Debugger Commands - Debugger Customization - Unattended Execution -Internal & Externals Portable Functions. Extensive Exercises for Programming in PERL .

UNIT – 5:

Functional Verification coverage using design, verification languages and implementation standards: Verilog IEEE 1364, VHDL IEEE 1076, System Verilog IEEE 1800, Property Specific Language (PSL) IEEE 1850, System C™ IEEE 1666, Encryption IEEE 1735, e Verification Language IEEE 1647, Open Verification Methodology (OVM) and Universal Verification Methodology (UVM).

COURSE OUTCOMES:

On successful completion of the course the student will be able to		POs related to COs
CO1	Understand, analyze the PERL basics	PO1, PO2
CO2	Demonstrate knowledge on PERL operators, data structures and arrays.	PO1, PO2
CO3	Understand, analyze and utilize the tools and commands for inter-process communication.	PO1, PO2, PO3, PO4
CO4	Analyze and apply the concepts of PERL for debugging the code.	PO1, PO2, PO3, PO4

CO5	Understand and analyze the other verification tools and techniques.	PO1, PO2

Text Books:

1. Programming PERL, 3/e, 2000, Larry Wall, Tom Christiansen, John Orwant, Oreilly Publications.
2. Learning PERL,3/e, 2000,Randal L, Schwartz Tom Phoenix, Oreilly Publications.
3. The World of Scripting Languages, 2000, David Barron,Wiley Publications, New Delhi.
4. IEEE International Standard – Property Specification Standard, IEEE, 2nd Edition, 2010.

Reference Books:

1.Perl for Dummies, 4/e, 2011, Paul Hoffman, Wiley Publishers, New Delhi.
2.PERL Cookbook, 3/e, 2000,Tom Christiansen, Nathan Torkington,Oreilly Publications.
3.Perl by Example, 4/e, 2009,E.Quigley, Pearson Education, New Delhi.

CO-PO Mapping

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	-	-	-	-	-	-	-	-	-	-
CO2	2	3	-	-	-	-	-	-	-	-	-	-
CO3	3	3	2	2	-	-	-	-	-	-	-	-
CO4	3	3	2	2	-	-	-	-	-	-	-	-
CO5	3	2	-	-	-	-	-	-	-	-	-	-
CO*	2.8	2.8	2	2	-	-	-	-	-	-	-	-

I year M.Tech II Semester

L	T	P	C
3	*0*	*0*	*3*

20MVSD24 CAD FOR VLSI

Course Educational Objectives:

CEO1: To provide knowledge on Design Automation and methods for optimization.
CEO2: To acquire knowledge and skills on layout Partitioning and floor planning.
CEO3: To be able to understand the concept of placement and routing.
CEO4: To identify and utilize the other routing algorithms and compaction.
CEO5: To understand the need for the simulation, synthesis and verification.

UNIT-1: VLSI Physical Design Automation:
VLSI Design Cycle and New Trends - Physical Design Cycle and New Trends -Design Styles - System Packaging Styles.
General Purpose Methods for Combinational Optimization: Backtracking- Branch and Bound- Dynamic Programming- Integer Linear Programming- Local Search- Genetic Algorithms.

UNIT-2: Partitioning, Floor planning and Pin Assignment::
Problem Formulation-Classification of Partitioning Algorithms-Group Migration Algorithms-Simulated Annealing and Evolution – Floor planning-Chip planning-Pin Assignment.

UNIT-3: Placement & Routing:
Classification of Placement Algorithms-Simulation Based Placement Algorithms-Partitioning Based Placement Algorithms-Global Routing-Classification - Maze Routing Algorithms-Line-Probe Algorithms-Shortest Path Based Algorithms-Steiner Tree based Algorithms -Detailed Routing-classification-Single-Layer Routing Algorithms-Two-Layer Channel Routing Algorithms.

UNIT-4: Other Important Routing Algorithms and Compaction:
Over-the-cell Routing-Via Minimization-Clock Routing-Power and Ground Routing-Classification of Compaction Algorithms-One Dimensional Compaction-Two Dimensional Compaction-Hierarchical Compaction.

UNIT-5: Simulation, Logic Synthesis and Verification:
General Remarks on VLSI Simulation-Gate-level Modeling and Simulation - Switch-level Modeling and Simulation-Introduction to Combinational Logic Synthesis - Binary-decision Diagrams -Two-level Logic Synthesis.

COURSE OUTCOMES:

	Course Outcomes	POs related to COs
CO1	Understand need for VLSI physical design automation.	PO1, PO2 , PO4
CO2	Formulate partitioning, floor planning and pin assignment problems and simulate.	PO1, PO2, PO3, PO4 & PO5
CO3	Able to analyze the methods placement and routing.	PO1, PO2, PO3, PO4
CO4	Gain the in depth approaches to other important routing approaches and compaction methods.	PO1, PO2, PO3, PO4
CO5	Understand and apply simulation, synthesis and verification.	PO1, PO2, PO3, PO4

Text Books:

1.Algorithms for VLSI Design Automation, Student Edition, 1999, S.H.Gerez, John wiley & Sons (Asia) Pvt. Ltd.
2.Algorithms for VLSI Physical Design Automation, 3/e, 1999,Naveed Sherwani, Springer International Edition.

Reference Books:

1. VLSI Physical Design Automation. Theory and practice, 2/e, 1995, S. Sait, H. Youssef, McGrawHill.
2. An Introduction to VLSI Physical Design, 2/e, 1996, M. Sarrafzadeh, C. K. Wong, McGraw-Hill, New Delhi.
3. Synthesis and Optimization of Digital Circuit ,3/e, 2003, G. De Micheli, Tata McGraw Hill Edition.
4. Logic Synthesis and Verification Algorithms, 2/e, 1996, G. Hachtel, F. Somenzi, Kluwer Academic Publishers.
5.Computer Aided Logical Design with Emphasis on VLSI, 4/e, 2004, Frederick J. *Hill*, Gerald R. *Peterson*, ISBN publishers.

CO-PO Mapping

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	-	2	-	-	-	-	-	-	-	-
CO2	3	3	2	2	-	-	-	-	-	-	-	-
CO3	3	3	3	3	-	-	-	-	-	-	-	-
CO4	3	3	3	3	-	-	-	-	-	-	-	-
CO5	3	3	3	3	-	-	-	-	-	-	-	-
CO*	3	2.8	2.75	2.6	-	-	-	-	-	-	-	-

I year M.Tech II Semester

L	T	P	C
3	*0*	*0*	*3*

20MVSD25A MULTIGATE TRANSISTORS (Core Elective – III)

Course Educational Objectives:

CEO1: Understand the structure and working principles os multigate devices.
CEO2: To be able to understand the physical structure of multi-gate MOSFET technology
CEO3: To gain the 2D and 3D - dimentional aspects of mu;tigate systems.
CEO4: Apply the knowledge in designing the digital devises and SRAM memory.
CEO5: Obtain the ability to realize the analog circuit designs

UNIT-1: Structures of Multigate Devices
Principle operation of FlexFET-Independent Double Gated FlexFET – Principle operation of FinFET-Pi-gate-Tri-gate - Principle operation of Ω-gate - GAA transistor - Comparison of Multigate devices with CMOS.

UNIT-2: Multi-Gate MOSFET Technology
Quantum effects - Volume inversion-Mobility - Threshold voltage - Inter subband scattering - multigate technology-Mobility - Gate stack.

UNIT-3: Physics of the Multigate MOS Systems
MOS Electrostatics : 1D, 2D MOS Electrostatics - Modeling assumptions - Gate voltage effect - Semiconductor thickness effect - Asymmetry effect - Oxide thickness effect - Electron tunnel current.

UNIT-4: Circuit Design using Multigate Devices
Digital circuits-Impact of device performance on digital circuits - Leakage performance trade off - Multi VT devices and circuit - SRAM design.

UNIT-5: Analog Circuit Design using Multi-Gate Transistor
Introduction to Analog circuit design: design issues-Transconductance - Intrinsic transistors gain-Matching behavior - Flicker noise - Transit and maximum oscillation frequency – Self heating - Charge trapping in high K dielectric - RF circuit design.

COURSE OUTCOMES:

On successful completion of the course the student will be able to		POs related to COs
CO1	Expose to the advantages of multi-gate FETs and the challenges posed by the appearance of novel effects.	PO1
CO2	Realize the issues associated with multi-gate FET manufacturing.	PO1, PO2
CO3	Analyze the behavior of electron mobility in different multi-gate structures	PO1, PO2, PO4
CO4	Apply the principle of multi-gate device in digital circuits design.	PO1, PO2, PO3
CO5	Familiarize with the applications of multi-gate device in analog circuits for modern IC design.	PO1, PO2, PO3

REFERENCES:

1. Jean-Pierre Colinge, "FinFETs and Other Multi-GateTransistors", Springer Science & Business Media LLC, ISBN 978-0-387-71751-7, e-ISBN 978-0-387-71752-4, 2008.
2. Hiroshi Iwai, "Future of Nano CMOS technology", Solid-State Electronics, Elsevier, pp.56-67, 2015.
3. Prateek Mishra, Anish Muttreja, and Niraj K. Jha, "FinFET Circuit Design", Nanoelectronic Circuit Design, Springer Science & Business Media LLC, pp. 23-54, 2011.
4. J.P. Colinge, "Multi-gate SOI MOSFETs", Microelectronic Engineering, Elsevier, pp. 2071-2076,2007.
5. D. Lederer, "FinFET analogue characterization from DC to 110 GHz", Solid-State Electronics, Elsevier, pp. 1488–1496, 2005.

CO-PO Mapping

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	-	-	-	-	-	-	-	-	-	-	-
CO2	3	3	-	-	-	-	-	-	-	-	-	-
CO3	3	3	-	2	-	-	-	-	-	-	-	-
CO4	3	3	2	-	-	-	-	-	-	-	-	-
CO5	3	3	2	-	-	-	-	-	-	-	-	-
CO*	3	3	2	2	-	-	-	-	-	-	-	-

I M.Tech II Semester

L	T	P	C
3	*0*	*0*	*3*

20MVSD25B NANO-SCALE TRANSISTORS (CORE ELECTIVE III)

Course Educational Objectives:

CEO1: To understand the essential of MOS transistor scaling
CEO2: To introduce the nano scale MOS transistor concept and performance to study and Analyze the different nano scaled MOS transistors
CEO3: To evaluate the i-v characteristics for non degenerate carrier statistics
CEO4: To analyze the radiation effects in multigate devices
CEO5: To analyze impact of multi gate device performance on digital circuits

UNIT - 1: INTRODUCTION TO NOVEL MOSFETS

MOSFET scaling, short channel effects-channel engineering - source/drain engineering – high k dielectric - copper interconnects - strain engineering, SOI MOSFET, multi gate transistors – single gate– double gate – triple gate – surround gate, quantum effects – volume inversion – mobility – threshold voltage – inter sub band scattering, multi gate technology – mobility – gate stack

UNIT 2 : PHYSICS OF MULTIGATE MOS SYSTEM

MOS Electrostatics – 1D – 2D MOS Electrostatics, MOSFET Current-Voltage Characteristics – CMOS Technology – Ultimate limits, double gate MOS system – gate voltage effect – semiconductor thickness effect – asymmetry effect – oxide thickness effect – electron tunnel current – two dimensional confinement, scattering – mobility.

UNIT 3: NANOWIRE FETS AND TRANSISTORS AT THE MOLECULAR SCALE

Silicon nano wire MOSFETs – Evaluation of I-V characteristics – The I-V characteristics for non degenerate carrier statistics – The I-V characteristics for degenerate carrier statistics – Carbon nano tubes – Carbon nano tube FETs – Electronic conduction in molecules – General model for ballistic nano transistors – MOSFETs with 0D, 1D, and 2D channels – Molecular transistors

UNIT 4: RADIATION EFFECTS

Radiation effects in SOI MOSFETs, total ionizing dose effects – single gate SOI – multigate devices, single event effect, scaling effects

UNIT 5: CIRCUIT DESIGN USING MULTIGATE DEVICES

Digital circuits – impact of device performance on digital circuits – leakage performance trade off – multi VT devices and circuits – SRAM design, analog circuit design – Trans conductance – intrinsic gain
– flicker noise – self heating –band gap voltage reference – operational amplifier – comparator designs, mixed signal – successive approximation DAC, RF circuits

COURSE OUTCOMES:

On successful completion of the course the student will be able to,		POs related to COs
CO1	Explain about the various novel MOSFETs to tackle short channel effects	PO1, PO2
CO2	Apply the physics of multi gate MOS system	PO1, PO2
CO3	Identify the performance of Nano wire FETs and transistors at the molecular scale	PO1, PO2
CO4	Understand about the radiation effects in SOI MOSFETs	PO1, PO2, PO4
CO5	Explain about the concept of circuit design using multi gate devices	PO1, PO4,.

Text Books

1. J P Colinge, FINFETs and other multi-gate transistors, Springer – Series on integrated circuitsand systems, 2008.
2. Mark Lundstrom Jing Guo, Nanoscale Transistors: Device Physics, Modeling and Simulation,Springer,2006.

Reference Books

1. M S Lundstorm, Fundamentals of Carrier Transport, 2nd Ed., Cambridge University Press, Cambridge UK, 2000.

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	-	-	-	-	-	-	-	-	-	-
CO2	3	3	-	-	-	-	-	-	-	-	-	-
CO3	3	2	-	-	-	-	-	-	-	-	-	-
CO4	3	3	-	2	-	-	-	-	-	-	-	-
CO5	3	-	-	2	-	-	-	-	-	-	-	-
CO *	**3**	**2.5**	**-**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**

I YEAR M.Tech II Semester

L	T	P	C
3	*0*	*0*	*3*

20MVSD25C MICROELECTRONICS (Core Elective – III)

Course Educational Objectives:

CEO1: Be familiar with the MOSFET physical structure and operation, terminal characteristics, Circuit models and basic circuit applications.
CEO2: Provide knowledge on small signal analysis of MOSFET amplifier along with its internal Characteristics.
CEO3: Analyze and design microelectronic circuits for single stage linear amplifier and digital Applications.
CEO4: Understand the concepts of high frequency response of MOSFET transistor.
CEO5: Analyze the characteristics of differential and multi-stage amplifiers

UNIT – 1: MOSFETS: Device Structure and Physical Operation, V-I Characteristics, MOSFET Circuits at DC, MOSFET as an amplifier and as a switch.

UNIT – 2: MOSFETS (continued): Biasing in MOS amplifier Circuits, Small Signal Operation and Models, Basic MOSFET amplifier, MOSFET internal capacitances, frequency response of CS amplifier.

UNIT – 3: Single Stage IC Amplifier: Discrete circuit MOS amplifiers: Comparison of MOSFET and BJT, Current sources, Current mirrors and current steering circuits, high frequency response- general considerations.

UNIT – 4: Single Stage IC Amplifier (continued): CS with active loads, high frequency response of CS, CG amplifiers with active loads, high frequency response of CG, Cascode amplifiers. CS with source degeneration.

UNIT – 5: Differential and Multistage Amplifiers: The MOS differential pair, small signal operation of MOS differential pair, Differential amplifier with active loads, and frequency response of the differential amplifiers. Multistage amplifiers.

COURSE OUTCOMES:

On successful completion of the course the student will be able to,		**POs related to COs**
CO1	Explain the underlying physics and principles of operation of Metal oxide-semiconductor (MOS) capacitors and MOS field effect transistors (MOSFETs).	PO1,PO2
CO2	Describe and apply simple large signal circuit models for MOSFETs.	PO1,PO2,PO3
CO3	Analyze and design microelectronic circuits for linear amplifier for Digital applications.	PO1,PO2,PO3
CO4	Use of discrete MOS circuits to design Single stage and Multistage Amplifiers to meet stated operating specifications.	PO1,PO2
CO5	Demonstrate the characteristics of differential and multi-stage amplifiers	PO1,PO2

Text Book:

1. "Microelectronic Circuits", Adel Sedra and K.C. Smith, 6th Edition, Oxford University Press, International Version, 2009.

Reference Books:

1. Microelectronics An integrated approach", Roger T Howe, Charles G Sodini, Pearson education.
2. Fundamentals of Microelectronics", Behzad Razavi, John Wiley India Pvt. Ltd, 2008.
3. Microelectronics – Analysis and Design", Sundaram Natarajan, Tata McGraw-Hill, 2007.
4. Microelectronic Devices and Circuits -Clifton G. Fonstad - McGraw-Hill
5. Microelectronics Circuit Analysis and Design - Donald Neamen - 4th Edition - McGraw-Hill Education

6. CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	-	-	-	-	-	-	-	-	-	-
CO2	3	2	2	-	-	-	-	-	-	-	-	-
CO3	2	3	1	-	-	-	-	-	-	-	-	-
CO4	2	2	-	-	-	-	-	-	-	-	-	-
CO5	1	2	-	-	-	-	-	-	-	-	-	-
CO *	2.2	2.2	1.5	-	-	-	-	-	-	-	-	-

I year M.Tech II Semester

L	T	P	C
3	*0*	*0*	*3*

20MVSD25D MODELING AND SIMULATION (Core Elective III)

Course Educational Objectives:

CEO1: To provide knowledge on Fundamentals of simulation software.

CEO2: To acquire knowledge and skills on simulation models and systems.

CEO3: To be able to understand and analyze the state machines.

CEO4: To be able to use the Event driven models.

CEO5: To perform the system optimization.

UNIT - 1: Basic Concepts & Simulation Software

Basic Simulation Modeling - Systems - Models and Simulation - Discrete Event Simulation - Simulation of Single Server Queuing System - Simulation of Inventory System - Alternative approach to Modeling and Simulation. Comparison of Simulation Packages with Programming Languages - Classification of Software - Desirable Software Features - General Purpose Simulation Packages – Arena - Extend and Others - Object Oriented Simulation - Examples of Application Oriented Simulation Packages.

UNIT - 2: Simulation Models & Time Driven Systems

Guidelines for Determining Levels of Model Detail - Techniques for Increasing Model Validity and Credibility. Modeling Input Signals - Delays - System Integration - Linear Systems - Motion Control Models - Numerical Experimentation.

UNIT - 3: Exogenous Signals And Events

Disturbance Signals - State Machines - Petri Nets & Analysis - System Encapsulation.

UNIT - 4: Markov Process & Event Driven Models

Probabilistic Systems - Discrete Time Markov Processes - Random Walks - Poisson Processes - the Exponential Distribution - Simulating a Poison Process - Continuous -Time Markov Processes. Simulation Diagrams - Queuing Theory - Simulating Queuing Systems - Types of Queues - Multiple Servers.

UNIT - 5: System Optimization

System Identification - Searches - Alpha/Beta Trackers - Multidimensional Optimization - Modeling and Simulation Mythology.

COURSE OUTCOMES:

On successful completion of the course the student will be able to		POs related to COs
CO1	Understand basic simulation models, characterizing and simulation diagrams.	PO1, PO2
CO2	Model time driven systems and stochastic processes.	PO1, PO2, PO4
CO3	Know how to simulate Exogenous signals.	PO1, PO2, PO4
CO4	Build simulation models with programming languages.	PO1, PO2, PO3, PO4
CO5	Discuss system optimization methodologies.	PO1, PO2, PO4

Text books:

1. System Modeling & Simulation, an Introduction, 2/e, 2011, Frank L. Severance, John Wiley & Sons, New -Yark, USA.

Refrence books:

1. Systems Simulation, 1/e, 1978, Geoffery Gordon, Prentice Hall of India, New Delhi.
2. Simulation Modeling and Analysis, 3/e, 2000, McGraw -Hill, Law, A.M. and W.D. Kelton, New York, NY.
3. Discrete Event Simulation: A Practical Approach, 1/e, 1992, Pooch, U.W and J.A. Wall, CRC Press, Boca Raton, FL.
4. Handbook of Simulation: Principles, Methodology, Advances, Applications, and Practice, 1/e, 1998, Banks, J., Ed., John Wiley & Sons, New York.
5. Monte Carlo: Concepts, Algorithms and Applications, 2/e, 1996, Fishman, G.S., Springer -Verlag, New York, NY.

CO-PO Mapping

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	-	-	-	-	-	-	-	-	-	-
CO2	3	3	-	3	-	-	-	-	-	-	-	-
CO3	3	2	-	2	-	-	-	-	-	-	-	-
CO4	3	3	3	2	-	-	-	-	-	-	-	-
CO5	3	3	-	3	-	-	-	-	-	-	-	-
CO*	3	2.8	3	2.5	-	-	-	-	-	-	-	-

I Year M.Tech II Semester

L	T	P	C
3	*0*	*0*	*3*

20MVSD26A MEMORY DESIGN (Core Elective – IV)

Course Educational Objectives:

CEO1: To provide knowledge on
- Different types of memories
- Different packing techniques of memories.

CEO2: To analyze Non-volatile Memories.

CEO3: To Analyze different parameters that leads malfunctioning of memories.

CEO4: Analyze different Radiation techniques.

CEO5: Design reliable memories with efficient architecture to improve processes times and power

UNIT - 1: Random Access Memory Technologies Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar, SRAM Technologies-Silicon On Insulator (SOl) Technology-Advanced SRAM Architectures and Technologies- Application Specific SRAMs. Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Structures- BiCMOS DRAMs Advanced DRAM Designs and Architecture-Application Specific DRAMs.

UNIT - 2: Non-Volatile Memories-Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)- Bipolar PROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating- Gate EPROM Cell-One-Time Programmable (OTP) Eproms-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

UNIT - 3: Memory Fault Modeling, Testing, And Memory Design For Testability And Fault Tolerance-RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

UNIT - 4: Semiconductor Memory Reliability And Radiation Effects-General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification. Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques, Process and Design Issues.

UNIT - 5: Advanced Memory Technologies And High-Density Memory Packaging Technologies-Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories-Magneto resistive Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.

COURSE OUTCOMES:

On successful completion of the course the student will be able to,		**POs related to Cos**
CO1	Identify different types of memories and different packing techniques of memory transistor.	PO1, PO2 ,PO3, PO5
CO2	Demonstrate knowledge on **Non-volatile Memories.**	PO1, PO2
CO3	Identify different parameters that leads malfunctioning of memories.	PO1, PO2, PO3, PO5
CO4	Analyze the effect of different Radiation techniques.	PO1, PO2, PO4
CO5	Understand and use the concept of reliable memories with efficient architecture to improve processes times and power.	PO1, PO4,.

TEXT BOOKS:

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma- 2002, Wiley.

REFERENCE BOOKS:

1. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1st Ed., Prentice all.

CO-PO Mapping

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	-	-	-	-	-	-	-	-	-	-
CO2	2	3	2	-	-	-	-	-	-	-	-	-
CO3	2	2	2	-	-	-	-	-	-	-	-	-
CO4	2	3		-	-	-	-	-	-	-	-	-
CO5	3	1	-	-	-	-	-	-	-	-	-	-
CO*	2.4	2.2	2	-	-	-	-	-	-	-	-	-

I M.Tech II Semester

L	T	P	C
3	*0*	*0*	*3*

20MVSD26B ADVANCED COMPUTER ARCHITECTURE (Core Elective - IV)

Course Educational Objectives:

CEO1: To understand the basics of fundamental computer units

CEO2: To gain the knowledge on parallel computers and instruction level parallelism

CEO3: To acquire knowledge memory concepts, functional principles and design of Memory hierarchy.

CEO4: To obtain the concepts of multiprocessors.

CEO5: To be able to define the advanced proessors and functionality.

UNIT 1: FUNDAMENTALS OF COMPUTER DESIGN

Introduction, The task of a Computer Designer, Technology and Computer Usage Trends, Cost ad Trends in Cost, Measuring and reporting performance, Quantitative principles of computer design, Control Units: Hardwired And Micro Programmed Design Concept, Microprogramming, Bus architectures: Uni-bus and multi-bus architectures.

UNIT 2: PARALLEL COMPUTER MODELS & INSTRUCTION LEVEL PARALLELISM

The state of computing, Classification of parallel computers, Multiprocessors and multicomputers, Multivector and SIMD computers, Instruction Level Parallelism, Overcoming Data Hazards with Dynamic Scheduling, Reducing Branch Penalties with Dynamic , HardwareSupport for Extracting More Parallelism.

UNIT 3: MEMORY HIERARCHY DESIGN

Introduction, The Fundamentals of Caches, Reducing Cache Misses, Reducing Cache Miss Penalty, Reducing Hit Time, Main Memory, Virtual Memory, Issues in the Design of Memory Hierarchy.

UNIT 4: MULTIPROCESSORS

Introduction, Characteristics of Application Domains, Centralized Shared Memory Architectures, Distributed Shared Memory Architectures, Synchronization, Models of Memory Consistency, Crosscutting Issues.

UNIT 5: ADVANCED PROCESSORS

Advanced processor technology, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Vector and Symbolic processors

COURSE OUTCOMES:

On Successful completion of this course the students will be able to		POs related to Cos
CO1	Able to know the functional units, classification and differences between uni bus and multi bus systems.	PO1, PO2
CO2	Demonstrate and the classification of parallel computers.Analyze the complex issues related to data hazard and branch penalities.	PO1, PO2,PO4
CO3	Classification of memory, identify cacne and memeory related issues in multipricessors and design of memeory hierarchy.	PO1, PO2,PO3
CO4	Demonstrate the multiprocessors architecture and its classifications.	PO1, PO2
CO5	Acquire knowledge on advanced prcessors and differences between RISC and CISC.	PO1,PO2

TEXT BOOKS:

1. Kai Hwang, "Advanced computer architecture", TMH.2000.
2. J.P.Hayes, "computer Architecture and organization", MGH.1998.

REFERENCE BOOKS:

1. D. A. Patterson and J. L. Hennessey, "Computer organization and design," Morgan Kaufmann, 2nd Ed.
2. Harvey G.Cragon,"Memory System and Pipelined processors"; Narosa Publication.
3. R.K.Ghose, RajanMoona&Phalguni Gupta, "Foundation of Parallel Processing"; Narosa Publications.

CO-PO Mapping

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	-	-	-	-	-	-	-	-	-	-
CO2	3	2	-	2	-	-	-	-	-	-	-	-
CO3	2	3	2	-	-	-	-	-	-	-	-	-
CO4	3	2	-	-	-	-	-	-	-	-	-	-
CO5	3	2	-	-	-	-	-	-	-	-	-	-
CO*	3	2.2	2	2	-	-	-	-	-	-	-	-

I Year M.Tech II sem.

L	T	P	C
3	0	0	3

20MVSD26C Fault Tolerant Design (Core Elective-IV)

Course Educational Objectives:

CEO1: To provide knowledge on Fundamentals of reliability.
CEO2: To acquire knowledge and skills on software approaches for reliability.
CEO3: To be able to understand the reliability modeling.
CEO4: To understand the fault tolerant architectures.
CEO5: To understand the need for synchronization.

UNIT - 1: INTRODUCTION TO RELIABILITY

Reliability — Repairable and Non Repairable systems — Maintainability and Availability — Designing for higher reliability — Redundancy — MTBF — MTTF MDT - MTTR— k out of in systems.

UNIT - 2: SOFTWARE RELIABLITY AND APPROACHES

Software reliability - Software reliability Vs Hardware reliability – Failures and Faults - Classification of Failures – Counting – System Configuration – Components and Operational Models – Concurrent Systems – Sequential Systems – Standby Redundant systems Fault Avoidance — Passive Fault detection — Active Fault Detection — Fault Tolerance - Fault Recovery - Fault Treatment.

UNIT - 3: RELIABILITY MODELING

Introduction to Software Reliability Modeling – Parameter Determination and Estimation - Model Selection – Markovian Models – Finite and Infinite failure category Models – Comparison of Models – Calendar Time Modeling.

UNIT - 4: FAULT TOLERANT ARCHITECTURE

Fault tolerant computers - general purpose commercial systems-fault tolerant multiprocessor and VLSI based communication architecture. Design-N-version programming recovery block - acceptance tests-fault trees- validation of fault tolerant systems.

UNIT - 5: FAULT DETECTION AND SYNCHRONIZATION

Fault types – Fault detection and containment – Redundancy – Data diversity – Reversal checks – Obtaining parameter values – Reliability models for hardware redundancy – Software error models – Clocks – Fault tolerant synchronization – Synchronization in software.

COURSE OUTCOMES:

On successful completion of the course the student will be able to		POs related to COs
CO1	Understand the reliability terminologies.	PO1, PO2
CO2	Understand the software reliability approaches.	PO1, PO2
CO3	Able to analyze and utilize the modeling for reliability	PO1, PO2
CO4	Understand and analyze the FT architectures.	PO1, PO2, PO3
CO5	Gain knowledge on synchronization.	PO1, PO2

Text Book:

1. John D. Musa, " Software Reliability", McGraHill, 1985.
2. Patric D. T.O connor," Practical Reliability Engineering" , 4th Edition, John Wesley & sons , 2003.

Reference Books:

1. Israel Koren and C. Mani Krishna; Fault-Tolerant Systems; Morgan-Kaufman Publishers, 2007.
2. Elena Dubrova; Fault-Tolerant Design; Springer, 2013.
3. Michael R. Lyu; Handbook of Software Reliability Engineering; IEEE Computer Society Press (and McGraw-Hill), 1996.
4. Martin L. Shooman; Reliability of Computer Systems and Networks: Fault Tolerance, Analysis, and Design; John Wiley & Sons Inc., 2002.
5. Kishor S. Trivedi; Probability and Statistics with Reliability, Queuing and Computer Science Applications; John Wiley & Sons Inc., 2016.

6. CO-PO Mapping

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	-	-	-	-	-	-	-	-	-	-
CO2	3	2	-	-	-	-	-	-	-	-	-	-
CO3	3	3	-	-	-	-	-	-	-	-	-	-
CO4	3	3	2	-	-	-	-	-	-	-	-	-
CO5	3	2	-	-	-	-	-	-	-	-	-	-
CO*	3	2.4	2	-	-	-	-	-	-	-	-	-

I Year M.Tech II sem.

L	T	P	C
3	0	0	3

20MVSD26D Microsensors and interfacing (Core elective-IV)

Course Educational Objectives:

CEO1: To provide knowledge on Fundamentals of Micro Sensors and MEMS.
CEO2: To acquire knowledge on MEMS materials & Fabrication methods
CEO3: To be able to understand micromachining process and sensors
CEO4: To be able to understand Interface Electronics for MEMS and its technology
CEO5: To understand the need for MEMS technology and its applications.

UNIT - 1: INTRODUCTION -MEMS

An Introduction to Micro Sensors and MEMS, Evolution of Micro Sensors and MEMS, Micro Sensors and MEMS Applications, Market Survey Introduction to MOEMS.

UNIT - 2: MEMS MATERIALS & FABRICATION TECHNIQUES

MEMS Materials Properties, Microelectronic Technology for MEMS, Micromachining Process, Etch Stop Techniques and Microstructure, Surface and Quartz Micromachining, fabrication of Micromachined Microstructure, Microstereolithography.

UNIT - 3: MICROMACHINING PROCESS AND SENSORS

Microelectronic Technologies For MEMS, Micromachining Technology, Surface, Bulk Micromachining, Other Micromachining Techniques, New Materials From MEMS ; Micro Machined Micro Sensors: Mechanical, Inertial, Biological, Chemical And Acoustic. MEMS Capacitive Accelerometer, MEMS Gyro Sensor

UNIT - 4: MEMS OPERATING PRINCIPLES

Mechanics, Dynamics, Electrostatics, Advanced MEMS Operating, Principles For Sensing And Actuation Including Piezoresistive, Piezoelectric, Thermo-Mechanical, Microfluidics: Flow, Heat And Mass, Transfer At Small Scales; Electro kinetics.

UNIT - 5: MEMS TECHNOLOGY AND APPLICATIONS

Wafer Bonding, Chemical Mechanical Polishing ,Bonding & IC Packaging Of MEMS, Micro Scaling Considerations, Applications In Automotive Industry, Mechanical, Optical, Biomedical & Chemical Transducers, Optical MEMS, Bio MEMS, Plastic MEMS. MEMS for Space Application,MEMS Accelerometers for Avionics

COURSE OUTCOMES:

On successful completion of the course the student will be able to		POs related to COs
CO1	Demonstrate knowledge on Micro Sensors &analyse MEMS and MOEMS	PO1, PO2
CO2	Understand, analyze MEMS material properties and utilize Techniques for fabrication	PO1, PO2, PO5
CO3	Analyze and understand the concepts of Micromachining Technology and different sensors	PO1, PO2
CO4	Understand and analyze the Mechanics, Dynamics and Electrostatics of MEMS	PO1, PO2, PO3, PO4

CO5	Demonstrate knowledge on MEMS technology and analyze its applications.	PO1, PO2

Text Book:

1. Maluf N., "An Introduction to Micro electromechanical Systems Engineering", Norwood, MA: Artech House, 2000.
2. Julian W. Gardner, "Micro sensors - Principles and Applications", John Wiley & Sons, Inc.1997.

Reference Books:

1. Stephen D. Senturia, "Microsystem Design", Kluwer Academic Publishers, 1st Ed., 2001.
2. Marc Madou, "Fundamentals of Microfabrication" , CRC Press, 1st Ed., 1997.
3. Gregory Kovacs, "Micromachined Transducers Sourcebook", WCB McGraw-Hill, Boston, 1 st Ed., 1998.
4. M. H. Bao, "Micromechanical Transducers: Pressure sensors, accelerometers, and gyroscopes" by Elsevier, New York, 1st Ed., 2000.
5. Ljubisa Ristic, "Sensor Technology and Devices", Artech House, 1994

CO-PO Mapping

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	-	-	-	-	-	-	-	-	-	-
CO2	3	3	-	-	2	-	-	-	-	-	-	-
CO3	3	3	-	-	-	-	-	-	-	-	-	-
CO4	3	3	2	2	-	-	-	-	-	-	-	-
CO5	3	3	-	-	-	-	-	-	-	-	-	-
CO*	3	3	2	2	2	-	-	-	-	-	-	-

I year M.Tech I Semester **L T P C**

0 0 3 2

20MVSD27 ASIC DESIGN LAB (CAD Tool)

Course Educational Objectives:

CE01: To develop the knowledge on different arithmetic design like Adder and Subtractor
CE02: To Design the different skills on different circuits
CE03: To provide a design knowledge and analysis of different counters
CE04: Understand the signed pipelined multiplier configurations
CE05: To design and develop an using layout design and LVS.

List of Experiments

1. Adder/ Subtractor
2. Multiplexer/ Demultiplexer
3. 8-bit Counter
4. Signed Pipelined Multiplier
5. Accumulator
6. MAC
7. Memory
8. Using Layout Design of any one of the above seven
9. Using LVS Tape out Preparation

The above experiments are carried out using the following tools:

1. Model SIM
2. Cadence
3. Synopsis
4. Mentor Graphics
5. Xilinx Plan ahead

Course Outcomes:

On successful of the courses the student will be able to		POs related to Cos
CO1	Demonstrate knowledge on using Arithmetic and Logical circuits	PO1
CO2	Analyze the simulated results in different combinational circuits	PO2
CO3	Design and develop the different counters based on circuits	PO3
CO4	Investigate and test the circuits for produces required outputs	PO4
CO5	Select appropriate design tools to test the different cicuits for different values	PO5
CO6	Follow the ethical values in designing the circuits	PO8
CO7	Do experiments effectively as an individual and as a member in a group	PO9
CO8	Communicate verbally and in written form, the understandings about the experiments	PO10
C09	Continue updating their design skill related to for various circuits on different applications during their life time	PO12

CO-PO MAPPING

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	-	-	-	-	-	-	-	-	-	-	-
CO2	-	3	-	-	-	-	-	-	-	-	-	-
CO3	-	-	3	-	-	-	-	-	-	-	-	-
CO4	-	-	-	3	-	-	-	-	-	-	-	-
CO5	-	-	-	-	3	-	-	-	-	-	-	-
CO6	-	-	-	-	-	-	-	3	-	-	-	-
CO7	-	-	-	-	-	-	-	-	3	-	-	-
CO8	-	-	-	-	-	-	-	-	-	3	-	-
CO9	-	-	-	-	-	-	-	-	-	-	-	3
CO*	3	3	3	3	3	-	-	3	3	3	-	3

I M.Tech I Semester

L	T	P	C
0	*0*	*3*	*2*

20MVSD28 SCRIPTING LANGUAGE LAB

Course Educational Objectives:

CEO1: Understand the principles of creating an effective web page, including an in-depth consideration of information architecture.
CEO2: Use JavaScript to access and use web services for dynamic content
CEO3: understand how to develop and implement various types of programs in the Perl language
CEO4: understand the appropriate applications of the Perl language
CEO5: Recognize similarities and common characteristics of programming languages.

List of Experiments

1. Write an HTML document that contains a VB script that will retrieve quantity and unit price from a webpage. When "Calculate Cost" button is pressed, it calculates & displays total amount for the order.
2. Develop and demonstrate a XHTML file that includes Javascript script for the following problems:
   a) Input: A number n obtained using prompt
      Output: The first n Fibonacci numbers
   b) Input: A number n obtained using prompt
3. Output: A table of numbers from 1 to n and their squares using alert
4. Write a Perl script that prints your name and your area of interest in VLSI Domain and run the script.
5. Develop a perl program to demonstrate the pattern matching features of perl.
6. Write a perl script to compute the n^{th} power of a given number.
7. Develop a Perl Program to find the given number is prime, even and odd.
8. Develop a perl program to demonstrate the usage of Signals.
9. Develop a perl program to demonstrate the usage of Files.
10. Develop a perl program to demonstrate the usage of Pipes.
11. Write a Perl program to insert name and age information entered by the user into a table created using MySQL and to display the current contents of this table.

Tools Required:

1. UNIX OS.
2. Windows OS and PERL software.

COURSE OUTCOMES:

On successful completion of the course the student will be able to,		POs related to COs
CO1	Use Javascript and XHTML to create web pages with advanced interactivity	PO1
CO2	Illustrate the process of system administration using suitable script.	PO2
CO3	Develop and demonstrate the usage of Signals and Files in the Perl	PO3
CO4	Acquire the skills for expressing syntax and semantics in formal notation	PO4
CO5	Follow ethical principles in syntax and semantics of the Perl language	PO8
CO6	Do experiments effectively as an individual and as a member in a group.	PO9
CO7	Communicate verbally and in written form, the understandings about the experiments.	PO10
CO8	Continue updating their skill and apply during their life time.	PO12

CO-PO MAPPING

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	-	-	-	-	-	-	-	-	-	-	-
CO2	-	3	-	-	-	-	-	-	-	-	-	-
CO3	-	-	3	-	-	-	-	-	-	-	-	-
CO4	-	-	-	3	-	-	-	-	-	-	-	-
CO5	-	-	-	-	3	-	-	-	-	-	-	-
CO6	-	-	-	-	-	-	-	3	-	-	-	-
CO7	-	-	-	-	-	-	-	-	3	-	-	-
CO8	-	-	-	-	-	-	-	-	-	3	-	-
CO9	-	-	-	-	-	-	-	-	-	-	-	3
CO*	3	3	3	3	3	-	-	3	3	3	-	3

II M. Tech I– Semester

20MVSD31 PROJECT WORK PHASE – I

L	T	P	C
-	-	-	10

20MVSD41 PROJECT WORK PHASE – II

L	T	P	C
-	-	-	14

Course Educational Objectives:

CEO1: To develop the ability to undertake problem identification, formulation and solution.
CEO2: To demonstrate the ability to engage in design and to execute to an appropriate professional standard.
CEO3: To develop the capacity to undertake lifelong learning.
CEO4: To develop the ability to communicate effectively, not only with engineers but also with the community at large.
CEO5: To develop an understanding of the social, cultural, global and environmental responsibilities of the professional Engineer, and the principles of sustainable design and development

PROJECT WORK:

The aim of the project work is to deepen comprehension of principles by applying them to a new problem which may be the design / fabrication / analysis for a specific application, a research project with a focus on an application needed by the industry / society, a computer project, a management project or a design and analysis project. A project topic must be selected by the students in consultation with their guides. To train the students in preparing project reports and to face reviews and viva voce examination. The internal evaluation shall be done by the committee, consisting of HOD/HOD's nominee, coordinator and project supervisor on the basis of two seminars to be givenby each student on the topi of hi/ her project. The evaluation of the proect work will be conducted at the endof the II-II s emester.

Course Outcomes:

On successful completion of this course, the students should be able to		POs related to COs
CO1	Demonstrate in-depth knowledge on the project topic	PO1
CO2	Identify, analyze and formulate complex problem chosen for project work to attain substantiated conclusions.	PO2
CO3	Design solutions to the chosen project problem.	PO3
CO4	Undertake investigation of project problem to provide valid conclusions.	PO4
CO5	Use the appropriate techniques, resources and modern engineering tools necessary for project work.	PO5
CO6	Apply project results for sustainable development of the society	PO6
CO7	Understand the impact of project results in the context of environmental sustainability	PO7
CO8	Understand professional and ethical responsibilities while executing the project work.	PO8
CO9	Function effectively as individual and a member in the project team.	PO9
CO10	Develop communication skills, both oral 3and written for preparing and presenting project report.	PO10
CO11	Demonstrate knowledge and understanding of cost and time analysis required for carrying out the project.	PO11
CO12	Engage in lifelong learning to improve knowledge and competence in the chosen area of the project.	PO12

CO-PO Mapping

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	-	-	-	-	-	-	-	-	-	-	-
CO2	-	**3**	-	-	-	-	-	-	-	-	-	-
CO3	-	-	**3**	-	-	-	-	-	-	-	-	-
CO4	-	-	-	**3**	-	-	-	-	-	-	-	-
CO5	-	-	-	-	**3**	-	-	-	-	-	-	-
CO6	-	-	-	-	-	**3**	-	-	-	-	-	-
CO7	-	-	-	-	-	-	**3**	-	-	-	-	-
CO8	-	-	-	-	-	-		**3**	-	-	-	-
CO9	-	-	-	-	-	-	-	-	**3**	-	-	-
CO10	-	-	-	-	-	-	-	-	-	**3**	-	-
C011	-	-	-	-	-	-	-	-	-	-	**3**	-
CO12	-	-	-	-	-	-	-	-	-	-	-	**3**