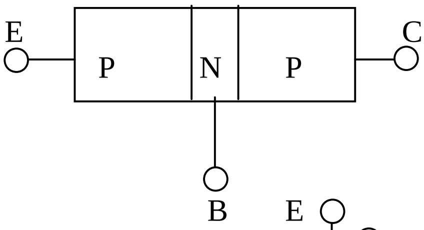
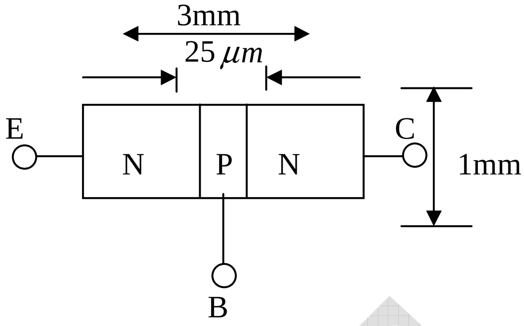
DEPARTMENT OF ECE

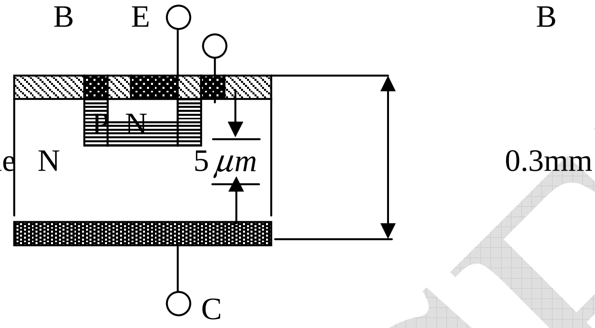
## UNIT-V&VI

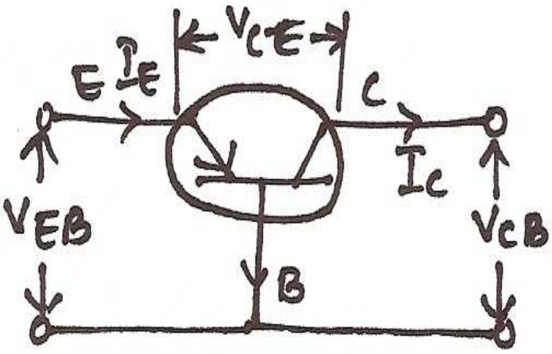
Construction: -

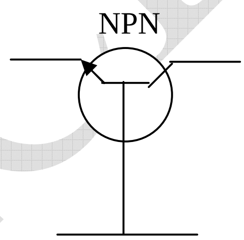



Silicon diode

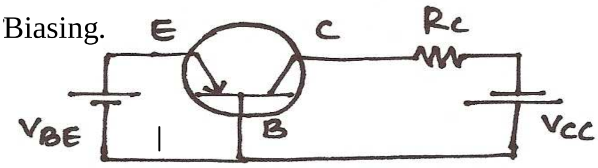


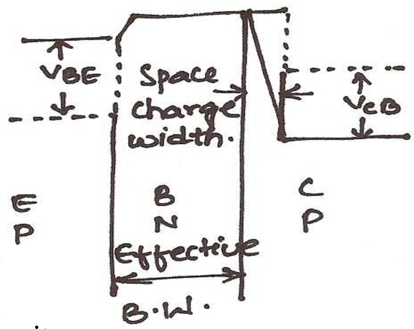




Potential barrier at the
junctions of unbiased transistor.

Biasing.




Currents in a Transistor.

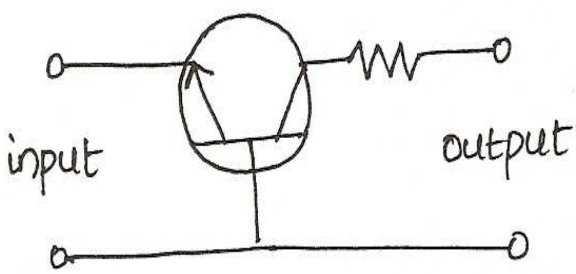
$I_E = I_C + I_B$ and $I_C \approx I_E$

$I_{CEO}$ = Collector current when base is open circuit
(Reverse saturation current of B – C junction) µA

$I_{CEO} = (\beta+1) I_{CBO}$ = Collector current when Emitter is open circuited
(very less current due to junction barriers) µA.

$I_{EO}$ = Emitter base reverse (biased) saturation current when collector is open circuited.

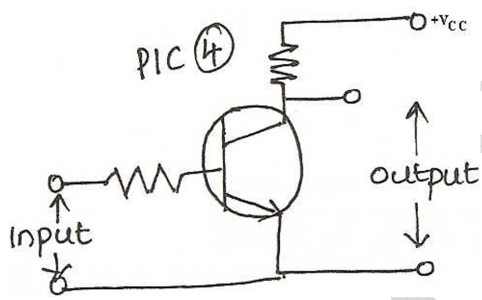
**COMMON BASE CONFIGURATION: -**




Current gain(∝) = Collector current / emitter current = $\frac{\Delta I_C}{\Delta I_E}$

∝ Varies from 0.9 to 0.95.

**COMMON EMITTER CONFIGURATION:**

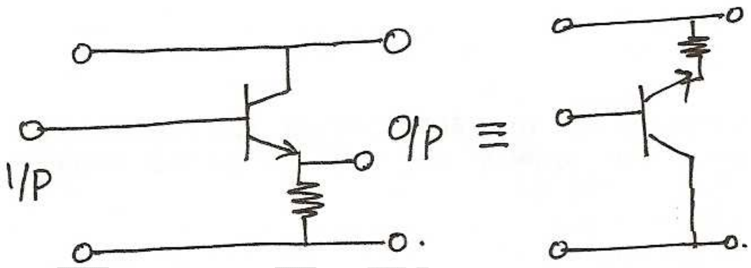



Current gain

$$(\beta) = \frac{Collector\ Current}{Base\ Current} = \frac{\Delta I_C}{\Delta I_B}$$

$\beta$ varies from 10 to 200 or 80.

**COMMON COLLECTOR CONFIGURATION: -**




**Input** **Output**

Used for impedance matching

$\gamma$ = CC Current gain

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

Similarly we can get ii) $\beta = \frac{Ic - I_{CBO}}{I_B}$ iii) $I_C = \beta I_B + I_{CEO}$

iv) $I_{CEO} = (1+\beta) I_{CBO}$ v) $I_E = \frac{1}{1-\alpha} \cdot I_{CBO} + \frac{1}{1-\alpha} \cdot I_B$

**RELATION BETWEENα, β & ϒ**

a) We know $\Delta I_E = \Delta I_C + \Delta I_B$, But $\Delta I_C = \alpha I_E$.

∴ $\Delta I_E = \alpha$ & $\Delta I_E + I_B$

$\Delta I_E - \alpha I_E = \Delta I_B$ or $\Delta I_B = \Delta I_E (1 - \alpha)$

Dividing both sides by $\Delta I_c$, $\frac{\Delta I_B}{\Delta I_C} = \frac{\Delta I_E}{\Delta I_C}(1 - \alpha)$

Or $\quad \frac{1}{\beta} = \frac{1}{\alpha}(1-\alpha) \; or \; \beta = \frac{\alpha}{1-\alpha}$

(b) $\quad \frac{\Delta I_E}{\Delta I_B} = \frac{\Delta I_C}{\Delta I_B} + \frac{\Delta I_B}{\Delta I_B}$ OR $\frac{\Delta I_E}{\Delta I_B} = \beta + 1$

Or $\quad \frac{\Delta I_E}{\Delta I_C} \times \frac{\Delta I_C}{\Delta I_B} = \beta + 1$ OR $\frac{\Delta I_E}{\Delta I_C} \times \frac{\Delta I_C}{\Delta I_B} = \beta + 1$

Or $\quad \frac{1}{\alpha}.\beta = 1 + \beta$ or $\alpha = \frac{\beta}{1+\beta}$

(c) $\quad \gamma = \frac{\Delta I_E}{\Delta I_B}$, Substituting $\Delta I_B = \Delta I_E - \Delta I_C$.

$\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C},$ by diving N & 0 on R.H.S, by $\Delta I_E$.

$\gamma = \frac{\Delta I_E / \Delta I_E}{\Delta I_E / \Delta I_E - \Delta I_C / \Delta I_E} = \frac{1}{1-\alpha}$

Putting the value of $\alpha = \beta / \beta + 1$.

$\gamma = \frac{1}{1 - \beta / \beta + 1}$

$(or)\gamma = \frac{1}{\frac{\beta + 1 - \beta}{\beta + 1}} = \frac{\beta + 1}{1} = \beta + 1$

$(or)\gamma = \frac{1}{1-\alpha} = \beta + 1$

**INPUT & OUTPUT CHARACTERISTICS OF CB CONFIGURATION.**

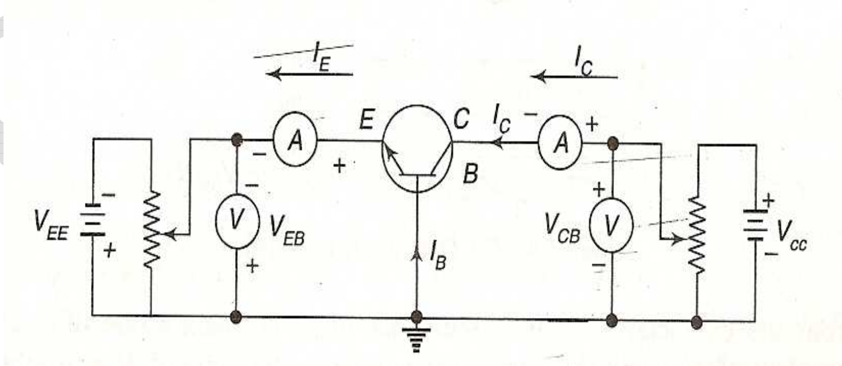
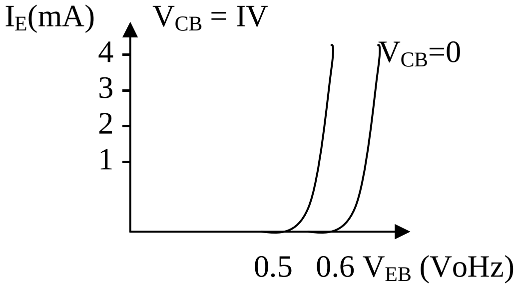
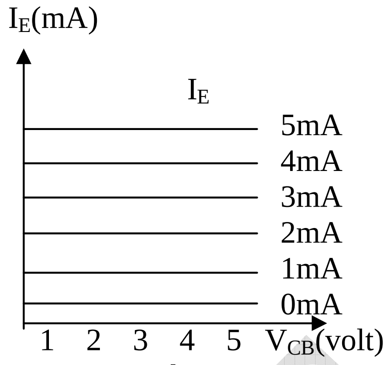



Fig. 4.7 Circuit to Determine CB Static Characteristics.




Input characteristics.




O/P Characteristics.

## CE CONFIGURATION

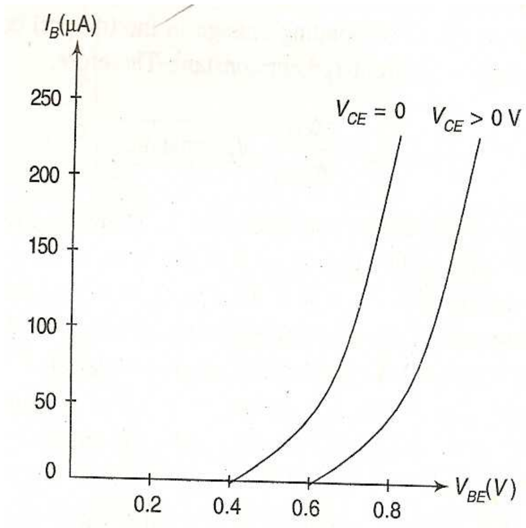



Fig. 4.11 CE Input Characteristics

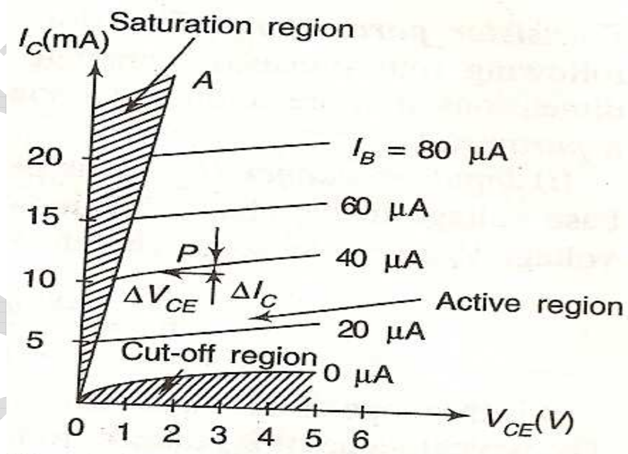
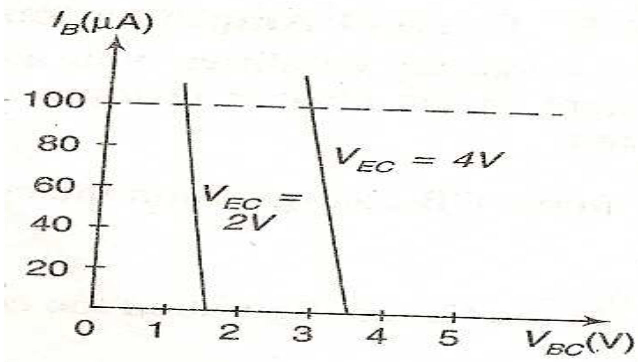



Fig. 4.12 CE Output Characteristics

## C.C.CONFIGURATION:




ig. 4.14 CC Input Characteristics

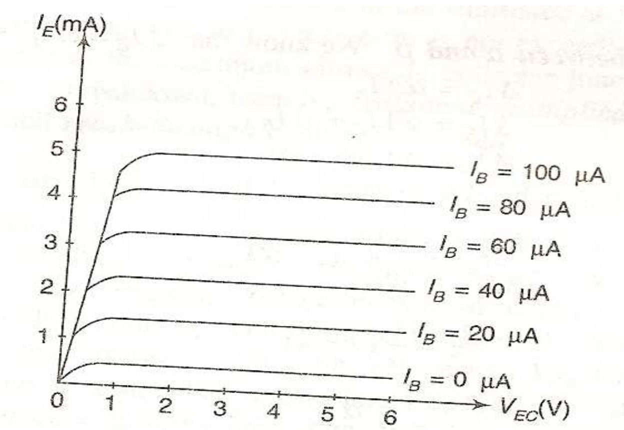



Fig. 4.15 CC Output Characteristics

## EARLY EFFECT OR BASE WIDTH MODULATION. (IN CB CONFIGURATION)

As $V_{CC}$ made to increase the reverse bias, the space charge width between collector and base tends to increase. This results in decrease of effective width of the base. This dependence of base width on collector voltage is known as 'Early Effect'. This decrease of effective base width has three consequences.

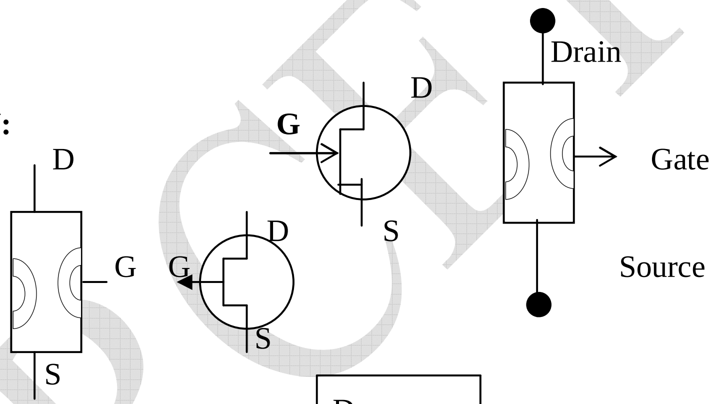
(i) There is less chance of recombination in base region and Ic increases causing $\alpha$ to increase with increase in $V_{CB}$.

(ii) The charge gradient is increased with in the base and current of minority carries injected across emitter junction increases.

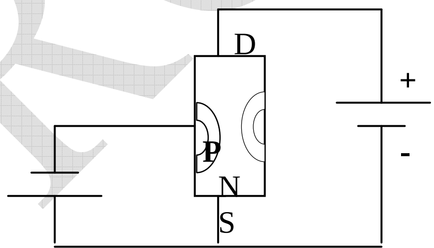
(iii) For extremely large Vcs, the effective base width becomes zero causing voltage breaks down in the transistor. This phenomenon is called the "Punch through".

**JFET CONSTRUCTION:**

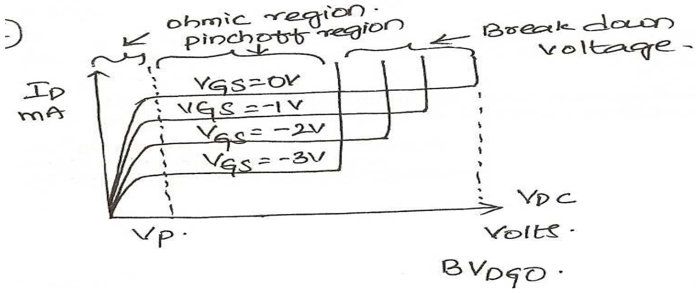
a) N Channel JFET
b) P Channel JFET




**BIASING OF JFET**




**DRAIN CHARACTERISTICS: -**
**OHMIC REGION:-** Drain current increases With drain voltage



**PINCH OFF VOLTAGE($V_P$):**

$V_{DS}$ for which maximumdrain current is there.
Further increase in $V_{DS}$ will not increase $I_D$.

**PINCH OFF REGION: -**

Where drain current is saturated.

**BREAK DOWN VOLTAGE: -**

$V_{DS}$ where JFET breaks down
$V_{GS}$ cut off – Where $I_B$ becomes zero, irrespective of $V_{DS}$.

$V_P = |V_{GS} \text{ cut off}|$

**CHARACTERISTICS OF JFET**

**MUTUAL CONDUCTANCE OR TRANS CONDUCTANCE OF FET ($g_m$)**

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \text{ when } V_{DC} \text{ kept constant.}$$

It is the ratio of small change in the drain current to the corresponding small change in gate voltage when drain voltage is kept constant.

b) Drain resistance $(\gamma_d) = \frac{\Delta V_{DS}}{\Delta I_D}$, $V_{GS}$ kept constant

c) Amplification factor $\mu = \frac{\Delta V_{DC}}{\Delta V_{GS}}$, $I_D$ kept constant.

Q.1) In common base connection $I_E$ = 1mA, $I_C$ = 0.95 mA calculate value of $I_B$.

**(JNTU – 2000)**

$I_B = I_E - I_C = 1 - 0.95 = 0.05$mA.

Q2) In a CB configuration current amplification factor is 0.90 and emitter current is 1mA. Determine base current.

$\alpha = 0.9$, $I_E = 1$mA

$\alpha = \frac{I_C}{I_E}$; $I_C = \alpha . I_E = 0.9 \times 1 = 0.9$mA

$I_B = I_E - I_C = 1 - 0.9 = 0.1$mA.

Q3) A BJT has $I_B$ = 10 μA, α = .99 and $I_{CBO}$ = 1 μA what is collector current.

Solution:

$I_C = \beta I_B + (1+\beta) I_{CBO}$

$B = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-0.99} = \frac{0.99}{0.01} = 99$

$I_C = 99 \times 10 + (1 + 99)1$

$= 990 + 100 = 1090\ \mu A = 1.09$ mA.

Q4) A transistor operating in CB configuration has $I_C$ = 2.98mA, $I_E$ = 3.0mA and $I_{co}$ = 0.01mA. What current will flow in collector circuit of that transistor when connected in $C_E$ configuration and base current is 30μA. **(May,2006)**

Given :

CB = $I_C$ = 2.98mA, $I_E$ = 3.0mA $\therefore \alpha = \frac{2.98}{3.0} = 0.99$

$I_{CO}$ = 0.01mA.

CE = $I_B$ = 30 μA $I_C$ = ? $I_C = \beta I_B$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-0.99} = \frac{.99}{0.01} = 99$$

$I_C$ = $\beta I_B + (\beta + 1)$ Ico.

= $99 \times 30 \times 10^{-6} + (100)0.01 \times 10^{-3}$

= $2.97 \times 10^{-3} + 1 \times 10^{-3}$ = 3.97mA

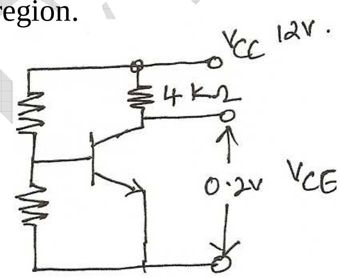
Q 5) Given an NPN transistor for which α = 0.98, Ico = 2μA $I_{EO}$ = 1.6μA. A $C_E$ configuration is used and $V_{CC}$ = 122 and $R_C$ = 4.0K. What is the min. base current required in order that transistor enter in to saturation region.

Given α = 0.98, $I_{CO} = I_{CB}$ = 2μA,

$I_{EO} = I_{CEO}$ = 1.6μA.

$V_{CC}$ 12 $VC_E = V_{CC}$ = 12V,

$R_L$ = 4.0K $I_B$ = ? (In saturation)




**Solution:-**

Where Transistor is in saturation $V_{CE}$ = 0.2 (Assumed)

$\therefore V_{RL}$ = 12 – 0.2 = 11.8 Volts.

$$I_c = \frac{V_{RL}}{R_L} = \frac{11.8}{4\times10^3} = 2.95\times10^{-3} = 2.95mA$$

We know

$Ic = \beta I_B + (\beta+1) I_{CBO}$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = \frac{.98}{0.02} = 49$$

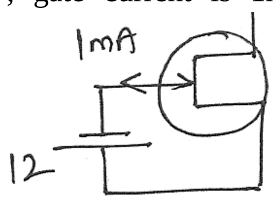
2.95 x 10-3 = 49 IB + (49+1) 2 x 10-6

2950μA = $49I_B$ +100μA

$49I_B$ = (2950 – 100)μA = 2850 μA

$I_B$ = $\frac{2850}{49} = 58.16\mu A$

Q 6) When a reverse gate voltage is 12V, gate current is 1mA. Determine the resistance between gate & source. **(JNTU 2000)**




$$R = \frac{V}{I} = \frac{12}{1\times10^{-3}} = 12k\Omega$$

Q 7) When reverse Gate voltage changes from 4.0 to 3.9V, the drain current changes from 1.3 to 1.6 mA. Find the Trans conductance.

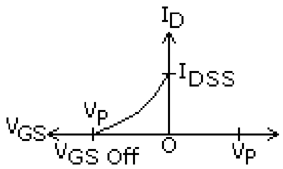
Solution:

Given $\Delta V_{GS} = 4.0 - 3.9 = 0.1$ V

$\Delta I_D = 1.6 - 1.3 = 0.3$ mA

$g_m = ?$ $$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{0.3\times10^{-3}}{0.1} = 3\times10^{-3}\,mho$$

Q 8) A FET has a drain current of 4mA. If $I_{DSS}$ = 8mA and $V_{GS}$ off = -6V. Find values of $V_{GS}$ and $V_P$. **(Nov. 2001)**




Given $I_{DS}$ = 4 mA

$I_{DSS}$ = 8mA

$V_{GS\ off}$ = - 6V.

**Solution: -**

(i) $V_P = |V_{GS}\text{ off}| = |-6V| = 6V.$

(ii) $$I_{DS} = I_{DSC}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$$4\times10^{-3} = 8\times10^{-3}\left(1-\frac{V_{GS}}{6}\right)^2$$

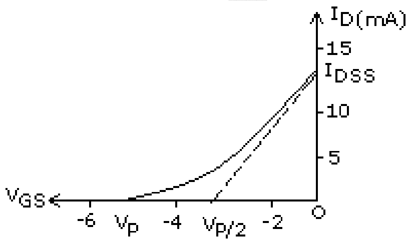
$$\frac{1}{2} = \left(1-\frac{V_{GS}}{6}\right)^2 \; or \; \frac{1}{\sqrt{2}} = 1-\frac{V_{GS}}{6}$$

$(or)0.707 = 1-\frac{V_{GS}}{6};$

or $(or)\frac{V_{GS}}{6} = 1-0.707 = 0.293$

$V_{GS} = 6\times0.293 = 1.758\,Volts.$

**SATURATION DRAIN CURRENT ($I_{DSS}$)**




$$I_{DS} = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 \quad g_m = \frac{2\sqrt{I_{DS}I_{DSS}}}{V_P}$$

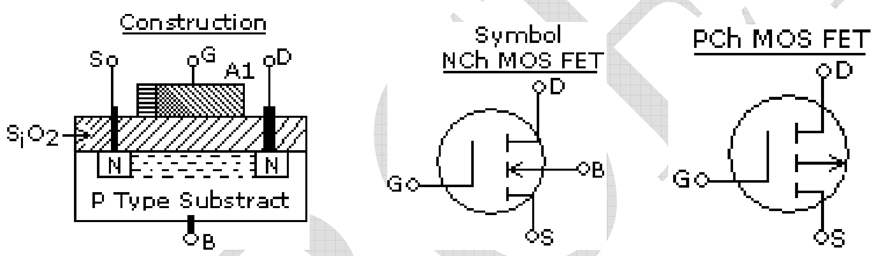
$g_{mo}$ is $g_m$ when $V_{GS} = 0$

$$g_{mo} = \frac{-2I_{DSS}}{V_P}\, and g_m = g_{mo}\left(1-\frac{V_{GS}}{V_P}\right)$$

## COMPARISON OF BJT AND FET

1) FET is uni polar device – current $I_D$ is due to majority (Where as BJT is Bipolar) charge carries only.
2) FET is less noisy as there are no junctions(in conduction channel) FET
3) FET Input impedance is very high (100 mΩ) (due to reverse bias)
4) FET is voltage controlled device, BJT is current controlled device
5) FETs are easy to fabricate
6) FET performance does not change much with temperature. FET has –Ve temp. Coefficient, BJT has +Ve temp. coefficient.
7) FET has higher switching speeds
8) FET is useful for small signal operation only
9) BJT is cheaper than FET.

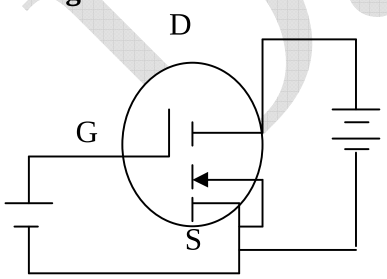
## MOS FET (Metal Oxide Semiconductor Field Effect Transistor)




N regions are highly doped
P regions are lightly doped.
Both N regions (D & S) are repeated by 1 mil. ($10^{-3}$ inch) or So.

A thin insulating layer is over the surface. This is Si $0_2$ ( a metal oxide) layer that curves entire channel region given and a gate of metal (AP) is formed over the Si $0_2$ layer.

**Biasing: -**

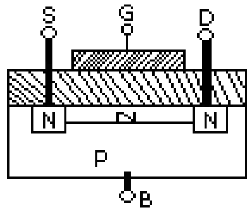


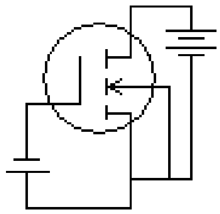

Gate is kept positive w.r.t source. And attracts electrons (or induces negative Charge in the channel opposite to gate) This region acts like a capacitor with $Si0_2$ layer acts as insulator between two plates of the capacitor.

Due to this induced negative region a temporarily N Channel is created from Drain to source or N channel is enhanced. Therefore it is called as Enhancement MOSFET.

Gate leakage current is in the order of $10^{-12}$ Amps. Hence input impedance is very ($10^{10}$ to $10^{15}$ ohms).

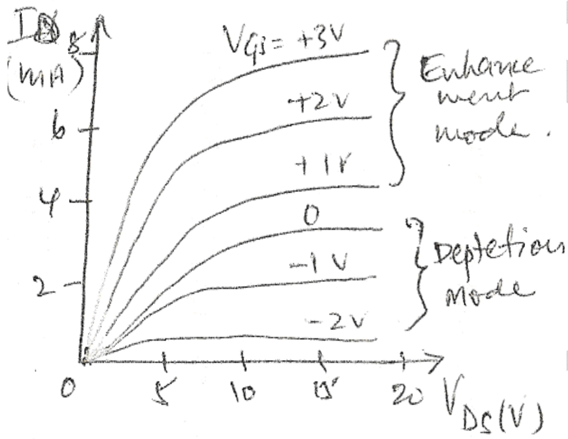
**Depletion Mode.**



N channel exists.
Gate is kept negative wrt source.

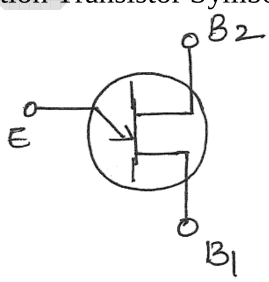
**Volt Ampere characteristics of MOSFET (or) Output characteristics of MOS FET**

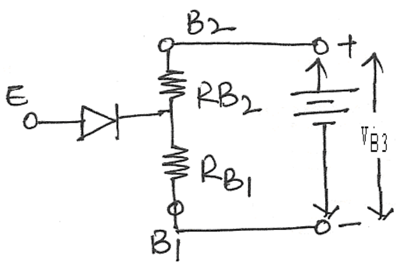



**Precautions of Handling MOS FET**

- MOS FET may be damaged due to high voltage or static change. Thin $Si0_2$ layer get damaged which is between Gate and Channel.
- Static voltage up to 300V may develop across a man if he uses high resistance soled shoes.
- MOS FET are protected by shorting ring that is rapped around all the four terminals.
- Technician handling the MOS FET are required to use shorting strap to discharge static charge.

Q) Explain the working principle of UJT with its characteristics **(May 06, 07).**
Unit Junction Transistor Symbol Equivalent Circuit

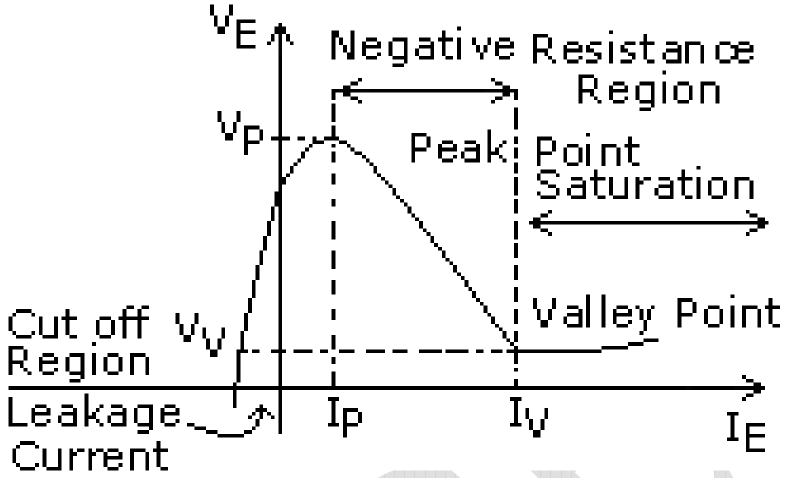



It has only one PN junction. Therefore it is called as Unit Junction Transistor.

- Arrow indicates direction of convectional circuit
- Inter Base resistance ($R_{BB}$) = $R_{B1}$ + $R_{B2}$.

- Intrinsic stand off ratio $\eta = \frac{R_{B1}}{R_{B1+}R_{B2}}$ and ranges from 0.56 to .75.
- Voltage drop across $R_{B1} = \eta V_{BB}$ which reverse biases PN junction.




**Working Principle**

- UJT remains cut off till emitter voltage is greater than $\eta V_{BB}$.
-
- When $V_E > \eta V_{BB}$, large number of holes are injected into the N region.
-
- These holes are repelled by terminal $B_2$ (being +Ve biased) and collected by $B_1$.
-
- Accumulation of holes in E to $B_1$ region reduced the resistance in this section leading to increase in current $I_E$.
-
- UJT has a stable firing voltage $V_P = \eta V_{BB} + V_d$ = voltage across $R_{B1} + V_d$.
- $(R_{B1}) / (R_{B1} + R_{B2})$ . $V_{BB}$.

**UJT RELAXATION OSCILLATOR.**

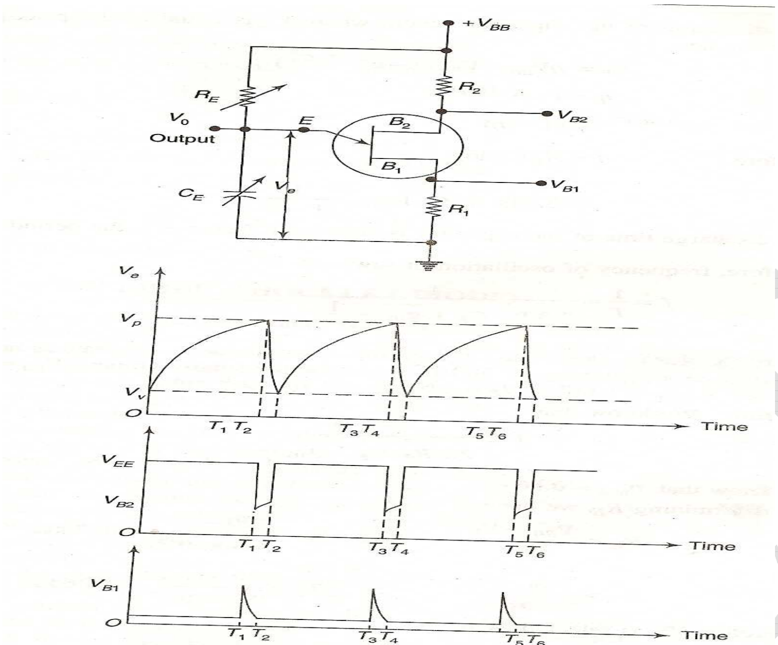
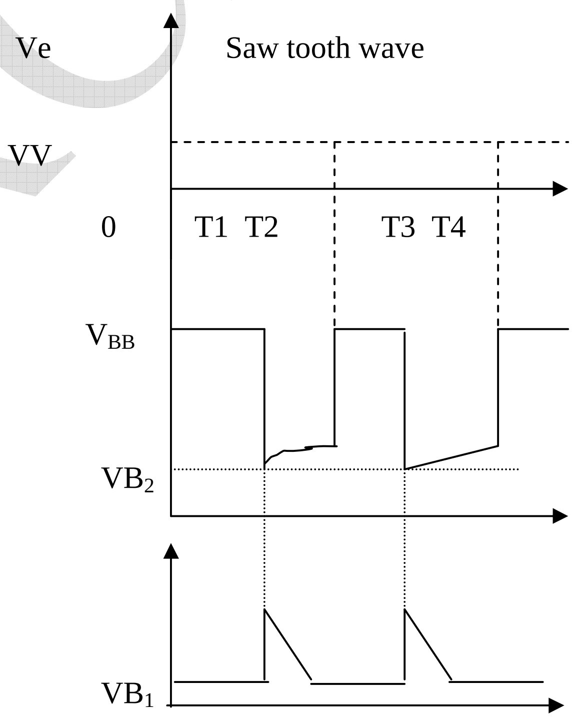



Fig. 4.31 UJT Relaxation Oscillator



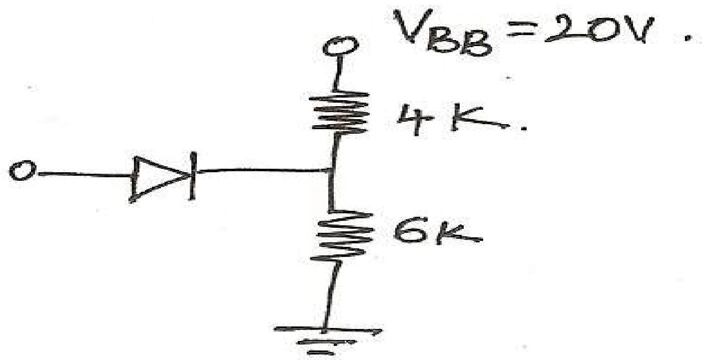

- UJT is used to generate saw tooth waveform
- $R_1$ and $R_2$ are external resistors(not $R_{B1}$ & $R_{B2}$)
- By changing $C_E$ and $R_E$ we can change the frequency of oscillation.
- $V_C = V_{BB}\left(1 - e^{\frac{-t}{R_E C_E}}\right)$
- $V_P = \eta V_{BB} = V_{BB}\left(1 - e^{\frac{t}{R_E C_E}}\right)$

or $n = \left(1 - e^{\frac{-t}{RECE}}\right)$, taking log e both sides t = $R_E C_E \log_e(1/1-n)$

or t = 2.303 $R_E C_E$ log10 (1/1-n)

- Frequency of Oscillation $f = \frac{1}{t} = \frac{1}{2.3 R_E C_E \log_{10} \frac{1}{1-n}}$

Q1) A silicon UJT has an inter base resistance $R_{BB}$ = 10kΩ and $R_{B1}$ = 6kΩ with $I_E = 0$. If $V_{BB}$ = 20V and $V_E < V_P$ find UJT current (c) and $V_P$ **(Dec.2003)**




$R_{BB}$ = 10KΩ; T current (c) = $\frac{V_{BB}}{R_{BB}} = \frac{20}{10K} = 2mA$

$V_P = V_{RB1} + V_d$ = 6K x 2mA + 0.7V = 12.7Volts

Q2) If $\eta$ = 0.8 and $V_{BB}$ = 15V and $V_d$ = 0.7V, find the value of $V_P$. **(June 2005)**

**Solution:**

$V_P = \eta\ V_{BB} + V_d$ = 0.8 x 15 + 0.7 = 12.7 Volts

Q 3) A UJT has a firing potential of 20V. It is connected across the capacitor of a series RC circuit with R = 100K and C = 1000 Pf supplied by a source 40V DC. Calculate the time period of saw tooth wave form generated.

**Solution: -**

$V_C = V_{BB}\left(1 - e^{-t/R_C}\right)$

$V_C$ = 20V, $V_{BB}$ = 40V, R = 100K, C = 1000Pf.

$20 = 40\left(1 - e^{\frac{-t}{10^5 \times 1000 \times 10^{-12}}}\right) or \frac{1}{2} = 1 - e\frac{-t}{10^4}$

Or $\frac{1}{2} = 1 - e^{-10^4 t}$ or $e^{-10^4 t} = 1 - 1/2 = 1/2$

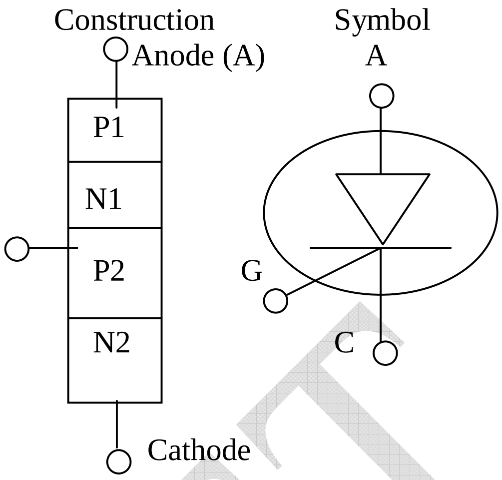
$-10^4 t \log_e^e = \log e 1/2 or -10^4 t = -0.693$

$t = \frac{0.693}{10^4} = \frac{.693 \times 10^6}{10^4} \mu\sec = 69.3 \mu\sec.$

**SILICON CONTROLLED RECTIFIER:**

1) Iit is a four layer three Terminal device

2) Leakage current in silicon is very small compared Germanium



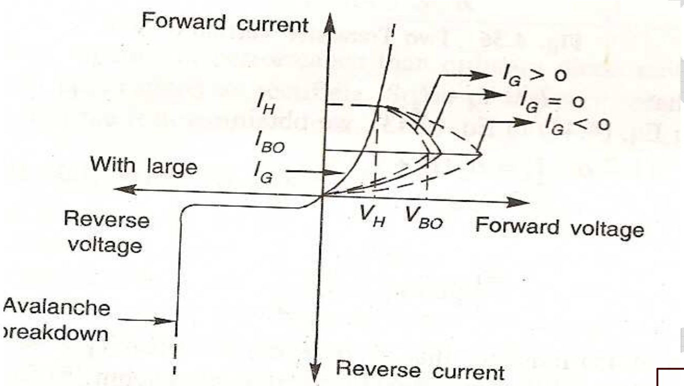
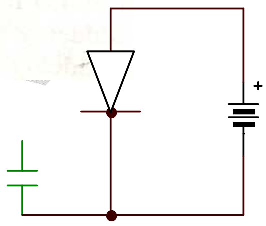




**Fig. 4.35** Characteristics of SCR

a)cut off region
b)negative Resistance region



Biasing of SCR.

**CHARACTERISTICS OF SCR.**

3) SCR acts as a switch when it is forward biased.

4) When gate is open i.e., $I_G = 0$, and anode voltage is applied junctions $P_1 - N_1$ and $P_2 - N_2$ are forward biased where $N_1 - P_2$ is reverse biased. Only small reverse current flows.

5) If we increase anode voltage further, at one stage anode current increases suddenly and voltage across the SCR falls to holding voltage VH.

6) Once SCR fires (conducts), it will remain in conduction till the current through the device is reduced less than IH, adding current by reducing applied voltage (to less than holding voltage) close to zero.

7) The firing angle can be varied by varying the Gate voltage. With very large positive (gate current break over may occur at very low voltage and SCR works as if it is a normal PN diode.

**TWO TRANSISTOR VERSION OF SCR.**

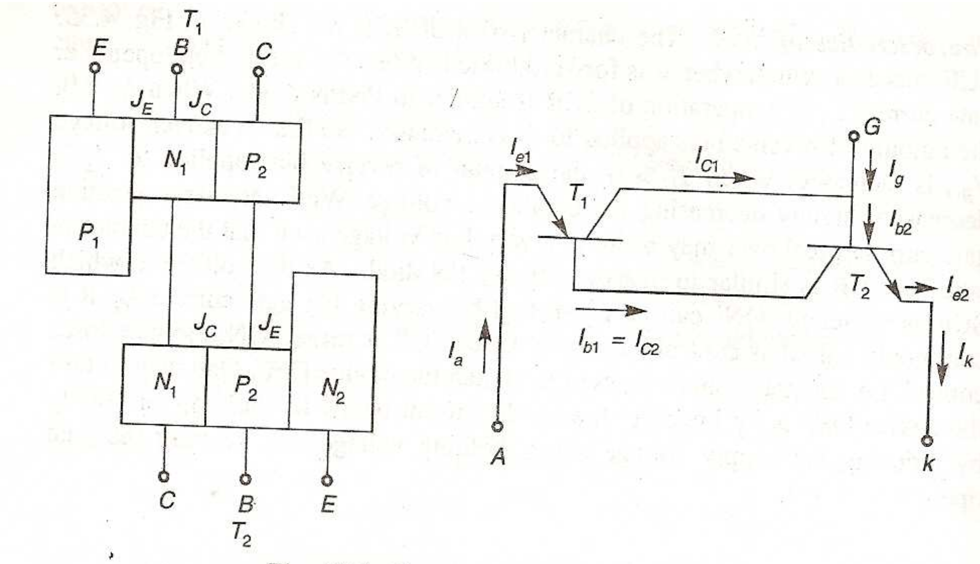



Fig. 4.36 Two Transistor Version of SCR

-$T_1$ is PNP and $T_2$ is NPN.

$I_{b1} = I_A - I_{e1} = I_A - \alpha_1 I_A = I_A(1 - \alpha_1)$ - (1)

$I_{b1} = I_{c2}$ and $I_{c2} = \alpha_2 I_k$ - (2)

$I_{b1} = I_A(1 - \alpha_1) = \alpha_2 I_K$ - (3)

We know $I_k = I_A + Ig$. ( $I_A = I_{C1} + I_{b1}$) - (4)

Putting the value of $I_k$ from eqn. (4) in eqn. (3)

$I_A(1 - \alpha_1) - \alpha_2(I_A + Ig)$

$I_A(1 - \alpha_1) = \alpha_2(I_A + Ig)$

$I_A(1 - \alpha_1 - \alpha_2) = \alpha_2$ Ig. Or $I_A = \left(\frac{\alpha_2 I_g}{1-(\alpha_1+\alpha_2)}\right)$ -(5)

Equation 5 indicates that if$(\alpha 1 + \alpha 2) = 1$, $I_A = \infty$

- SCR is also called as Thirster
- Latching current ($I_L$) the min. current required to fire the device
- Holding current ($I_H$) – min. current to keep the SCR conductivity
- Voltage safety factor $V_f = \frac{PIV}{\sqrt{2} RMS\ of\ operating\ voltage.}$

Value of $V_f$ is 2 to 2.7.

**SCR Half wave Rectifier.**

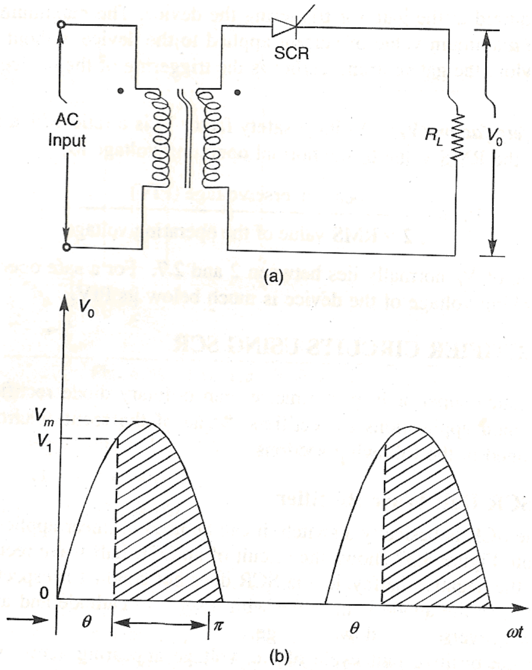



**Fig. 4.37** SCR Half Wave Rectifier

SCR does not conduct during negative half cycle (like normal PN diode)

- Firing angle θ depends on gate voltage
- Conduction angle is (π - θ)

**Average DC output**

$$V_{av} = \frac{1}{2\pi}\int_0^{\pi} V_m \sin wt.dwt$$

$$= \frac{1}{2\pi}\left[-V_m \cos wt\right]_0^{\pi}$$

$$= \frac{1}{2\pi}\left[-V_m \cos\pi - \cos\theta\right]$$

$$= \frac{1}{2\pi}\left[-V_m\left(-1-\cos\theta\right)\right]$$

$$= \frac{V_m}{2\pi}\left(1+\cos\theta\right)$$

**RMS VOLTAGE:** $V_{RMS}$ is given by $V_{RMS} = \frac{V_m}{2}\left[\frac{1}{\pi}\left(\pi-\theta+\sin 2\theta\right)\right]^{1/2}$

## SCR FULL WAVE RECTIFIER

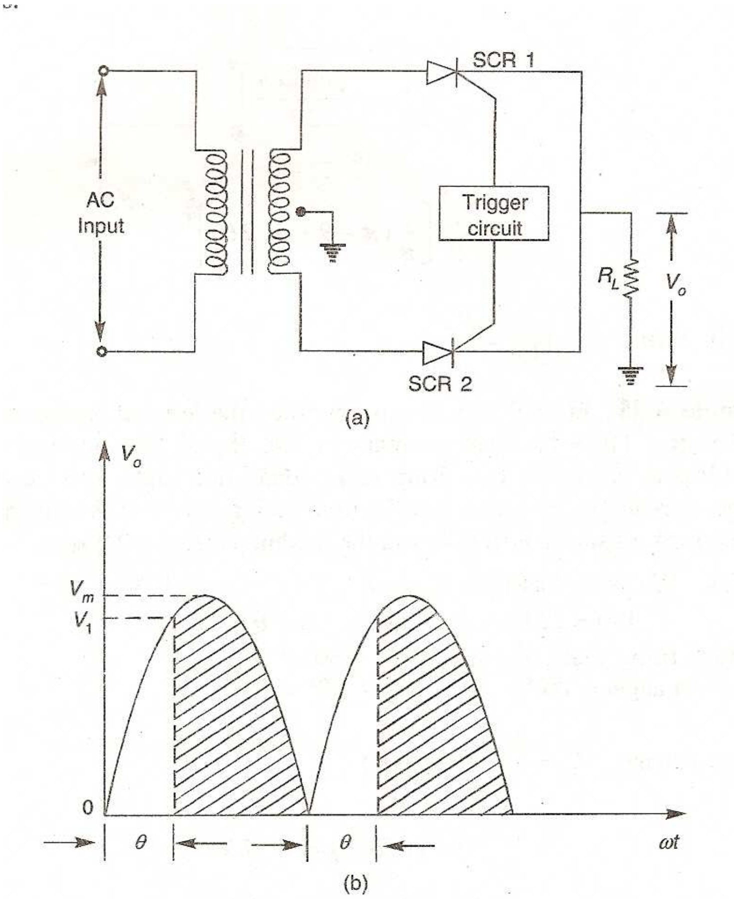



Fig. 4.38 SCR Full Wave Rectifier

$$V_{DC} = \frac{Vm}{\pi}(1+\cos\theta)$$

Q) An SCR FWR is connected to 250V. 50 Hz mains to supply ac voltage to resistive load of 10 Ω for firing angle of 90°. Find DC output voltage and load current.

**(May, 2000)**

**Solution: -**

Given $V_{RMS}$ = 230V, $R_L$ = 10Ω, θ = 90°

$V_{DC}$ = ? $I_L$ = ?

$$V_{RMS} = \frac{V\max}{\sqrt{2}}$$

$$V_{DC} = \frac{V_m}{\pi}(1+Cos\theta)$$

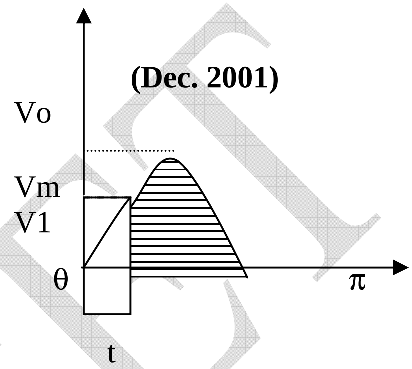
Or $V_{max} = V_{RMS}\sqrt{2} = 250\sqrt{2} = 353.6$ volts

$$\frac{353.6}{\pi}(1+\cos 90) = 112.6\,volts$$

$$I_L = \frac{V_{DC}}{R_L} = \frac{112.6}{10} = 11.26\,Amps$$

Q 2) A sinusoidal voltage V = 200 sin 314 t is applied to an SCR whose forward break down voltage is 150V. Determine the time during which SCR remain off.

**(Dec. 2001)**




Solution: -

Given $V_1 = 150V$, $V_m = 200V$

W = 314 θ = ? t = ?

$$V_1 = V_m \sin\theta \quad \text{or} \quad \sin\theta = \frac{V_1}{V_m} = \frac{150}{200} = \frac{3}{4}$$

$\theta = \sin^{-1} 3/4 = 48.6°$

T = 1/f f = ? w = 2πf = 314 or f = 314/2π = 50Hz.

T= 1/50 = 0.02sec = 20 m. sec.

t = $T \times \frac{\theta}{360} = 20 \times \frac{48.6}{360} = 2.7\,m\sec$

Q 3) A half wave rectifier employing SCR is adjusted to have a gate current of 1mA and its forward breakdown voltage is 150V. If a sinusoidal voltage of 400V peak is applied, determine.

i) Firing angle (ii) Average output voltage

iii) Average current for a load resistance of 200Ω

**iv)** Power output. **(Nov. 2002)**

Given

$V_1 = 150V$, $V_m = 400V$, θ = ? $V_{DC}$ = ? $I_{DC}$ = ? $P_{DC}$ = ? $R_L = 200Ω$

Solution: -

$V_1 = V_m \sin\theta$, or Sin θ = $V_1 / V_m$ = 150/400 = 3/8 = 0.375.

θ = $\text{Sin}^{-1}$ 0.375 = 22°.

$$V_{DC} = \frac{V_m}{2\pi}(1+\cos\theta) = \frac{400}{2\pi}(1+\cos 22°) = \frac{400}{2\pi}(1.927) = 122.6\,volts$$

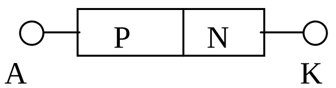
$$I_{DC} = \frac{V_{DC}}{R_L} = \frac{122.6}{200} = 0.613\,Amps.$$

$$P_{DC} = V_{DC}.I_{DC} = 122.6 \times 0.613 = 75.15\,Watts.$$

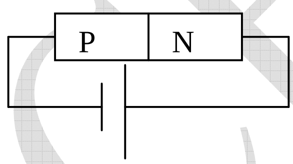
| Color | Construction | Typical FWD Voltage (V) |
|---|---|---|
| Amber | Al In Ga P | 2.1 |
| Blue | Ga N | 5.0 |
| Green | Ga P | 2.2 |
| Orange | Ga As P | 2.0 |
| Red | Ga As P | 1.8 |
| White | Ga N | 4.1 |
| Yellow | Al In Ga P | 2.1 |

- Reverse break down voltage of LED is very less – 3 to 5 volts
- LEDs are used for displays, including seven-segment display.

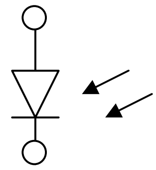
**PHOTO DIODES**:




Biasing




Symbol



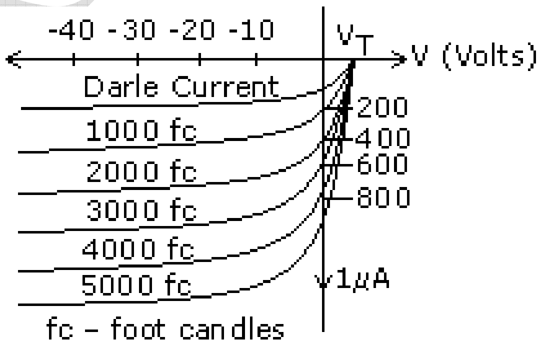
- Photo diode is always reverse biased
- When light falls on reverse biased junction, electrons are liberated and an EMF is available at the terminals, which leads to current through external load.

W = hf Joules

1 Lumen = 1.496 x $10^{-10}$ watts

- Current will be zero only for a
- positive voltage $V_T$.
- Current α luminous flux

application – signal detector, alarm systems.




**COMPARISON OF CB, CE, CC CONFIGURATIONS:**

Q) Summarize salient features of characteristics of BJT operating in CE, CB, CC configurations. **(August 07)**

(Auth: EDC by Salivahanam : P –112)

| S. No. | Property | CB | CE | CC |
|---|---|---|---|---|
| 1 | Input Resistance | Low (≈100Ω) | Moderate(≈750Ω) | High (≈750kΩ) |
| 2 | Output resistance | High (≈450k) | Moderate (≈45k) | Low (≈75Ω) |
| 3 | Current gain | 1 | High | High |
| 4 | Voltage gain | ≈150 | ≈500 | < 1 |

| | | | | |
|---|---|---|---|---|
| 5 | Phase shift between input and output voltages | 0 or 360° | 180° | 0 or 360° |
| 6 | Applications | High frequency circuits | AF circuits | Impedance matching. |

Q 1b) Calculate the values of $I_E$, $\beta_{dc}$ and $\alpha_{dc}$ for a transistor with Ic = 13μA, $I_B$=200mA, $I_{CBO}$ = 6μA. Also determine the new level of Ic which will result in reducing $I_B$ = 100mA. **(August 07)**

Solution: -

Given Ic = 13 μA find Ic, when $I_B$ = 100 mA

$I_B$ = 200mA PART – I

$I_{CBO}$ = 6μA $I_E$ = ? $\beta_{dc}$ = ? $\alpha_{dc}$ = ?

**PART – I**

When $I_B$ = 200mA $I_c$ cannot be 13 μA.

as Ic = β X. $I_B$.

Assume Ic = 13 Amperes

Then $\beta_{dc} = \frac{I_C}{I_B}$ = 13/200 x $10^3$ = 65

$I_E = I_C + I_B$ or $I_E$ = 13+0.2 Amperes.= 13.2 Amperes

We can also use the formulae $I_E = \frac{1}{1-\alpha} I_{CBO} + \frac{1}{1-\alpha} IB,$

Which will also result $I_c \approx$ 13.2 Amperes.

$$\alpha_{dc} = \frac{I_C}{I_E} = \frac{13}{13.2} = 0.985$$

**PART – II**

$I_C = \beta_{dc.} I_B = 65 \times 200 \times 10^{-3}$ = 6.5 Amperes

5. a) A transistor operating in CB configuration has $I_c$ = 2.98 mA in $I_E$- =3.00mA and Ico = 0.01mA. What current will flow in the collector circuit of the transistor when connected in CE configuration with base current of 30μA **(May 2006)**

**Solution:** To find

Given $I_c$ = 2.98 mA If $I_B$ = 30 μA, $I_c$ = ?

$I_E$ = 3 mA

$I_{co}$ = 0.01 mA

$I_c = \beta I_B + (\beta+1)$ ICO and $\beta = \frac{\alpha}{1-\alpha}, \alpha = \frac{I_C}{I_E}$

$\alpha = \frac{2.98}{3.0} = 0.99 \quad \beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-0.99} = 99$

$I_c$ – 99 x 30 x $10^{-6}$ + (99+1) x 0.01 x $10^{-3}$ = 3970μA = 3.97 mA.

5(b) The reverse saturation current in a transistor is 8μA. If the transistor common base current gain is 0.979, calculate the collector and emitter current for 40μA base current.

**(May 2006)**

**Solution:** To find

Given $I_{CO} = I_{CBO} = 8\mu A$ $I_C$ & $I_E$ for $I_B = 40\mu A$

$\alpha = 0.979$

$$I_E = \frac{1}{1-d} I_{CBO} + \frac{1}{1-\alpha} I_B; \quad \frac{1}{1-\alpha} = \frac{1}{1-0.979} = 47.62$$

$$I_E = 47.62 \times 8 \times 10^{-6} + 47.62 \times 40 \times 10^{-6} = 2285 \times 10^{-6} = 2285 \mu A$$

$I_C = I_E - I_B = 2285 - 40 = 2245\ \mu A.$

Q 6b) Given an NPN transistor for which $\alpha = 0.98$, $I_{CO} = 2\mu A$ and $I_{EO} = 1.6\mu A$. A common emitter connection is used and $V_{CC} = 12V$ and $R_L = 4.0K$. what is the minimum base current required in order that transistor enter into saturation region.

**(Nov. 05)**

Solution:

Given $d = 0.98$ To Find

$I_{CO} = 2\mu A$ $I_B$ for $I_{csat}$

$I_{EO} = 1.6\mu A$

$V_{CC} = 12V$

$R_L = 4.0\ K.$

When the transistor is in saturation $I_c = I_{csat}$ and $V_{CE}$ of ideal transistor = 0 volts.

$$I_{csat} = \frac{V_{cc}}{R_L} = \frac{12}{4000} = 3mA$$

$$I_B = \frac{Ic}{\beta} \text{ and } \beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = 49$$

$$I_B = \frac{3 \times 10^{-3}}{49} = 0.061 mA \quad \text{Or} \quad 61\mu A.$$

Q 9b) The current gain of a transistor in CE circuit is 49. Calculate CE gain and find base current where the emitter current in 3mA.

**Solution**

Given $\beta = 49$ To find $\alpha = ?$

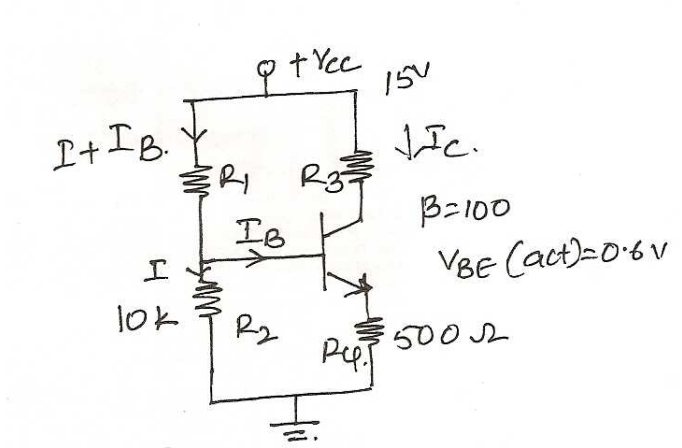
$I_B$ for $I_E = 3mA$.

$$d = \frac{\beta}{1+\beta} = \frac{49}{1+49} = 0.98$$

$I_E = (\beta+1)\, I_B$ or $I_B = \frac{I_E}{1+\beta} = \frac{3\times10^{-3}}{1+49} = 60\mu A$

Q 1b) In the circuit shown if Ic = 2mA and $V_{CE}$ = 3V. Calculate $R_1$ and $R_3$.
**May 07, Aug. 06, 07)**

Solution: -




$I_C$ = 2mA and β =100

$$\therefore I_B = \frac{Ic}{\beta} = \frac{2\times10^{-3}}{100} = 200\mu A$$

$I_E = I_C + I_B$ = 2mA+20μA
= 2020μA IB

$V_E = I_E.R_4 = 2020 \times 10^{-6} \times 500$

$V_E$ = 1.01 volts

$V_B = V_E + V_{BE}$ = 1.01 + 0.6 = 1.61 volts

$V_B = V_{R2}$ = 1.61 volts

$$I = \frac{V_B}{R_2} = \frac{1.61}{10\times10^{-3}} = 0.161mA - 161\mu A$$

$V_{R1} = V_{CC} - V_{R2}$ = 15 - 1.61 = 13.39 volts

$$R_1 = \frac{V_{R1}}{I + I_B} = \frac{13.39}{(161+20)10^{-6}} = \frac{13.39}{181\times10^{-6}} = 73.97k\Omega$$

$R_1$ = 7397 kΩ

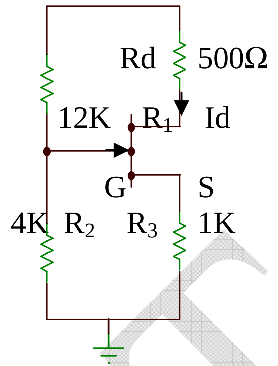
$V_{R3} = V_{CC} - V_{CE} - V_E$ = 15 – 3 – 1.01 = 10.99 volts

$$R_3 = \frac{VR_3}{I_C} = \frac{10.99}{2\times10^{-3}} = 5.49k\Omega$$

$R_3 = 5.49k\Omega.$

Q 3) For the JFET shown in the circuit with the voltage divider bias as shown below, calculate $V_G$, $V_S$, $V_D$ and $V_{D}s$ if VGS = - 2V **(Sep. 2006)**

Solution:



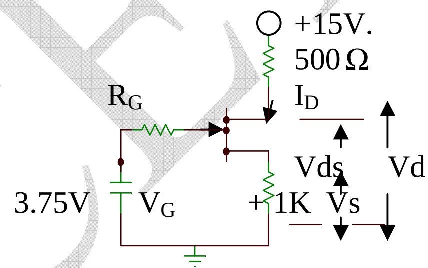

$$V_G = \frac{V_{DD.}R_2}{R_1 + R_2} = \frac{15 \times 4K}{(12+4)k} = \frac{15}{4} = 3.75V$$

Since gate current is negligible voltage drop
Across RG = 0

$V_{GS} = V_G - I_{DRS}$.

- 2V = 3.75 – $I_{DRS}$

$I_{dRs}$ = 3.75 + 2 = 5.75V = Vs.
Id = 5.75/1R = 5.75mA
Voltage drop across RL = $I_{DRL}$.




= 5.75 x 10-3 x 500 = 2.875V

$V_{DS} = V_{DD} - I_{DRL} - I_{DRS}$

= 15 – 2.875 – 5.75 = 6.375 volts

$V_D = V_{DD} - I_{DRL}$ = 15 – 2.875 = 12.125V

**COMPARISON OF MOS FET WITH JFET**

1) In JFET, the transverse electric field across the reverse biased P N junction controls the conductivity of he channel. In FET Transverse electric field is induced across the insulating layer.
2) Input impedance of MOS FET is much higher ($10^{10}$ to $10^{15}$ Ω) compared to that of JFET ($10^8$Ω) because gate is insulated from channel.
3) The output characteristics of JFET are flatter than that of MOS FET because drain resistance of JFET is much higher than MOS FET.
4) JFET is operated in depletion mode only where as MOSFET can be operated in depletion and enhancement mode.
5) MOSFET are easier to fabricate than JFET
6) MOSFETs are easily get damaged due to static change
7) In MOSFET source and drain can be interchanged
8) CMOSFETs discipates very low power
9) MOS FETs are widely used in VLSI.