SREENIVASA INSTITUTE of TECHNOLOGY and MANAGEMENT STUDIES
(Autonomous)
Academic Regulations for M. Tech
(Effective for the students admitted into I - year from the Academic Year 2013-2014 onwards)

1. Eligibility for admission:

- Admission to the above programme shall be made subject to the eligibility, qualifications and specialization prescribed by the university from time to time.
- Admission shall be made strictly on the basis of merit rank obtained by the qualifying candidates at an entrance test (PGSET) to be conducted by the university/ GATE or on the basis of any other order of merit approved by the university, subject to reservations prescribed by the Government of Andhra Pradesh.

2. Award of degree:

- A candidate shall be eligible for the award of M.Tech degree, if he/ she satisfies the minimum academic requirements in every subject including the seminar, comprehensive viva-voce and project work successfully in not less than the prescribed course work duration and not more than double the prescribed course work duration and he/ she has not involved in any sort of indisciplinary activities certified by the Principal.
- Students, who fail to fulfill all the above academic requirements, shall forfeit their seat in B.Tech course and their admission will stand cancelled.

3. Post-Graduate courses offered:

M.Tech with specialization

1. Computer Science and Engineering (CSE).
2. Software Engineering(CSE)
3. VLSI system design(ECE)
4. Communication Systems(ECE)
5. Electrical Power Engineering(EEE)
6. Power Electronics(EEE)

4. Course pattern:

The entire course work of M.Techconsists of four semesters. During I-I and I–II semesters the student has to study the course work and in II-I and II-II semesters he/ sheshould carryout the project work.

Table 1: Contact periods, credits and marks

	Semester				
	Periods/ week	Credits	Internal marks	External marks	Total marks
Theory	04	04	40	60	100
Practical	03	02	40	60	100
Seminar		02	100	-	100
Comprehensive viva- voce		02	100	-	100
Project		12	40	60	100

Table 2: Course pattern and total credits

Semester	No. of subjects	Number of labs	Total credits	
I-I	06	02	6x4 + 2x2=28	28
I-II	06	02	6x4 + 2x2=28	28
II-I	Seminar			2
	Comprehensive viva-voce (II-I- Semester)			2
II-II	Project Work			12
Total credits				72

5. Attendance:

- A student shall be eligible to appear for external examinations, if he/ she acquires a minimum of 75% of attendance in aggregate of all the subjects in a semester.
- **Shortage of attendance below 65% in aggregate shall in NO case be condoned.**
- Condonation of shortage of attendance in aggregate up to 10% (65% or above but below 75%) in each semester may be granted on valid reasons only.
- Students whose shortage of attendance is not condoned in any semester are not eligible to take their external examination of that class and their registration shall stand cancelled.
- A student will not be promoted to the next semester unless he/ she satisfies the attendance requirements of the present semester and can seek re-admission for that semester when offered next.
- A stipulated condonation fee shall be payable to the college towards the shortage of attendance.

6. Distribution and credence of marks:

a. Evaluation of student's performance:

- The performance of a student in each semester shall be evaluated subject-wise with a maximum of 100 marks for each theory and each practical subject. In addition, a seminar for 100 marks and project work for 100 marks shall be evaluated.
- In professional theory subjects internal evaluation will be for 40 marks (15 marks for each internal examination and 10 marks for 'Advanced Technical Study') and 60 marks for the external examination.

b. Advanced Technical Study:

In 'Advanced Technical Study', the student will select one advanced topic beyond the text book material for each theory subject in the curriculum for that semester and appear for the test to be conducted in that topic for 10 marks.

c. Internal examinations:

- During the semester, there shall be **two** internal examinations for theory subjects. Each internal examination question paper consists of 5 short answer questions for 10 marks and 5 descriptive answer questions, out of which the student has to answer 3 questions for 20 marks with a total duration of 2 hours.
- I- internal examination shall be conducted in units-1 and 2 and II-internal examination shall be conducted in units- 3, 4 and 5 of syllabus.
- 'Advanced Technical Study' internalexamination will be conducted for 10 marks along with II-internal examination, in the topic selected by the student in consultation with the subject staff concerned.
- If there is any fraction in the marks secured by the student in any subject in the internal examinations, then it will be rounded off to the next nearest highest mark.

- The cumulative marks secured by the student in both the internal examinations and 'Advanced Technical Study' examination for a maximum of 40 will be considered internal marks.

d. Make-up examination:

- One make-up internal examination shall be conducted at the end of the semester but before the practical examinations in all the five units for 15 marks or 30 marks as the case may be.
- Make-up examinations will be conducted for those students who are absent for either one or both internal examinations on medical grounds or with genuine valid reasons only with the written permission of the HOD/ Principal.
- Make-up examination will be conducted for the absentees in 'Advanced Technical Study' for 10 marks.

e. External examination:

- The external examination question paper consists of short answer questions (without choice) for 10 marks and 5 descriptive answer questions of equal credence with internal choice for 50 marks for a total duration of 3 hours.

f. Seminar and comprehensive viva-voce:

- The seminar and comprehensive viva-voce shall be evaluated by a three member committee consisting of HOD/HOD's nominee, co-ordinator and one senior faculty member.
- For the seminar, the student shall collect the information on a specialized topic and prepare a technical report, showing his understanding about the topic and submit the same to the department before making presentation. The report and the presentation shall be evaluated by the above three member committee.
- Comprehensive viva-voce pertaining to the student's specialization will be conducted for 100 marks at the end of II-I-semester by the above three member committee. He/ she should secure 50% marks to acquire the required credits.

g. Project work:

Out of a total of 100 marks for the project work, 40marks shall be for internal evaluation and 60marks for the external examination (viva-voce).

h. A student eligible to appear for the external examination in a subject, but absent for it or has failed in it may appear for that subject at the next supplementary examination offered.

7. Minimum academic requirements:

Academic requirements to be satisfied besides the attendance mentioned in section-**5.**

- A student shall be deemed to have satisfied the minimum academic requirements and earned the credits allotted to each theory, practical, seminar, comprehensive viva-voce and project, if he/ she secures a minimum of 50% of marks in the external examination and a total of 50% of marks in the internal and external examinations put together for that particular subject.
- A student should get 50% of total credits in every academic year for promotion to next academic year

8. Re-registration for improvement of internal marks:

Conditions to avail the benefit of improvement of internal marks:

- The candidate should have completed the course work and obtained the examination results for I and II-semesters.

- Out of the subjects the candidate has failed in the examination due to lack of internal marks secured being less than 50%, the candidate shall be given one chance for each theory subject and for a maximum of three theory subjects for improvement of internal evaluation marks.
- The candidate has to re-register for the chosen subjects and fulfill the academic requirements as and when they are offered.
- For each subject the candidate has to pay a fee equivalent to one- third of the semester tuition fee and the amount is to be remitted in the form of DD in favor of the Principal, SITAMS payable at Chittoor along with a requisition through the HOD/HOD's nominee of the respective department.
- In case of availing the chance of improvement of internal marks, both the internal as well as the external marks secured by the candidate in the previous attempts for the registered subjects will stand cancelled.

9. Evaluation of Project work / Dissertation:

- Every candidate shall be required to submit thesis/ dissertation after taking up a topic approved by the Project Review Committee (PRC).
- PRC shall be constituted by the Principal with a senior faculty member as the Chairperson, HOD/ HOD's nominee, co-ordinator and project supervisor.
- A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects (theory and practical).
- A candidate has to submit the title, objective and plan of action of his/ her project work to the PRC for its approval in consultation with the project supervisor and after approval only the project work can be started.
- If a candidate wishes to change his /her supervisor or topic of the project he/ she can do so with an approval of PRC. However, the PRC shall examine whether the change of topic/ supervisor leads to a major change of his/ her initial plans of project proposal. If so, his / her date of registration for the project work starts from the date of change of supervisor/ topic as the case may be.
- The internal evaluation shall be done by the PRC on the basis of two seminars to be given by each student on the topic of his /her project.
- A candidate shall submit status report in two stages at least with a gap of 3 months.
- The work on the project shall be initiated at the beginning of II-I-semester and the duration of the project is for two semesters. A candidate is permitted to submit the project thesis only after successful completion of theory and practical courses with the approval of PRC in not earlier than 180 days from the date of registration of the project work. For the approval of PRC, the candidate shall submit the draft copy of thesis to the Principal (through HOD) and shall make an oral presentation before the PRC.
- Three copies of the project thesis certified by the supervisor shall be submitted to the institute.
- The evaluation of project work shall be conducted at the end of the II-II-semester.
- The HOD/ HOD's nominee will submit a panel of 5 examiners to the Principal through the Controller of the Examinations, who are eminent and expertise in that field with the help of the guide and HOD concerned. The thesis shall be adjudicated by any one external examiner selected from the panel that is submitted by the Controller of Examinations in consultation with the Principal.
- If the report of the examiner is not favorable, the candidate shall have to revise and resubmit the thesis, in the time frame as stipulated by PRC. If the report of the examiner is unfavorable again, the thesis shall be summarily rejected.
- If the report of the examiner is favorable, viva-voce examination shall be conducted by PRC and the examiner who adjudicated the thesis. The HOD shall coordinate and make arrangements for the conduct of viva-voce examination.
- If the candidate fails in viva-voce, then he/ she has to reappear for the viva-voce examination after 90 days. If he/ she fails again in the second viva-voce examination, he/ she will not be eligible for the award of the degree.

10. Re-admission:

When a student is detained due to lack of credits/ shortage of attendance he/ she has to get re-admitted for that semester/ year after fulfillment of academic regulations, whereas he/ she continues to be in the academic regulations in which he/ she is admitted.

11. Class committee:

- Every class shall have a class committee consisting of teachers of the class concerned, student representatives and a Chairperson who does not teach that class. The overall goal of the class committee is to improve the teaching-learning process.

The functions of the class committee are to:

- Solve the problems experienced by students in the class room/the laboratories.
- Clarify the regulations of the degree programme and the details of rules therein.
- Inform the student representatives about the academic schedule, course structure including the dates of assessments and the syllabus coverage for each assessment.
- Enlighten the student representatives about the regulations regarding credence used for each assessment. In case of practical courses (laboratory/ project work/ seminar etc.) the breakup of marks for each experiment/ exercise/ module of work/ assignments and evaluation pattern should be clearly discussed in the class committee meeting and informed to the students.
- Analyze the performance of the students of the class after each test and final examinations, finding the ways and means for solving problems, if any (in the class committee held after the external examinations, the student representatives should not be present).
- Identify the weak students, if any, and request the teachers concerned to provide some additional help/ guidance/ coaching to them
- The class committee should be constituted by the HOD one week in advance before the commencement of class work for the semester.
- The Chairperson may invite the faculty members and the HOD to the meeting of the class committee along with the students' representatives.
- The Principal may participate in any class committee of the institution.
- The Chairperson is required to prepare the minutes of every meeting and submit the same to the Principal within two days after the meeting is over and arrange to circulate it among the students and teachers concerned. If there are certain vital points in the minutes that require immediate action to be taken by the management, the same shall be brought to the notice of the Management by the Head of the Institution.
- The first meeting of the class committee shall be held within one week from the date of commencement of the semester. Subsequently, two or three such meetings may be held in a semester at suitable and convenient dates.
- The class committee Chairperson shall display the cumulative attendance particulars of each student on the notice board at the end of every such meeting to enable the students to know their attendance details.
- During these meetings the student members representing the entire class, shall significantly interact and express the opinions and suggestions of the other students of the class in order to improve the effectiveness of the teaching-learning process.

12. Transitory regulations:

Candidates who have been detained due to lack of attendance or have not fulfilled academic requirements or failed after having undergone the course in the earlier regulations or discontinued and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same or equivalent subjects as and when subjects are offered, subject to section-**2** and they continue to be in the same academic regulations in which they are admitted.

13.Withhold of results:

If the candidate has not paid the dues to the college or if any case of indiscipline/ malpractice is pending against him/her, the result of such candidate shall be withheld and he/she will not be allowed/ promoted into the next higher semester. The issue of degree is liable to be withheld in such cases.

14. Award of letter grades:

- All assessments of a course will be done on absolute marks basis. However, for the purpose of reporting the performance of a candidate, letter grades, each carrying certainnumber of points, will be awarded as per the range of total marks (out of 100) secured by the candidate in each subject as detailed below:

Letter grade	Grade points	Marks range
S	10	90 – 99
A	9	80 – 89
B	8	70 – 79
C	7	60 – 69
D	6	50 – 59
F	0	< 50 (Fail)
ABS	0	---------

- **Grade sheet:**

After results are declared, grade sheets will be issued to the student with the following details:

a. The college in which the candidate has studied
b. The list of courses enrolled during the semester and the grade scored
c. The Grade Point Average (GPA) for the semester and
d. The Cumulative Grade Point Average (CGPA) of all courses enrolled from first semester/ I-year onwards

GPA for a semester is the ratio of the sum of the products of the number of credits for courses acquired and the corresponding points to the sum of the number of credits for the courses acquired in the semester.

$$\text{GPA} = \frac{\text{Sum of [Credits acquired x Grade points]}}{\text{Sum of Credits acquired}}$$

CGPA will be calculated in a similar manner, considering all the courses registered from I-semester. “F”&”ABS”, grades will be excluded for calculating GPA and CGPA.

$$\text{CGPA} = \frac{\sum_{i=1}^{n} C_i GP_i}{\sum_{i=1}^{n} C_i}$$

where Ci– is the credits assigned to the course
GPi– is the point corresponding to the grade obtained for each course

n – is the number of all courses successfully cleared during the particular semester in the case of GPA and during all the semesters in the case of CGPA.

- Whenever students, having arrear subjects, appear for the external semester examination during which there are no regular batch of students writing the same subjects, then, the letter grades for the arrears subjects shall be awarded based on the range of marks approved by the class committee immediately preceding end semester examination in which regular students wrote.

15. **Classification of successful candidates**

- Classification of performance of the students at the end of the course (after completing all the course requirements) will be based on CGPA(Cumulative Grade Point Average) as indicated below**.**

Classification	**CGPA**
First class with distinction	8.0 and above
First Class	6.5 to 7.99
Second Class	5.0 to 6.49

- A minimum of 5.0 CGPA is required for the award of the degree.

16.**Revaluation and Improvement:**

- A candidate can apply for revaluation of his/ her external examination answer paper in a theory course, within two days from the date of declaration of results, on payment of a prescribed fee through proper application to the Controller of Examinations through the Head of the Institution. A candidate can apply for revaluation of answer scripts in not more than **5**subjects at a time**.** The Controller of Examination will arrange for the revaluation and the results will be intimated to the candidate concerned through the Principal.
- **No** revaluation for seminar, comprehensive viva-voce, practical and project work.
- A candidate can be allowed to apply for improvement only in theory subjects in the next supplementary examinations of that semester (not more than one chance per subject).

17. Number of instruction days:

The minimum no. of instruction days including examinations will be 90 per semester.

18. Rules of discipline:

- Any attempt by any student to influence the teachers, examiners, faculty and staff of controller of examination for undue favors in the exams, and bribing them for marks/ attendance will be treated as malpractice cases and the student will be debarred from the college.
- When the student absents himself/ herself, he/she is treated as to have appeared and obtained ZERO marks in that subject(s) and grading is done accordingly.
- When the performance of the student in any subject(s) is cancelled as a punishment for indiscipline, he/shewill be awarded zero marks in that subject(s).
- When the student's answer book is confiscated for any kind of attempted or suspected malpractice the decision of the examiner is final.

19. General:

- The academic regulations should be read as a whole for purpose of any interpretation.
- Malpractices rules- nature and punishments is appended.
- In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Vice-Chairman of the academic council will be final.

- The college may, from time to time, revise, amend or change the regulations, scheme of examinations and syllabi.

20. Disciplinary action for malpractices / improper conduct in examinations:

	Nature of Malpractices/ Improper conduct	**Punishment**
	If the candidate	
1. (a)	possesses or keeps access in examination hall, any paper, note book, programmable calculators, cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory/ practical) in which he/she is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons inside or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he/she will be handed over to the police and a case is registered against him/her.
2.	has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate will be cancelled and retained by the CE.
3.	impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall and forfeits the seat. The performance of the original candidate, who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all university examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he/she will be handed over to the police and a case is registered against him/her.
4.	smuggles in the answer book or additional sheet	Expulsion from the examination hall and

	or takes out or arranges to send out the question paper or answer book or additional sheet, during or after the examination.	cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all university examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6.	refuses to obey the orders of the Chief Superintendent/Assistant-Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall or causes any injury to his person or to any of his relatives whether by offensive words spoken or written or by signs or by visible representation or assaults the officer-in-charge, or any person on duty inside or outside the examination hall or any of his relatives, or indulges in any other act of misconduct or mischief which results in damage to or destruction of property in the examination hall or any part of the college campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates are also debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	leaves the exam hall taking away answer script or intentionally tears off the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all the external examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	possesses any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate

		has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9.	belongs to college, who is not a candidate for the particular examination or any person not connected with the college but indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the college will be expelled from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the college will be handed over to police and, a police case will be registered against them.
10.	comes in a drunken state to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	copying is detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12.	If any malpractice is detected which is not covered in the above clause(1) to (11) shall be reported to the University for further action to award suitable punishment.	

Malpractices identified by squad or special invigilators

- Punishments to the candidates as per the above guidelines.
- Punishment for institutions : (if the squad reports that the college is also involved in encouraging malpractices)
  a. A show cause notice shall be issued to the college.
  b. Impose a suitable fine on the college.
- Shifting the examination centre from the college to another college for a specific period of not less than one year.

Note: All the above regulations will be also applicable for the other M.Tech courses that may be sanctioned to the institution in future.

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SREENIVASA INSTITUTE of TECHNOLOGY and MANAGEMENT STUDIES

CHITTOOR-517 127 (Autonomous)

Department of Electronics and Communicaiton Engineering

Course structure for M.TECH (VLSI System Design)

I Semester

S. No.	Course Code	Subject	Scheme of Instruction Periods per week			Scheme of Examination Maximum Marks		
			L	P	C	I	E	Total
1.	13MVSD 11	VLSI Technology	4	-	4	40	60	100
2.	13MVSD 12	Analog IC Design	4	-	4	40	60	100
3.	13MVSD 13	Digital IC Design	4	-	4	40	60	100
4.	13MVSD 14	Hardware Description Languages	4	-	4	40	60	100
5.	13MVSD 15	Microcontroller & Embedded System Concepts	4	-	4	40	60	100
6.	13MVSD 16A 13MVSD 16B 13MVSD 16C	**Elective I** A)Real Time Operating Sytem B)System Modelling & Simulation C)ASIC Design	4	-	4	40	60	100
7.	13MVSD 17	Digital IC Design Lab	-	3	2	40	60	100
8.	13MVSD 18	Embedded System Lab	-	3	2	40	60	100
Contact periods per week			24	6				
Total periods per week			30					
Total (6 Theory + 2 Labs)					28			
Total Marks						320	480	800

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II Semester

S. No.	Course Code	Subject	Scheme of Instruction Periods per week			Scheme of Examination Maximum Marks		
			L	P	C	I	E	Total
1.	13MVSD 21	Testing & Testability	4	-	4	40	60	100
2.	13MVSD 22	Low Power VLSI Design	4	-	4	40	60	100
3.	13MVSD 23	Algorithms for VLSI Design Automation	4	-	4	40	60	100
4.	13MVSD 24	FPGA Architecture & Applications	4	-	4	40	60	100
5.	13MVSD 25	Scripting Language for VLSI Design Automation	4	-	4	40	60	100
6.	13MVSD 26A 13MVSD 26B 13MVSD 26C	**Elective II** A) Nano Electronics B) Cryptography & Network Security C)Hardware Software Codesign	4	-	4	40	60	100
7.	13MVSD 27	Mixed Signal Lab	-	3	2	40	60	100
8.	13MVSD 28	PERL Scripting Language Lab	-	3	2	40	60	100
Contact periods per week			24	6				
Total periods per week			30					
Total (6 Theory + 2 Labs)					28			
Total Marks						320	480	800

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III Semester

S. No.	Course Code	Subject	Scheme of Instruction Periods per week			Scheme of Examination Maximum Marks		
			L	P	C	I	E	Total
1.	13MVSDS 31	Seminar	-	-	2	100	-	100
2.	13MVSDS 32	Comprehensive Examination	-	-	2	100	-	100
Contact periods per week			-	-				
Total periods per week			-					
Total (Seminar + Comprehensive Examination)					4			
Total Marks						200	-	200

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IV SEMESTER COURSE STRUCTURE

S. No.	Course Code	Subject	Scheme of Instruction Periods per week			Scheme of Examination Maximum Marks		
			L	P	C	I	E	Total
1.	13MVSD 41	Project Work	-	-	12	40	60	100
Contact periods per week			-	-				
Total periods per week			-					
Total (Project)					12			
Total Marks						40	60	100

L -> Lecture C -> Credits T -> Tutorial

I -> Internals P -> Practical E -> External

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I Year M. Tech I semester	**L**	**P**	**C**
	4	**-**	**4**

13MVSD 11 VLSI TECHNOLOGY

UNIT - 1: Fabrication Process & Layout Design and Tools

Introduction to IC circuit technology and IC era - Fabrication process of MOS transistors - Transistor Structures - Wires and Vias - Scalable Design Rules - Layout Design Tools - VLSI Design Flow.

UNIT - 2: Logic Gates & Layouts

Static Complementary Gates - Switch Logic - Alternative Gate Circuits - Low Power Gates - Resistive and Inductive Interconnect Delays.

UNIT - 3: Combinational Logic Networks

Layouts - Simulation - Network delay Interconnect Design - Power Optimization - Switch Logic Networks - Gate and Network Testing.

UNIT - 4: Sequential Systems

Memory Cells and Arrays - Clocking Disciplines - Design - Power Optimization - Design Validation and Testing.

UNIT - 5: Floor Planning & Architecture Design

Floor Planning Methods - Off-Chip Connections - High Level Synthesis - Architecture for Low Power - SOCs and Embedded CPUs - Architecture Testing.

Introduction To Cad Systems (Algorithms) And Chip Design

Layout Synthesis and Analysis - Scheduling and Printing - Hardware-Software Co design - Chip Design Methodologies - A simple Design Example.

Text Books:

1.Essentials of VLSI Circuits and Systems, 2/e, 2005, K. Eshraghian et. al , Prentice Hall of India Ltd., New Delhi.
2.Modern VLSI Design, 5/e, 2005, Wayne Wolf, Pearson Education, New Delhi.

Reference books:

1.Principles of CMOS Design, 2/e, N.H.E Weste, K.Eshraghian, Adison Wesley, New Delhi.
2.Introduction to VLSI Design, 2/e, 1990, Fabricius, McGraw Hill International Edition, New Delhi.
3.CMOS Circuit Design, Layout and Simulation, 2/e, 2004, Baker, Li Boyce, Prentice Hall of India, New Delhi.
4.VLSI Technology, 2/e , 2003, S.M. SZE, Bell Laboratories, Tata McGraw Hill, New Delhi.
5. Introduction to VLSI Circuits and Systems, Student Edition, Reprint 2006, John .P.Uyemura, John Wiley, New Delhi.

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I Year M. Tech I semester	**L**	**P**	**C**
	4	**-**	**4**

13MVSD 12 ANALOG IC DESIGN

UNIT - 1: MOS Transistor

MOS Transistors - Modeling In Linear - Saturation And Cutoff - High Frequency Equivalent Circuit.

UNIT - 2: Integrated Devices and Modeling and Current Mirror

Advanced MOS Modeling - Large Signal and Small Signal Modeling for BJT/Basic Current Mirrors and Single Stage Amplifiers: Simple CMOS Current Mirror - Common Source - Common Gate Amplifier with Current Mirror Active Load - Source Follower with Current Mirror to Supply Bias Current - High Output Impedance Current Mirrors and Bipolar Gain Stages - Frequency Response.

UNIT - 3: Operational Amplifier Design and Compensation

Two Stage CMOS Operational Amplifier - Feedback and Operational Amplifier Compensation - Advanced Current Mirror. Folded – Cascade Operational Amplifier - Current Mirror Operational Amplifier Fully Differential Operational Amplifier - Common Mode Feedback Circuits - Current Feedback Operational Amplifier - Comparator - Charge Injection Error - Latched Comparator and Bi-CMOS Comparators.

UNIT - 4: Sample and Hold Switched Capacitor Circuits

MOS – CMOS - Bi-CMOS Sample and Hold Circuits - Switched Capacitor Circuits - Basic Operation and Analysis - First Order and Biquard Filters - Charge Injection - Switched Capacitor Gain Circuit - Correlated - Double Sampling Techniques - Other Switched Capacitor Circuits.

UNIT - 5: Data Converters and Filters

Ideal D/A & A/D Converters - Quantization Noise - Performance Limitations - Nyquist Rate D/A Converters - Decoders Based Converters. Binary Scaled Converters. Hybrid Converters. Nyquist Rate A/D Converters: Integrating -Successive Approximation - Cyclic Flash Type - Two Step – Interpolating - Folding and Pipelined - A/D Converters - Over Sampling with and Without Noise Shaping - Digital Decimation Filter - High Order Modulators - Band pass over Sampling Converter - Practical Considerations - Continuous Time Filters.

Text Books:

1.Analog Integrated Circuit Design, 2/e, 1997, D.A.John & Ken Martin, John Wiley, New Delhi.
2.Design of Analog CMOS Integrated Circuit, 2/e, 2002, Behzad Razavi Tata Mc GrawHill, Delhi.

Reference Books:

1.CMOS Analog Circuit Design,2/e, 2002, Philip Allen & Douglas Holberg, Oxford University Press.
2.Analog MOS Integrated Circuits, 2/e, 1986, Gregolian, Temes, John Wiley, NewDelhi.
3. Introduction to CMOS OP-AMPs and comparators, 1/e, 1999, Roubic Gregorian, Wiley, Delhi.
4. Bipolar and MOS Analog integrated circuit design, 2/e, 2002, Alen B. Greben, Wiley-Interscience.
5. Analog Integrated Circuit Design, 2/e, 2012, Tony Chan Carusone, David A.Johns, Kenneth Martin, John Wiley & Sons, United States of America.

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13MVSD 13 DIGITAL IC DESIGN

UNIT - 1: Introduction

Issues in Digital IC Design - Quality Metrics of a Digital Design - CMOS inverters -Static and Dynamic Characteristics.

UNIT - 2: CMOS Design

Static and Dynamic CMOS design- Domino and NORA logic - combinational and sequential circuits.

UNIT - 3: Arithmetic Circuits in CMOS VLSI

Adders - Digital Subtractor – Multipliers - Shifter - CMOS Memory Design - SRAM and DRAM

UNIT - 4: Layout Design Rules

Need for Design Rules - Mead Conway Design Rules for the Silicon Gate NMOS Process - CMOS Based Design Rules - Simple Layout Examples - Design Verification.

UNIT - 5: Subsystem Design Process

General arrangement of 4-bit Arithmetic Processor - Design of 4-bit shifter - Design of ALU sub – system - Implementing ALU functions with an adder - Carry-look-ahead adders - Multipliers- Serial Parallel multipliers - Pipeline multiplier array - Modified Booth's algorithm.

Text books:

1.CMOS Digital Integrated Circuits - Analysis & Design, 2/e., 1999, Sung-Mo Kang & Yusuf Leblebici, McGraw Hill, New Delhi.
2. Digital Integrated Circuits - A Design Perspective, 2/e, 1997, Jan M Rabaey Prentice Hall, New Delhi.
3. Introduction to VLSI Design, International Edition, 1990, Eugene D Fabricus,. McGraw Hill New Delhi.

Reference books:

1. Digital Integrated Circuit Design, 2000 , 2/e, Ken Martin, Oxford University Press, New Delhi.
2. Principles of CMOS VLSI Design: A System Perspective, 2/e, 2002, Neil H E West and Kamran Eshranghian, Addision-Wesley New Delhi.
3. CMOS circuit design, layout, and simulation, 2/e, 1998, R. J. Baker, H. W. Li, and D. E. Boyce New York, IEEE Press, New Delhi.
4. Analysis and Design of Digital Integrated Circuits, 3/e, 2004,David A. Hodges, Horace G. Jackson, and Resve A. Saleh McGraw-Hill, New Delhi.
5. Basic VLSI Design, 3/e, 2011, Douglas A. Pucknell, Kamran Eshraghian, Prentice Hall of India, New Delhi.

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13MVSD 14 HARDWARE DESCRIPTION LANGUAGES

UNIT - 1: Verilog HDL Fundamentals

The Verilog Module - Verilog Primitives - Descriptive Styles - Structural Connections - Behavioral Description in Verilog - Hierarchical Descriptions of Hardware - Structured (Top Down) Design Methodology - Arrays of Instances - Using Verilog for Synthesis - Language Conventions - Representation of Numbers.User-Defined Primitives - User Defined Primitives – Combinational Behavior User-Defined Primitives – Sequential Behavior - Initialization of Sequential Primitives. Verilog Variables - Logic Value Set - Data Types - Strings. Constants – Operators - Expressions and Operands - Operator Precedence Models Of Propagation Delay; Built-In Constructs for Delay - Signal Transitions - Verilog Models for Delays.

UNIT - 2: Behavioral Descriptions in Verilog HDL

Verilog Behaviors - Behavioral Statements - Procedural Assignment - Procedural Continuous Assignments - Procedural Timing Controls and Synchronization - Intra-Assignment - Delay- Blocked Assignments - Non-Blocking Assignment - Intra-Assignment Delay - Non-Blocking Assignment - Simulation of Simultaneous Procedural Assignments - Repeated Intra Assignment Delay - Indeterminate Assignments and Ambiguity - Constructs for Activity Flow Control - Tasks and Functions - Summary of Delay Constructs in Verilog - System Tasks for Timing Checks - Variable Scope Revisited - Module Contents - Behavioral Models of Finite State Machines.

UNIT - 3: Verilog Synthesis

HDL - Based Synthesis – Technology -Independent Design - Benefits of Synthesis - Synthesis Methodology - Vendor Support - Styles for Synthesis of Combinational Logic - Technology Mapping and Shared Resources - Three State Buffers - Three State Outputs and Don't Cares - Synthesis of Latches - Synthesis of Edge -Triggered Flip Flops - Registered Combinational Logic - Shift Registers and Counters - Synthesis of Finite State Machines – Resets - Synthesis of Gated Clocks - Design Partitions and Hierarchical Structures. Synthesis of Nets - Synthesis of Register Variables - Synthesis of Expressions and Operators - Synthesis of Resets - Timings Controls in Synthesis - Synthesis of Multi -Cycle Operations - Synthesis of Loops - Synthesis if Fork Join Blocks - Synthesis of The Disable Statement Synthesis of User defined Tasks - Synthesis of User defined Functions - Synthesis of Specify Blocks - Synthesis of Compiler Directives.

UNIT - 4: Switch Level Models in Verilog

MOS Transistor Technology - Switch Level Models of MOS Transistors - Switch Level Models of Static CMOS Circuits - Alternative Loads and Pull Gates - CMOS Transmission Gates. Bidirectional Gates (Switches) - Signal Strengths - Ambiguous Signals - Strength Reduction By Primitives - Combination and Resolution of Signal Strengths - Signal Strengths and Wired Logic. Design Examples in Verilog.

UNIT - 5: Testbenches & Systemverilog Simulation

Basic testbenches - Testbench structure - Constrained random stimulus generation - Object -oriented programming - Assertion -based verification. Event -driven simulation - SystemVerilog simulation Races - Delay models - Simulator tools**.**

SystemVerilog synthesis: RTL synthesis - Non -synthesizable SystemVerilog - Constraints - Attributes - Area and structural constraints Synthesis for FPGAs - Behavioral synthesis - Verifying synthesis results.

Text Books:

1. Modeling, Synthesis, and Rapid Prototyping with the Verilog HDL,2/e, 1999, M.D.CILETTI, Prentice -Hall, Newjersey, USA (Indian Edition).
2. Verilog HDL, 2/e, 2003, Samir Palnitkar, Pearson Education, NewDelhi
3. Digital System Design with SystemVerilog, 1/e, 2010, Mark Zowilski, Pearson Education, NewDelhi
4. Verilog Digital System Design, 2/e, 2006, Zainalabedin Navabi, Tata McGraw Hill, Noida.

Reference Books:

1. A Verilog Primer, 3/e, 2013, J.Bhaskar, BS Publications, Hyderabad.
2. Verilog HDL Synthesis A Practical Primer, 1/e, 2004, J.Bhasker, B.S.Publications, Hyderabad.
3. System Verilog Primer - 2013 - J.Bhasker - B.S.Publications - Hyderabad.
4. Verilog Digital Computer Design, 1999, M.G.ARNOLD, Prentice -Hall (PTR)
5. Fundamentals of Logic Design with Verilog, 2005, Stephen.Brown and Zvonko Vranesic, Tata McGraw Hill, NewDelhi .
6. Digital Design with RTL Design, Verilog and VHDL , 2/e, 2011, Frank Vahid, Wiley & Sons, USA.

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13MVSD 15 MICROCONTROLLERS & EMBEDDED SYSTEM CONCEPTS

UNIT - 1: Overview Of Architecture Of Microcontroller And Embedded Systems

Architecture of a microcontroller– Microcontroller resources – Resources in advanced and next generation microcontrollers – 8051 microcontroller – Internal and External memories – Counters and Timers – Synchronous serial cum asynchronous serial communication – Interrupts
An Embedded System - Processor in The System - Other Hardware Units - Software Embedded into a System - Exemplary Embedded Systems - Embedded System– On – Chip (SOC) and in VLSI Circuit.

UNIT - 2: 8051 Family Microcontrollers Instruction Set

Basic Assembly language programming – Data transfer instructions – Data and Bit -manipulation instructions – Arithmetic instructions – Instructions for Logical operations on the test among the Registers - Internal RAM and SFRs – Program flow control instructions – Interrupt control flow. **Processor Memory Organization:** Memory Selection for an Embedded Systems - Allocation of Memory to Program Cache and Memory Management Links - Segments and Blocks and Memory Map of a System - DMA - Interfacing Processors - Memories and Input Output Devices.

UNIT - 3: Real Time Control & Interrupts

Interrupt handling structure of an MCU – Interrupt Latency and Interrupt deadline – Multiple sources of the interrupts – Non -maskable interrupt sources – Enabling or disabling of the sources – Polling to determine the interrupt source and assignment of the priorities among them – Interrupt structure in Intel 8051.

UNIT - 4: Design Of Digital And Analog Interfacing Methods

Switch - Keypad and Keyboard interfacings – LED and Array of LEDs – Keyboard cum Display controller (8279) – Alphanumeric Devices – Display Systems and its interfaces – Printer interfaces – Programmable instruments interface using IEEE 488 Bus – Interfacing with the Flash Memory – Interfaces – Interfacing to High Power Devices – Analog input interfacing – Analog output interfacing – Optical motor shaft encoders – Industrial control – Industrial process control system – Prototype MCU based Measuring instruments – Robotics and Embedded control – Digital Signal Processing and Digital Filters.

UNIT - 5: Devices and Buses for Device Networks

I/O Devices - Timer and Counting Devices - Serial Communication Using The I^2C - CAN - Profibus Foundation Field Bus and Advanced I/O Buses Between the Network Multiple Devices.

Text Books:

1. Microcontrollers: Architecture, Programming, Interfacing and System Design, 2/e, 2012, Raj Kamal, Pearson Education, NewDelhi

2. The 8051 Microcontroller and Embedded Systems using Assembly and C, 3/e, 2008, Mazidi and Mazidi, Pearson Education, NewDelhi

Reference Books:

1. The 8051 Microcontroller *&* Embedded Systems Using Assembly and *C* with CD, 1/e, 2010, Ayala Kenneth & Dhananjay V. Gadre , CENGAGE Learning.
2. Microprocessors and Microcontrollers Architecture, Programming and System Design, 2/e, 2011, Krishna Kanth, Prentice Hall of India, NewDelhi
3. Embedded System Design: A Unified Hardware/Software Introduction, 2/e, 2007, Frank Vahid/ Tony Givargis, Wiley India, Noida.
4. EmbeddedSystems, 4/e, 2012, Shibu K V, Tata McGraw Hill, NewDelhi
5. An embedded software primer, 2/e, 2004, David Simon , Pearson Education.

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13MVSD16A REAL TIME OPERATING SYSTEMS (Elective I)

UNIT - 1: Real Time Systems -1

Terminology - Systems Concepts - Real time definitions - Events and Determinism - CPU Utilization - Typical Real Time Application - Hard Vs Soft Real Time Systems - a Reference Model of Real Time Systems - Processors and Resources - Temporal Parameters of Real Time Workload.

UNIT - 2: Real Time Systems -2

Periodic Task Model - Precedence Constraints and Data Dependency Functional Parameters - Resource Parameters of Jobs and Parameters of Resources.

UNIT - 3: Real -Time Operating Systems

RealTime Kernels - Pseudokernels - Interrupt Driven Systems - Preemptive -Priority Systems - Hybrid Systems - The Task -Control Block Model - Theoretical Foundations of Real -Time Operating Systems - Effective Release Times and Dead Lines - Offline Vs Online Scheduling - Process Scheduling - Round Robin Scheduling - Cyclic Executives - Fixed -Priority Scheduling– Rate - Monotonic Approach - Dynamic Priority Scheduling - Earliest -Deadline First Approach - Intertask Communication and Synchronization - Buffering Data - Time -Relative Buffering - Ring Buffers - Mailboxes - Queues -Critical Regions - Semaphores - Capabilities of Commercial Real Time Operating Systems.

UNIT - 4: Memory Management

Process Stack Management - Run -Time Ring Buffer - Maximum Stack Size -Multiple -Stack Arrangements - Memory Management in the Task -Control -Block -Model - Swapping - Overlays - Block or Page Management - Replacement Algorithms - Memory Locking -Working Sets - Real - Time Garbage Collection - Contiguous File Systems - Building versus Buying Real -Time Operating - Selecting Real -Time Kernels.

UNIT - 5: Case Studies -Vx Works

Memory Managements Task State Transition Diagram - Pre -Emptive Priority - Scheduling - Context Switches – Semaphore – Binary Mutex - Counting: Watch Dugs - I/O System - Interrupt Management and Synchronization.

Text Books:

1. Real -Time Systems, 1/e, 2000, Jane W. S. Liu, Pearson Education, NewDelhi
2. Real Time Systems Design and Analysis, 3/e, 2004, Phillip A. Lapante, Prentice Hall of India, New Delhi.

Reference Books:

1. Real Time Systems, 3/e, 2010, C.M.Krishna, KANG G. Shin, TataMcGraw.Hill, NewDelhi.
2. Real -Time Systems: Theory and Practice, 1/e, 2007, Rajib Mall, Pearson Education, NewDelhi.
3. Embedded Systems, 4/e, 2012, Shibu K V, Tata McGraw Hill, NewDelhi
4. Operating Systems, Internals and Design Principles, 5/e, 2007, Stallings W, Pearson Education, New Delhi.
5. Simple Real -time Operating System: A Kernel Inside View for a Beginner, 3/e, 2007, Chowdary Venkateswara Penumuchu, Trofford Publishing, USA& Canada.

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13MVSD 16B SYSTEM MODELLING & SIMULATION (Elective I)

UNIT - 1: Basic Concepts & Simulation Software

Basic Simulation Modeling - Systems - Models and Simulation - Discrete Event Simulation - Simulation of Single Server Queuing System - Simulation of Inventory System - Alternative approach to Modeling and Simulation. Comparison of Simulation Packages with Programming Languages - Classification of Software - Desirable Software Features - General Purpose Simulation Packages – Arena - Extend and Others - Object Oriented Simulation - Examples of Application Oriented Simulation Packages.

UNIT - 2: Simulation Models & Time Driven Systems

Guidelines for Determining Levels of Model Detail - Techniques for Increasing Model Validity and Credibility. Modeling Input Signals - Delays - System Integration - Linear Systems - Motion Control Models - Numerical Experimentation.

UNIT - 3: Exogenous Signals And Events

Disturbance Signals - State Machines - Petri Nets & Analysis - System Encapsulation.

UNIT - 4: Markov Process & Event Driven Models

Probabilistic Systems - Discrete Time Markov Processes - Random Walks - Poisson Processes - the Exponential Distribution - Simulating a Poison Process - Continuous -Time Markov Processes. Simulation Diagrams - Queuing Theory - Simulating Queuing Systems - Types of Queues - Multiple Servers.

UNIT - 5: System Optimization

System Identification - Searches - Alpha/Beta Trackers - Multidimensional Optimization - Modeling and Simulation Mythology.

Text books:

1. System Modeling & Simulation, an Introduction, 2/e, 2011, Frank L. Severance, John Wiley & Sons, New -Yark, USA.

Refrence books:

1. Systems Simulation, 1/e, 1978, Geoffery Gordon, Prentice Hall of India, New Delhi.
2. Simulation Modeling and Analysis, 3/e, 2000, McGraw -Hill, Law, A.M. and W.D. Kelton, New York, NY.
3. Discrete Event Simulation: A Practical Approach, 1/e, 1992, Pooch, U.W and J.A. Wall, CRC Press, Boca Raton, FL.
4. Handbook of Simulation: Principles, Methodology, Advances, Applications, and Practice, 1/e, 1998, Banks, J., Ed., John Wiley & Sons, New York.
5. Monte Carlo: Concepts, Algorithms and Applications, 2/e, 1996, Fishman, G.S., Springer -Verlag, New York, NY.

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13MVSD 16C ASIC DESIGN (Elective I)

UNIT - 1: ASIC Design Styles

Introduction – categories - Gate arrays -Standard cells - Cell based ASICs -Mixed mode and analogue ASICs – PLDs.PAL based PLDs: Structures; PAL Characteristics – FPGAs: Introduction - Selected families – Design outline.

UNIT - 2: ASIC Characteristics and Performance

Design styles - Gate arrays - Standard cell - Based ASICs - Mixed mode and Analogue ASICs.

UNIT - 3: ASIC Library Design & I/O Cells

Transistors as resistors - Transistor parasitic capacitance - Logical effort. DC output - AC output - DC input - AC input - Clock input - power input - other I/O cells.

UNIT - 4: ASIC Design Techniques

Overview - Design flow and methodology -Hardware Description Languages - Simulation - Synthesis and Checking - Commercial design tools - FPGA Design tools: XILINX - ALTERA

UNIT - 5: ASIC Construction

Floor planning - Placement and Routing system partition.

Text Books:

1. Integrated circuit engineering, 1/e, 1996, L.J.Herbst, OXFORD SCIENCE Publications.

Reference books:

1. Application Specific Integrated Circuits, 1/e, 1997, M.J.S.Smith, Addison -Wesley Longman.
2. Field Programmable Gate Array, 2/e, 2007, S.Brown, R.Francis, J.Rose, Z.Vransic, BSP, Hyderabad.
3. Digital Design Using Field Programmable Gate Array, 2/e, 1994, P.K.Chan & S. Mourad, Prentice Hall (Pte).
4. Principles of CMOS Design, 2/e, 2004, N.H.E Weste, K.Eshraghian, Adison Wesley, New Delhi.
5. Introduction to VLSI Design 2/e, 1990, Fabricius, McGraw Hill International Edition, New Delhi.

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13MVSD 17 DIGITAL IC DESIGN LAB

Modeling and Functional Simulation of the following digital circuits (with Xilinx/ ModelSim tools) using VHDL/Verilog Hardware Description Languages.

Cycle -I: Combinational Logic

1. Basic Logic Gates, Realization of a four variable function.
2. Arithmetic Units (Adders, Sub tractors).
3. 8 - bit parallel adder using 4 - bit with tasks and functions.
4. Multiplexers, Demultiplexers.
5. Encoders, Decoders, Priority encoder.
6. Four – bit Digital Comparator.
7. Arithmetic Logic Unit with 8 Instructions.
8. Waveform generators
9. 4 -bit Multiplier

Cycle -II: Sequential Logic

1. Latches and Flip – Flops: D -Latch, D -Flip Flop, JK -Flip Flop with synchronous and Asynchronous reset
2. Registers, Ripple Counters, Synchronous Counters,
3. Shift Registers (serial -to -parallel, parallel -to -serial)
4. Cyclic Encoder / Decoder

Cycle -III: Memories And State Machines

1. Read Only Memory (ROM), Random Access Memory (RAM)
2. Mealy State Machine, Moore State Machine: Sequence detector, Sequence Generators
3. Arithmetic Multipliers using FSMs

Cycle -IV: FPGA System Design

1. Demonstration of FPGA and CPLD Boards, Demonstration of Digital design using FPGAs and CPLDs. Implementation of combinational and sequentional circuits in above cycles.
2. Implementation of UART/Mini Processors on FPGA/CPLD

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13MVSD 18 EMBEDDED SYSTEMS LAB

The following experiments are "8051 Microcontroller and Interfacing" with the help of Assembly Language Programming / Embedded C Programming.

Requirements: Keil3.0 software tools, 8051 Microcontroller/Embedded based Kits

Cycle -I:

1. Study of 8051 board and Arithmatic and Logic Programming
2. I/O Programming: Four bit counter using LED
3. Display numbers using seven segment display
4. Sensing Key and Activating Relay
5. Timers/ Counters Programming
6. Write a program to receive and transmit a byte of data using serial interface.

Cycle -II:

1. Interface matrix keyboard with 8051. Write program to display key pressed on seven segment display
2. Interface LCD with the microcontroller. Display your name on the LCD.
3. ADC/DAC and Sensor Interfacing
4. Elevator Interface
5. Traffic light controller Interfacing

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13MVSD 21 TESTING & TESTABILITY

UNIT - 1: Introduction to DFT Fundamentals

Modeling: Modeling Digital Circuits at Logic Level - Register Level and Structural Models - Levels of Modeling. Logic Simulation - Types of Simulation - Delay Models - Element Evaluation - Hazard Detection - Gate Level Event Driven Simulation.

UNIT - 2: Fault Modeling

Logic Fault Models - Fault Detection and Redundancy - Fault Equivalence and Fault Location. Single Stuck and Multiple Stuck – Fault Models. Fault Simulation Applications - General Techniques for Combinational Circuits. Automated Test Pattern Generation (ATPG/ATG) for SSFS in Combinational and Sequential Circuits.

UNIT - 3: Design for Testability

Testability Trade - Offs Techniques. Scan Architectures and Testing – Controllability and Observability - Generic Boundary Scan - Full Integrated Scan - Storage Cells for Scan Design.

UNIT - 4: Built-In Self-Test (BIST)

BIST Concepts and Test Pattern Generation. Specific BIST Architectures – CSBL – BEST – LOCST – STUMPS – CBIST – CEBS – RTD – SST – CSTP - BILBO.

UNIT - 5: Brief Ideas on Embedded Core Testing

Functional Testing with Specific Fault Models. Vector Simulation – ATPG Vectors – Formats - Compaction and Compression - Selecting ATPG Tool. Introduction to Automatic in Circuit Testing (ICT) - JTAG Testing Features.

Text Books:

1.Digital Systems Testing and Testable Design, 2/e, 2001, Miron Abramovici- Melvin A. Breur-Arthur D.Friedman, Jaico Publishing House
2.Essentials Of Electronic Testing, 2/e, 2002, Michael L.Bushnell,D.Agarwal, Kluwer Academic publishers, London

Reference Books:

1.Design for Test for Digital ICs & Embedded Core Systems, 1/e, 1999, Alfred Crouch, Prentice Hall, New Delhi
2.Introduction to VLSI Testing, 1/e, 1998,Robert J.Feugate, Jr.Steven M.Mentyn, Prentice Hall, Englehood Cliffs
3. Digital System Test And Testable Design, 2/e, 2010, Z.Navabi, Springer Publications, London
4.An Introduction to logic circuit testing,2009/e,Parag K.Lala,Morgan &claypod Publishers,Texarkana
5.Testing of Digital Systems, 3/e, 2003, N.K. Jha, S. Gupta Published by Cambridge University, UK

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13MVSD22 LOW POWER VLSI DESIGN

UNIT-1: Low Power Design Over View & BICMOS Processes

Introduction to low voltage & low power design – Limitations - BiCMOS processes - Integration and Isolation considerations - Integrated Analog/Digital CMOS Process.

UNIT-2: Low-Voltage/Low Power CMOS/ BICMOS Processes

Deep submicron processes - SOI CMOS - lateral BJT on SOI - future trends and directions of CMOS/Bi-CMOS processes & Introduction to MOSFET models

UNIT-3: CMOS and Bi-CMOS Logic Gates

Conventional CMOS and Bi-CMOS logic gates – Low voltage low power logic circuits - Comparison of advanced Bi-CMOS Digital circuits. ESD free Bi-CMOS - Digital circuit operation and comparative Evaluation.

UNIT-4: Low Power Latches and Flip Flops

Evolution of Latches and Flip flops - Quality measures for latches and Flip flops - Design perspective.

UNIT-5: Special Techniques

Power Reduction in Clock Networks - CMOS Floating Node - Low Power Bus - Delay Balancing - Low Power Techniques for SRAM.

Text Books:

1. CMOS/BiCMOS ULSI low voltage low power, 1/e, 2002, Yeo Rofail, Gohl, Pearson Education, NewDelhi.
2. Practical Low Power Digital VLSI Design,1/e, 2002, Gary K. Yeap, KAP, NewDelhi

Reference Books:

1. Basic VLSI Design, 3/e, Douglas A.Pucknell & Kamran Eshraghian, Prentice Hall of india, NewDelhi.
2. Digital Integrated circuits, 1/e, 1996, J.Rabaey, Prentice Hall of india, NewDelhi.
3. CMOS Digital ICs, 3/e, 2003, Sung-mo Kang and yusuf leblebici, Tata McGraw-Hill,New Delhi.
4. Dynamic Power Management Design Techniques and CAD Tools, 1/e, 1998, L. Benini and G. De Micheli, Springer, Boston.
5. Low-Power Electronics Design, 1/e, 2005, C. Piguet, CRC Press, Florida.

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13MVSD23 ALGORITHMS FOR VLSI DESIGN AUTOMATION

UNIT-1: Preliminaries

Introduction to Design Methodologies- Design Automation tools- Algorithmic Graph Theory- VLSI Design cycle- physical design cycle- design styles.
General Purpose Methods for Combinational Optimization: Backtracking- Branch and Bound- Dynamic Programming- Integer Linear Programming- Local Search- Genetic Algorithms.

UNIT-2: Layout, Modelling and Simulation

Layout Compaction – Placement - Floor planning and Routing Problems - Concepts and Algorithms. Gate Level Modeling and Simulation- Switch level Modeling and Simulation.

UNIT-3: Logic Synthesis And Verification

Basic issues and Terminology – Binary decision diagrams - Two-Level logic Synthesis

UNIT-4: Physical Design Automation of FPGA's

FPGA technologies - Physical Design cycle for FPGA's - partitioning and Routing for segmented and staggered Models.

UNIT-5: Physical Design Automation of MCM's

MCM technologies - MCM physical design cycle - Partitioning - Placement - Chip Array based and Full Custom Approaches – Routing - Maze routing - Multiple stage routing - Topologic routing - Integrated Pin distribution and routing - Routing and Programmable MCM's.

Text Books:

1. Algorithms for VLSI Design Automation, Student Edition, 1999, S.H.Gerez, John wiley & Sons (Asia) Pvt. Ltd.
2. Algorithms for VLSI Physical Design Automation, 3/e, 1999,Naveed Sherwani, Springer International Edition.

Reference Books:

1.VLSI Physical Design Automation. Theory and practice, 2/e, 1995, S. Sait, H. Youssef, McGrawHill, New Delhi.
2. An Introduction to VLSI Physical Design, 2/e, 1996, M. Sarrafzadeh, C. K. Wong, McGraw-Hill, New Delhi.
3. Synthesis and Optimization of Digital Circuit ,3/e, 2003, G. De Micheli, Tata McGraw Hill Edition.
4. Logic Synthesis and Verification Algorithms, 2/e, 1996, G. Hachtel, F. Somenzi, Kluwer Academic Publishers.
5.Computer Aided Logical Design with Emphasis on VLSI, 4/e, 2004, Frederick J. *Hill*, Gerald R. *Peterson*,ISBN publishers.

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13MVSD 24 FPGA ARCHITECTURE & APPLICATIONS

UNIT - 1: Programmable Logic

ROM – PLA – PAL – PLD – PGA – Features – SPLD – CPLD - FPGA Programming and Applications using Complex Programmable Logic Devices Altera Series – Max 5000/7000 Series and Altera FLEX Logic – 10000 Series CPLD- AMD's – CPLD (Mach 1 To 5)- Cypres FLASH 370 Device Technology- Lattice Plsi's Architectures – 3000 Series – Speed Performance and in System Programmability.

UNIT - 2: Basics of FPGA

Field Programmable Gate Arrays – Logic Blocks- Routing Architecture - Design Flow - Technology Mapping for FPGAs - Implementing Functions using Shannon's Decomposition - Design example for combinational circuit and sequential circuit using FPGA - Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs - AT&T – ORCA's (Optimized Reconfigurable Cell Array) - ACTEL's – ACT - 1-2-3 and Their Speed Performance - FPGA Capacity - Maximum Gates versus Usable Gates

UNIT - 3: Finite State Machines (FSM)

Top Down Design - State Transition Table - State Assignments for FPGAs - Problem of Initial State Assignment for one hot Encoding. Derivations of State Machine Charges - Charts with a PAL - Alternative Realization for State Machine Chart using Microprogramming - Linked State Machines. One hot State Machine - Petrinetes for State Machines – Basic Concepts - Properties. Extended Petrinetes for Parallel Controllers - Finite State Machine - Case Study - Meta Stability - Synchronization and Debouncing.

UNIT - 4: FSM Architectures and Systems Level Design

Architectures Centered Around Non-Registered PLDs - State Machine Designs Centered Around Shift Registers – One hot Design Method - Use of ASMs in one hot Design- Application of one hot Method.

UNIT - 5: Digital Front end Digital Design Tools for FPGA'S & ASIC'S

Using Mentor Graphics EDA Tool (FPGA Advantage) - Design Flow using FPGAs - Guidelines - Cost of Programmability.

Text Books:

1. Field Programmable Gate Array Technology, 2/e, 2009, S.Trimberger, Springer, NewDelhi
2. Field Programmable Gate Arrays, 2/e, 2008, John V. Old Field, Richard C. Dorf, Wiley India, NewDelhi

Reference Books:

1. Field Programmable Gate Array, 3/e, 2007, S.Brown, R.Francis, J.Rose, Z.Vransic, BSP, Hyderabad.
2. Digital Design Using Field Programmable Gate Array, 2/e, 1994, P.K.Chan & S. Mourad, Prentice Hall (Pte).
3. Digital System Design using Programmable Logic Devices,2/e, 2003, Parag.K.Lala, BSPublications, Hyderabad.
4. Digital Systems Design with FPGA's and CPLDs, 2/e, 2009, Ian Grout, Elsevier.
5. FPGA Based system Design, 2/e, 2004, Wayne Wolf, Pearson Education, New Delhi.

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I Year M.Tech II semester	**L**	**P**	**C**
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13MVSD25 SCRIPTING LANGUAGE FOR VLSI DESIGN AUTOMATION

UNIT – 1: Introduction

Overview of Scripting Languages:PERL-CGI-VBScript-Java Script.

UNIT - 2: PERL

PERL Inroduction: Perl overview - Unary and binary operators – Statements : Simple - Compound-If-unless-given- Loop statements and goto. Concept of Pattern Matching - Perl Data Structures - Modules overview - Concept of Objects in Perl-Tied Variables:scalars -arrays-hashes- File handlers.

UNIT - 3: Inter Process Communication

Signals – Files – Pipes - SystemV IPC - Sockets. Concept of Perl Compilation: Lifecycle of Perl program - Compiling your code - Executing your code - Complier back ends - Code generation and tools. Line Interfacing: Command processing-Environment variables.

UNIT – 4: PERL Debugger

Using the Debugger - Debugger Commands - Debugger Customization - Unattended Execution - Internal & Externals Portable Functions. Extensive Exercises for Programming in PERL .

UNIT – 5:

Other Languages: Broad Details of CGI-VB Script-Java Script with Programming Examples.

Text Books:

1.Programming PERL, 3/e, 2000, Larry Wall, Tom Christiansen, John Orwant, Oreilly Publications.
2.Learning PERL,3/e, 2000,Randal L, Schwartz Tom Phoenix, Oreilly Publications.
3.The World of Scripting Languages, 2000, David Barron,Wiley Publications, New Delhi.

Reference Books:

1.Perl for Dummies, 4/e, 2011, Paul Hoffman, Wiley Publishers, New Delhi.
2.PERL Cookbook, 3/e, 2000,Tom Christiansen, Nathan Torkington,Oreilly Publications.
3.Perl by Example, 4/e, 2009,E.Quigley, Pearson Education, New Delhi.

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13MVSD 26A NANO ELECTRONICS (Elective II)

UNIT - 1: Introduction to Nanoelectronics

Limitations of the conventional MOSFETs at Nanoscales - Introductory concepts of Ballistic transport and Quantum confinement - Differences in Few Electron Devices (as analog version) and Single Electron Devices (as digital version) of Nanoelectronic devices. Current Nanoelectronic Devices.
Conventional MOS-FET- Gate Leakage due to Gate oxide - High K dielectrics and improvements in performance. Scaling effect - Quantum Effects in MOSFETs - Strained Silicon - Fully Depleted SOI – MOSFET - Double Gate MOSFET- Multi-gate MOSFETs- FIN-FET- Electrically Induced Junctions for EJ-MOSFETs- Ballistic Transport- Conductance Quantization- Quantum Point Contact Devices- New inter-connect strategies.

UNIT – 2: Nanostructures and Quantum Devices

Low dimensional structures: Quantum wells - Quantum wires - Quantum dots; Density of states in lowdimensional structures; Resonant tunneling phenomena and applications in diodes and transistors
Introduction to Single Electronics Principle of the Single - Electron Transistor - The Coulomb Blockade Phenomenon- Theoretical Quantum Dot Transistor: Energy of Quantum Dot system - Single Electron Quantum - Dot Transistor - Single-Hole Quantum -Dot Transistor - Single-Electron Transistor - Coulomb Blockade Devices - Conductance Oscillation and Potential Fluctuation - Transport under Finite temperature and Finite Bias - Single-Electron Effect - Modeling of Transport: Tunneling- Quantum kinetic Equation.

UNIT – 3: Logic Devices

Silicon MOSFETS - Novel Materials and Alternative Concepts - Ferro Electric Filed Effect Transistors - Super Conductor Digital Electronics - Carbon Nano Tubes for Data Processing.

UNIT – 4: Quantum Electronics

Upcoming Electronic Devices (QED) - Electrons in Mesoscopic structures - Examples of Quantum Electronic Devices: Quantum Interference Devices - SQUIDs - Split - Gate Transistor - Electron - Wave Transistor - Electron - Spin Transistor - Resonant Tunnelling Devices - Quantum Oscillators - Quantum Cellular Automata (QCA) - Quantum - dot Array- Introduction Quantum Computing.
Carbon Nantubes and CNT Based devices Carbon Nanotube theory: structure and phonon dispersion relations - nomenclature- acoustic and optical phonons - Nanotube theory: electronic structure- optical properties . Electronic structure of grapheme - SW and MWCNTs- 1D quantization in nanotubes- van Hove singularities - CNT-FET- CNT-TUBFET- CNT-SET- CNT memories- CNT based switches- Logic Gates- CNT based RF devices- CNT based RTDs.

UNIT – 5: Molecular Electronics

Overview - Characterization of switches and complex molecular devices - polyphenylene based Molecular rectifying diode switches. Polymer Electronics - Self-Assembling Circuits - Optical Molecular Memories Technologies - Quantum Mechanical Tunnel Devices – Quantum Dots & Quantum Wires. Spintronics: Introduction to Spintronics. Principles and concepts - Spintronic devices and applications - Spin filters- Spin diodes- Spin transistors.

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Text Books:

1.Silicon Nanoelectronics, 2/e, 2006, Shunri Oda, David Ferry, CRC Press, Taylor & Francis Group. New Delhi.
2.Nanotubes and nanowires, 3/e, 2005, C.N.R. Rao and A. Govindaraj RSC Publishing. New Delhi.

Reference Books:

1.Nanoelectronics and Nanosystems, 2/e, 2005, K. Goser, P. Glosekotter, Springer. New Delhi.
2.Nanoelectronics and Nanosystems – From transistors to Molecular and Quantum Devices , 2/e, 2004, Karl Goser, Peter Glosekotter, Jan Dienstuhl , Springer-Verlag . New Delhi.
3.Spin Electronics , 3/e, 2001, M. Ziese and M. J. Thornton (Eds.), Springer-Verlag New Delhi.
4.Introduction to Nano Technology, 2/e, May 2003, Charles Poole, Wiley Interscience,New Delhi.
5. Nano Electronics and Information Technology, 2/e, 2003, Rainer Waser, Wiley VCH, New Delhi.

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I Year M.Tech II semester	**L**	**P**	**C**
	4	**-**	**3**

13MVSD 26B CRYPTOGRAPHY & NETWORK SECURITY (Elective II)

UNIT-1: Symmetric Ciphers & Public-Key Encryption

Overview – classical Encryption Techniques - Block Ciphers and the Data Encryption standard - Introduction to Finite Fields - Advanced Encryption standard - Contemporary Symmetric Ciphers - Confidentiality using Symmetric Encryption. Introduction to Number Theory - Public-Key Cryptography and RSA - Key Management - Diffie-Hellman Key Exchange - Elliptic Curve Cryptography - Message Authentication and Hash Functions - Hash Algorithms - Digital Signatures and Authentication Protocols.

UNIT-2: Network Security Practice

Authentication Applications – Kerbors - X.509 Authentication Service - Electronic mail Security - Pretty Good Privacy - S/MIME - IP Security architecture - Authentication Header - Encapsulating Security Payload - Key Management.

UNIT-3: System & Wireless Security

Intruders - Intrusion Detection - Password Management - Malicious Software – Firewalls - Firewall Design Principles - Trusted Systems. Introduction to Wireless LAN Security Standards - Wireless LAN Security Factors and Issues.

UNIT-4: Designing Secure Networking & Threats

Attack Process - Attacker Types. Vulnerability Types - Attack Results - Attack Taxonomy - Threats to Security - Physical security - Biometric systems - Monitoring controls - Data security- Intrusion-detection systems. Components of a Hardening Strategy - Network Devices - Host Operating Systems – Applications - Based Network Services - Rogue Device Detection - Network Security Technologies - the Difficulties of Secure Networking - Security Technologies - Emerging Security Technologies General Design Considerations - Layer 2 Security Considerations - IP Addressing Design Considerations - ICMP Design Considerations - Routing Considerations - Transport Protocol Design Considerations.

UNIT-5: Encryption Techniques

Conventional techniques - Modern techniques - DES- DES chaining - Triple DES - RSA algorithm - Key management - Message Authentication - Hash Algorithm - Authentication requirements - functions secure Hash Algorithm - Message digest algorithm - Digital signatures - AES Algorithms.

Text Books:

1.Cryptography and Network Security - Principles And Practices, 3/e, 2003, William Stallings, Pearson Education,New Delhi.
2. Network Security Architectures, 1/e, 2004, Sean Convery, Published by Cisco Press.

Reference Books:

1. Cryptography and Network Security, 2/e, 2003, Atul Kahate, Tata McGraw Hill,New Delhi.
2. Applied Cryptography, 1/e, 2001, Bruce Schneier, John Wiley and Sons Inc.
3. Wi-Fi Security, 2/e, 2003, Stewart S. Miller, McGraw Hill,New Delhi.
4. Security In Computing, 3/e, 2003, Charles B. Pfleeger, Shari Lawrence Pfleeger, Pearson Education, New Delhi
5.Inside Internet Security,1/e, 2005, Jeff Crume, Addison Wesley.

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13MVSD 26C HARDWARE SOFTWARE CO- DESIGN (Elective II)

UNIT - 1: Co- Design Issues

Co- Design Models – Architectures – Languages - a Generic Co-design Methodology.

UNIT - 2: Algorithms, Prototyping & Emulation

Hardware software synthesis algorithms - hardware/software partitioning distributed system co-synthesis - Prototyping and emulation techniques - Prototyping and emulation environments- Future developments in emulation and prototyping architecture specialization techniques - System communication infrastructure.

UNIT - 3: Target Architectures

Architecture Specialization techniques - System Communication infrastructure - Target Architecture and Application System classes - Architecture for control dominated systems (8051-Architectures for High performance control) - Architecture for Data dominated systems (ADSP21060- TMS320C60) - Mixed Systems.

UNIT - 4: Architectures, Specification and Verification

Modern embedded architectures - Embedded software development needs- Compilation technologies practical consideration in a compiler development environment - Design- co-design- the co-design computational model - concurrency coordinating concurrent computations - interfacing components - design verification- implementation verification- verification tools- and interface verification.

UNIT - 5: Languages For System Level Specification And Design

System level specification - Design representation for system level synthesis - System level specification languages. Heterogeneous specifications and multi language co-simulation the cosyma system and lycos system.

Text Books:

1. Hardware / software co- design Principles and Practice, 2/e, 2009, Jorgen Staunstrup, Wayne Wolf, Springer, New Delhi.
2. Hardware / software co- design Principles and Practice,2/e, 2002, kluwer academic publishers, Netherlands.

Reference Books:

1. Specification and Design of Embedded Systems, 1/e, 2007, Daniel D. Gajaski, Frank Vahid, Sanjiv Narayan, Jie Gong, Pearson Education, New Delhi.
2. Hardware/Software Co-Design, 1/e, 2002, Giovanni De Micheli, Ern st, Wolf, Morgan Kaufmann (Academic Press), San Diego, United States of America.

3. A Practical Introduction to Hardware/Software Codesign, 2/e, 2012, Patrick Schaumont, Springer, New Yark, London.
4. Hardware/software co-design and co-verification, 1/e, 1997, Jean-Michel Bergé, Kluwer Academic Publishers, United States of America.
5. System Level Hardware/Software Co-Design: An Industrial Approach, 1/e, 1997, Joris van den Hurk, Jochen A.G. Jess, Kluwer Academic Publishers, Boston.

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	-	**4**	**2**

13MVSD 27 MIXED SIGNAL LAB

1. Analog Circuits Simulation using Spice.
2. Mixed Signal Simulation Using Mixed Signal Simulators.
3. Layout Extraction for Analog & Mixed Signal Circuits.
4. Parasitic Values Estimation from Layout.
5. Layout Vs Schematic.
6. Net List Extraction.
7. Design Rule Checks.

NOTE: Required Software Tools:

1**.** Mentor Graphic tools / Cadance tools/ Synophysis tools. (220 nm Technology and Above)
2. Xilinx 9.1i and Above for FPGA/CPLDS.

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13MVSD 28 PERL SCRIPTING LAB

Cycle 1:

1. Write an HTML document that contains a VB script that will retrieve quantity and unit price from a webpage. When "Calculate Cost" button is pressed, it calculates & displays total amount for the order.
2. Develop a Java Script that reads a five digit integer and determines whether it is a palindrome or not. If the number is not five digits, it should output the HTML text that displays an alert dialog indicating the user to enter a new value.

Cycle 2:

1. Develop a Perl Program to printing the text on the screen.
2. Develop a perl program using different operators.
3. Develop a perl program to demonstrate the pattern matching features of perl.

Cycle 3:

1. Develop a Perl Program to demonstate the use of scalars, arrays and hashes.
2. Develop a Perl Program to find the given number is prime, even and odd.
3. Develop a perl program to demonstate the usage of Signals.
4. Develop a perl program to demonstate the usage of Files.

Cycle 4:

1. Develop a perl program to demonstate the usage of Pipes.
2. Develop a perl program to demonstate the usage of SystemV IPC.
3. Develop a perl program to demonstate the usage of Sockets for Network communication.

NOTE: Required Software Tools:

1. UNIX OS.
2. Windows os and perl software.

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13MVSD 31 SEMINAR

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M. Tech III - Semester (VLSI System Design)	**L**	**P**	**C**
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13MVSD 32 COMPREHENSIVE EXAMINATION

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M. Tech IV - Semester (VLSI System Design)	**L**	**P**	**C**
	-	**-**	**12**

13MVSD 41 PROJECT WORK