HONOURS

S.No	Course Code	Course Title	Scheme of Instructions Hours per Week				Scheme of Examination Maximum Marks		
			L	T	P	C	I	E	Total
1	23HRECE1	Analog IC Design	3	-	-	3	30	70	100
2	23HRECE2	Digital IC Design	3	-	-	3	30	70	100
3	23HRECE3	Low Power VLSI	3	-	-	3	30	70	100
4	23HRECE4	Testing and Verification	3	-	-	3	30	70	100
5	23HRECE5	FPGA Architectures	3	-	-	3	30	70	100
6	23HRECE6	Analog and Digital IC Design Lab	-	-	3	1.5	30	70	100
7	23HRECE7	Physical Design Automation Lab	-	-	3	1.5	30	70	100

23HRECE1	**ANALOG IC DESIGN** **Honors with VLSI specialization**	**L**	**T**	**P**	**C**
		3	0	0	3

Course Objectives:

1. To explore MOSFET characteristics, biasing techniques and current mirrors for analog circuit design.
2. To design and analyze single-stage amplifiersand their performance with feedback and cascode configurations.
3. To analyze the designand performance of differential amplifiers in analog circuits.
4. To examine the characteristics and compensation techniquesof operational amplifiers.
5. To understand the design principles of bandgap reference circuits.

Course Outcomes:
At the end of this course, the students will be able to

1. Understand the MOSFET characteristics, biasing techniques and current mirrors for analog circuit design.
2. Design and analyze single-stage amplifiersand their performance with feedback and cascode configurations.
3. Analyze the designand performance of differential amplifiers in analog circuits.
4. Learn the characteristics and compensation techniquesof operational amplifiers.
5. Understand the design principles of bandgap reference circuits.

UNIT-I

Review of MOSFET device characteristics: Second order effects, MOSsmallsignalModel, Capacitances, body bias effect, Current biasing, voltage biasing, Technology biasing, Relative comparison and limitations.

Basic building blocks and basic cells-Switches, active resistors, Current sources and sinks, Current mirrors: Basic current mirror, cascode current mirror, low voltage current mirror, Wilson and Widlar current mirrors, voltage and current references, Mismatch in accuracies, Design solutions to minimize mismatch in accuracies.

UNIT-II

Singlestageamplifier: Analyticaljustificationofoperatingregionsuitableforamplification/switching ,Design of CS amplifier with different loads, Limitations of diode connected load, Improving output impedance of CS amplifier through feedback ,small signal analyses of common gate and common drain topologies and their frequencyresponsewithparasiticaffects,significanceofcascode,design ofcascodeamplifierandwithideal current source load and practical cascode load, Limitations of cascode, folded cascode amplifier and design with parasitics.

UNIT-III

Differential amplifier: Significance of differential signaling, Limitations of quasi differential amplifier, Design of differential amplifier with current source load and diode connected load and small signal analyses, errors due to mismatch, replication principle, qualitative analysis, common mode response, gilbert cell, Common centroid layout.

UNIT-IV

Operationa lamplifier: characterization, two stage O Pamp, small signal analysis, Miller compensation, effect of RHP zero on stability, Lead compensation, constant gmbiasing, design of biasing circuit independent of process and temperature variations.

UNIT-V

Band Gap Reference: General considerations, Supply independent biasing, temperature-independent references, negative-TC voltage, positive TC voltage, Bandgap reference, PTAT generation, curvature correction, Design of BGR under low voltage conditions.

TEXT BOOKS:

1. BehzadRazavi,DesignofAnalogCMOSIntegratedCircuit,McGrawHillEducation,2017,2nd Edition.
2. Paul J. Hurst, Paul R. Gray, Robert G Meyer and Stephen H. Lewis, Analysis and Design of Analog Integrated Circuits, Wiley, 2024, 6thEdition.
3. MohammedIsmailandTerriFiez,AnalogVLSI:SignalandInformationProcessing,M cGrawHill, 1994.

REFERENCE BOOKS:

1. RandallL.Geiger,PhillipE.AllenandNoelR.Strader,VLSIDesignTechniquesforAna logandDigital Circuits, Tata McGraw-Hill Education, 1989.
2. DavidJohns,TonyChanCarusoneandKennethMartin,AnalogIntegratedCircuit Design,Wiley, 2011, 2ndEdition.
3. Paul G. A. Jespers and Boris Murmann, Systematic Design of Analog CMOS Circuits,CambridgeUniversity Press, 2017.

		L	T	P	C
23HRECE2	**DIGITAL IC DESIGN** **Honors with VLSI specialization**	3	0	0	3

Course Objectives:

1. To understand MOSFET and CMOS inverter operation along with constraints.
2. To explore CMOS design techniques for combinational and sequential logic circuits.
3. To gain knowledge on the timing issues in digital circuits.
4. To design and analyze various arithmetic building blocks.
5. To learn about the design and functionality of semiconductor memories.

Course Outcomes:
At the end of this course, the students will be able to

1. To understand MOSFET and CMOS inverter operation along with constraints.
2. To explore CMOS design techniques for combinational and sequential logic circuits.
3. To gain knowledge on the timing issues in digital circuits.
4. To design and analyze various arithmetic building blocks.
5. To learn about the design and functionality of semiconductor memories.

UNIT-I

MOS Inverters: Structure and Operation of MOS Transistor (MOSFET), MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effect, MOSFET Capacitances, CMOS Inverter- Static and switching characteristics, Delay-Time Definitions, Calculation of Delay Times, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitic, Power Consumption in CMOS Gates.

UNIT-II

Designing Combinational & Sequential Logic Gates in CMOS: Static CMOS design- ratioed logic, pass transistor logic, transmission gate logic, Dynamic CMOS Design, Static Latches and Registers, Dynamic Latches and Registers, Alternative Register Styles, Nonbistable Sequential Circuits, Logic Style for Pipelined Structures.

UNIT-III

Timing Issues in Digital Circuits: Introduction, Synchronous Timing basics, Clock Skew and Jitter, Clock distribution techniques, Clock Generation and Synchronization.

UNIT-IV

DesigningArithmeticBuildingBlocks: Introduction,TheAdder:CircuitandLogicDesign,Multipliers:Shifters, Power Considerations in Datapath Structures.

UNIT-V

Designing Memory: Introduction, Semiconductor Memories - An Introduction, The Memory Core: RAM, ROM, Memory Peripheral Circuitry.

TEXT BOOKS:

1. JanM.Rabaey,AnanthaChandrakasanandBorivojeNikolic,DigitalIntegratedCircuits: ADesign Perspective, Pearson, 2003, 2nd Edition.
2. JohnP.Uyemura,CMOSLogicCircuitDesign,Springer,2001.
3. JohnP.Uyemura,IntroductiontoVLSICircuitsandSystems,Wiley,2002.

REFERENCE BOOKS:

1. Sung-MoKangandYusufLeblebici,CMOSDigitalIntegratedCircuits,McGraw-Hill, 2003,3rdEdition.
2. CharlesHawkins,JaumeSeguraandPaymanZarkesh-Ha,CMOSIntegratedDigitalElectronics:AFirst Course, IET, 2012

23HRECE3	**LOW POWER VLSI** **Honors with VLSI specialization**	**L**	**T**	**P**	**C**
		3	0	0	3

Course Objectives:

1. To explore low-power CMOS VLSI design techniques for minimizing power dissipation.
2. To understand CMOS adder architecturesand low-power design techniques.
3. To analyze various multiplier architectures and low-power design techniques for memories.
4. To examine architectural techniques for minimizing power dissipation in digital systems.
5. To apply low-power design techniques for optimizing power consumption in digital circuits.

Course Outcomes:
At the end of this course, the students will be able to

1. Explore low-power CMOS VLSI design techniques for minimizing power dissipation.
2. Understand CMOS adder architecturesand low-power design techniques.
3. Analyze various multiplier architectures and low-power design techniques for memories.
4. Examine architectural techniques for minimizing power dissipation in digital systems.
5. Apply low-power design techniques for optimizing power consumption in digital circuits.

UNIT 1

Low Power CMOS VLSI design: Introduction: Sources of Power Dissipation, Static Power Dissipation, Active Power Dissipation.

Circuit Techniques for Low Power Design:Design for Low Power, Multiple Vth techniques, Dynamic Vth techniques.

UNIT II

Adders: Standard Adder Cells, Review of CMOS Adders Architectures and performance Comparison, Low Voltage Low Power Design Techniques, Current Mode Adders.

UNIT III

Multipliers and Memories: Review of Multiplier Architectures, Braun, Booth and Wallace Tree Multipliers and their performance comparison. Sources of power dissipation in SRAMs, Low power SRAM circuit techniques, Sources of power dissipation in DRAMs, Low power DRAM circuit techniques.

UNIT IV

Architectural Techniques for Low Power: Parameters effecting power dissipation, Variable frequency, Dynamic voltage Scaling, Dynamic Voltage and Frequency Scaling, Reduced VDD, Architectural clock gating, Power gating, Multi-voltage, Optimizing memory power.

UNIT V

Low Power Implementation Techniques: Library Selection, Clock Gating, Timing Impact due to Clock gating, Gate-level power optimization techniques, Power Optimization for Sleep Mode.

Textbooks:

1. KiatSengYeoandKaushik Roy,Low-Voltage,Low-PowerVLSISubsystems, TataMcGrawHill, 2009.
2. SoudrisD,PiguetCandGoutisC,DesigningCMOSCircuitsforLowPower,KluwerAcademic Publishers, 2002.

References:

1. AbdellatifBellaouar,MohamedElmasry,Low-PowerDigitalVLSIDesign:CircuitsandSystems, Springer, 2012.
2. JanRabaey,LowPowerDesignEssentials,Springer,2009.

		L	T	P	C
23HRECE4	**TESTING AND VERIFICATION** **Honors with VLSI specialization**	3	0	0	3

Course Objectives:

1. To analyze VLSI testing concepts, fault modeling, and defect analysis for ensuring chip reliability.
2. To explore fault simulation techniques and algorithms for efficient fault detection in digital circuits.
3. To examine test generation techniques for combinational and sequential circuits, fault modeling, and scan chain-based testing.
4. To study and apply test generation algorithms for digital circuits and understand design-for-testability techniques.
5. To apply Design for Testability (DFT) techniques, including BIST architectures and test algorithms for embedded memory.

Course Outcomes:
At the end of this course, the students will be able to

1. Identify faults, model defects, and analyze testing methods for improving VLSI chip quality and yield.
2. Utilize serial, parallel, and deductive fault simulation algorithms for testing and diagnosing faults in digital systems.
3. Implement ATPG and path sensitization methods for fault detection in combinational and sequential circuits and implement scan chain-based testing.
4. Apply D, FAN, and PODEM algorithms for fault detection and implement design-for-testability techniques in digital circuits.
5. Adopt DFT methodologies to enhance testability, generate test patterns, and implement BIST for efficient fault detection in digital systems.

UNIT 1

RoleoftestinginVLSIDesignflow,Testingatdifferentlevelsofabstraction,Fault,error,defect,diagnosis, yield, Types of testing, Rule of Ten, Defects in VLSI chip. Modelling basic concepts, Functional modelling at logic level and register level, structure models, logic simulation, delay models. Various types of faults, Fault equivalence and Fault dominance in combinational sequential circuits.

UNIT II

Fault simulation applications, General fault simulation algorithms- Serial, and parallel, Deductive fault simulation algorithms.

UNIT III

Combinational circuit test generation, Structural Vs Functional test, ATPG, Path sensitization methods. Difference between combinational and sequential circuit testing, five and eight valued algebra, and Scan chain-based testing method.

UNIT IV

D-algorithm procedure, Problems, PODEM Algorithm. Problems on PODEM Algorithm. FAN Algorithm. Problems on FAN algorithm, Comparison of D, FAN and PODEM Algorithms. Design for Testability, Ad- hoc design, Generic scan-based design.

UNIT V

Classical scan-based design, System level DFT approaches Test pattern generation for BIST, Circular BIST.BISTArchitectures.Testablememorydesign-Testalgorithms-TestgenerationforEmbeddedRAMs.

Textbooks:

1. M. Abramovici, M. Breuer, and A. Friedman, ―Digital Systems Testing and Testable Design, IEEE Press, 1990.
2. M. Bushnell and V. Agrawal, ―Essentials of Electronic Testing forDigital, Memory & Mixed-Signal VLSICircuits‖, Kluwer Academic Publishers, 2000

References:

1. Stroud,―ADesigner‘sGuidetoBuilt-inSelf-Test‖,KluwerAcademicPublishers,2002
2. V.AgrawalandS.C.Seth,TestGenerationforVLSIChips,ComputerSocietyPress.1989

23HRECE5	**FPGA ARCHITECTURES** **Honors with VLSI specialization**	**L**	**T**	**P**	**C**
		3	0	0	3

Course Objectives:

1. To explore the evolution, design flow, and applications of FPGAs in modern digital systems.
2. To design and implement digital systems using Programmable Logic Devices (PLDs) for complex operations.
3. To study FPGA/CPLD architectures, programming technologies, and commercially available FPGA families.
4. To analyze the architecture, functionality, and performance impact of FPGAs and CPLDs.
5. To understand FPGA routing architectures, routing strategies, and their implementation in modern FPGA families like Kintex-7, Virtex-7, and Artix-7.

Course Outcomes:
At the end of this course, the students will be able to

1. Explain FPGA architecture, design process, and real-world applications in digital circuit implementation.
2. Develop efficient digital circuits such as universal blocks, memory units, floating-point multipliers, and barrel shifters using PLDs.
3. Analyze FPGA/CPLD programming technologies and compare commercially available FPGA architectures like Xilinx, Actel, and Altera.
4. Evaluate FPGA/CPLD building blocks, routing structures, and delay models for efficient digital design.
5. Understand FPGA routing structures, analyze routing strategies, and apply them in real-world FPGA applications using Kintex-7, Virtex-7, and Artix-7.

UNIT 1

IntroductiontoFPGAs: EvolutionofprogrammabledevicesFPGADesignflowApplicationsofFPGA.

UNIT II

DesignExamplesusingPLDs: DesignofUniversalblockMemoryFloatingpointmultiplierBarrelshifter.

UNIT III

FPGAs/CPLDs: ProgrammingTechnologiesCommerciallyavailableFPGAsXilinx‘sVertexandSpartan, Actel‘s FPGA, Altera‘s FPGA/CPLD.

UNIT IV

Building blocks of FPGAs/CPLDs: Configurable Logic block functionality, Routing structures, Input/output Block, Impact of logic block functionality on FPGA performance, Model for measuring delay.

UNIT V

Routing Architectures: Routing terminology, general strategy for routing in FPGAs, routing for row – based FPGAs, introduction to segmented channel routing, routing for symmetrical FPGAs, example of routing in a symmetrical FPGA, general approach to routing in symmetrical FPGAs, independence from FPGA routing architectures, FPGA routing structures. FPGA architectural assumptions, the logic block, the connection block, connection block topology, the switch block, switch block topology, architectural assumptions for the FPGA

CASESTUDY–ApplicationsusingKintex-7,Viretex-7,Artix-7.

Textbooks:

1. John V. Oldfield and Richard C. Dorf, Field Programmable Gate Arrays: Reconfigurable Logic for Rapid Prototyping and Implementation of Digital Systems, Wiley-Interscience, 1995, 1st Edition.
2. FrankBruno,FPGAProgrammingforBeginners,Packt,2021.
3. FrankBrunoandGuyEschemann,TheFPGAProgrammingHandbook, Packt,2024,2nd Edition.
4. StephenD.Brown,RobertJ.Francis,JonathanRoseandZvonkoG.Vranesic,FieldProgrammable Gate Arrays, Springer Science+Business Media, LLC, 1992, 1st Edition.

References:

1. CliveMaxfield,TheDesignWarrior‘sGuidetoFPGAs:Devices,ToolsandFlows,Elsevier-Newnes, 2004.
2. DatasheetsofArtix-7,Kintex-7,Virtex-7.

23HRECE6	**ANALOG AND DIGITAL IC DESIGN LAB**	**L**	**T**	**P**	**C**
	Honors with VLSI specialization	0	0	3	1.5

Course Objectives:

1. To gain proficiency in designing and analyzing MOSFET-based analog circuits, including amplifiers and current mirrors.
2. To explore the implementation of feedback topologies and differential amplifiers to enhance circuit performance.
3. To enhance proficiency in simulating and optimizing two-stage operational amplifiers from schematic to post-layout.
4. To acquire proficiency in designing and simulating CMOS inverters and logic gatesusingEDA tools.
5. To explore variousarchitectures for arithmetic circuitssuch as adders, shift registers, and multipliers.
6. To gain hands-on experience infunctional simulation, timing analysis, and RTL-to-GDS-II implementation**.**

Course Outcomes:

At the end of this course, the students will be able to

1. Construct and evaluate single-stage and multi-stage amplifiers with various loads and feedback techniques.
2. Apply the principles of current sources, sinks, and mirrors for effective circuit biasing.
3. Implement and refine CMOS differential and two-stage operational amplifiers through post-layout simulations.
4. Construct and analyze CMOS inverters and logic gates with different design constraints and logic styles.
5. Implement and compare parallel adders, shift registers, and multipliers for performance optimization.
6. Develop and verify digital systems through functional simulation, static timing analysis, and post-synthesis verification.

List of Experiments :

Any five experiments from each group (All circuit still post layout)

Analog IC Design Lab

1. Lambda calculation for PMOS & NMOS, Transconductance plots,
2. Single transistor amplifier with different loads,
3. CS amplifier with source degeneration,
4. Cascode amplifier.
5. Basiccurrentsink,Cascodecurrentsink.
6. Basiccurrentsource,Cascodecurrentsource.
7. Basiccurrentmirror,Wilsoncurrent mirror,
8. Cascodecurrentmirror,

9. Feedback topologies,
10. CMOS differential amplifier with current mirror load.
11. Two stage Operational amplifier.

Digital IC Design Lab

1. DesignandSimulationofCMOSInvertertostudythetransferCharacteristicsbyvaryingthe design constraints using EDA Tools
2. DesignandSimulationoflogicgatesusingvariouslogicstylesandcomparetheperformance

Designthefollowingbuildingblocksemployingvariousarchitecturesanddevelop HDLmodels:

3. 32-bitParalleladderusing8-bitaddermodule,
4. 32-bitShiftregisterusing8-bitShiftregistermodule
5. Combinational and sequential multipliers: 8 x 8 multiplier,
6. Combinational and sequential multipliers: 16 X 16 multipliers
7. Performthefunctionalsimulation,StaticTimingAnalysisandpostsynthesistimin gverification RTL to GDS-II: Design any System as a case Study

Text Books:

1. Behzad Razavi, Design of Analog CMOS Integrated Circuit, McGraw Hill Education, 2017, 2ndEdition.
2. PaulJ.Hurst,PaulR.Gray,RobertGMeyerandStephenH.Lewis,AnalysisandDesignofAnalog Integrated Circuits, Wiley, 2024, 6th Edition.
3. SamirPalnitkar,VerilogHDL,PearsonEducation,2003,2nd Edition.
4. ErikBrunv and, Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, Pearson, 2011.

Reference Books:

1. Randall L. Geiger, Phillip E. Allen and Noel R. Strader, VLSI Design Techniques for Analog and Digital Circuits, Tata McGraw-Hill Education, 1989.
2. David Johns, Tony Chan Carusone and Kenneth Martin, Analog Integrated Circuit Design, Wiley, 2011, 2nd Edition.
3. JosephCavanagh,VerilogHDLDesignExamples,CRCPress,2018.
4. Blaine Readler, Verilog by Example: A Concise Introduction for FPGA Design, Full ARC Press,2011.

23HRECE7	**PHYSICAL DESIGN AUTOMATION LAB** **Honors with VLSI specialization**	**L**	**T**	**P**	**C**
		0	0	3	1.5

Course Objectives:

1. To implement and analyze graph algorithms used in physical design automation for VLSI.
2. To study and apply line sweep algorithms for solving computational geometry problems efficiently.
3. To explore partitioning algorithms for efficient circuit design, including group migration, simulated annealing, and metric allocation methods.
4. To analyze various floor planning algorithms for VLSI design, focusing on constraint-based, hierarchical, and optimization techniques.
5. To study and apply routing algorithms for efficient pathfinding in VLSI design and network communication.

Course Outcomes:

At the end of this course, the students will be able to

1. Apply graph-based algorithms to solve problems like spanning trees, shortest paths, and Steiner trees in VLSI design.
2. Implement and analyze line sweep and extended line sweep methods for geometric problem-solving.
3. Apply partitioning techniques to optimize circuit design using algorithms like Kernighan-Lin, simulated annealing, and metric allocation.
4. Utilize floor planning algorithms to optimize area, performance, and layout efficiency in VLSI design.
5. Implement and analyze two-terminal and multi-terminal routing algorithms for optimal interconnection in circuits and networks.

List of Experiments: Any ten experiments are to be conducted (Minimum one from each group)

I. Graphalgorithms

1. Graph search algorithms
   - Depth first search
   - Breadth first search
2. Spanning tree algorithm
   - Kruskal‘s algorithm
3. Shortest path algorithm
   - Dijkstra algorithm
   - Floyd-Warshall algorithm
4. Steiner tree algorithm

II. Computational geometry algorithm

1. Line sweep method
2. Extended line sweep method

III. Partitioning algorithms

1. Group migration algorithms
   - Kernighan –Lin algorithm
   - Extensions of Kernighan-Lin algorithm
     - Fiduccias –Mattheyses algorithm
     - Goldberg and Burstein algorithm
2. Simulated annealing and evolution algorithms
   - Simulated annealing algorithm
   - Simulated evolution algorithm
3. Metric allocation method

IV. Floor planning algorithms

1. Constraint based methods
2. Integer programming based methods
3. Rectangular dualization based methods
4. Hierarchical tree based methods
5. Simulated evolution algorithms
6. Time driven Floorplanning algorithms

V. Routing algorithms

1. Two terminal algorithms
   - Maze routing algorithms
     - Lee‘s algorithm
     - Soukup‘s algorithm
     - Hadlock algorithm
   - Line-Probe algorithm
   - Shortest path based algorithm
2. Multi terminal algorithm
   - Stenier tree based algorithm
     - SMST algorithm
     - Z-RST algorithm