SREENIVASA INSTITUTE OF TECHNOLOGY AND MANAGEMENT STUDIES
(AUTONOMOUS)

QUESTION BANK

Year / Semester: III B.Tech VI Semester
Regulation: R23
Subject and Code: Digital Logic & Computer Organization – 23ESC232T

SYLLABUS

UNIT I: (9)
Data Representation: Binary Numbers, Fixed Point Representation. Floating Point Representation. Number base conversions, Octal and Hexadecimal Numbers, components, Signed binary numbers, Binary codes
Digital Logic Circuits-I: Basic Logic Functions, Logic gates, universal logic gates, Minimization of Logic expressions. K-Map Simplification, Combinational Circuits, Decoders, Multiplexers.

UNIT 2: (9)
Digital Logic Circuits-II: Sequential Circuits, Flip-Flops, Binary counters, Registers, Shift Registers, Ripple counters Basic Structure of Computers: Computer Types, Functional units, Basic operational concepts, Bus structures, Software, Performance, multiprocessors and multi computers, Computer Generations, Von- Neumann Architecture

UNIT 3: (9)
Computer Arithmetic : Addition and Subtraction of Signed Numbers, Design of Fast Adders, Multiplication of Positive Numbers, Signed-operand Multiplication, Fast Multiplication, Integer Division, Floating-Point Numbers and Operations Processor Organization: Fundamental Concepts, Execution of a Complete Instruction, Multiple-Bus Organization, Hardwired Control and Multi programmed Control

UNIT 4: (9)
The Memory Organization: Basic Concepts, Semiconductor RAM Memories, Read-Only Memories, Speed, Size and Cost, Cache Memories, Performance Considerations, Virtual Memories, Memory Management Requirements, Secondary Storage

UNIT 5: (9)
Input /Output Organization: Accessing I/O Devices, Interrupts, Processor Examples, Direct Memory Access, Buses, Interface Circuits, Standard I/O Interfaces

Prepared by Mrs.B.R.Usha rani, Mrs.S.P.Sasirekha, Mrs.R.Anitha, Mrs.G.Geethanjali

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Max Marks: 10

S.No.	CO	Questions	BT
Unit I: (Data Representation & Digital Logic Circuits – I**)**			
1	**1**	a) Explain fixed point and floating point representation. b) Convert (345)10 to binary and hexadecimal.	**L4**
2	**1**	Explain signed binary numbers and components.	**L3**
3	**1**	Perform binary subtraction using 2's complement.	**L4**
4	**1**	Minimize Boolean expression using K-Map.	**L3**
5	**1**	Design combinational circuit for given Boolean function.	**L5**
6	**1**	Explain universal logic gates with examples.	**L4**
7	**1**	Design 4:1 Multiplexer with diagram.	**L3**
8	**1**	Compare Decoder and Multiplexer.	**L5**
9	**1**	Simplify Boolean expression using Boolean laws.	**L4**
10	**1**	Explain logic gates with truth tables.	**L3**
11	**1**	Explain number base conversions with examples.	**L3**

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S.No.	CO	Questions	BT
Unit II: (Sequential Circuits & Basic Structure of Computers**)**			
1	**2**	a) Explain JK Flip-Flop. b) Compare SR and D Flip-Flops.	**L4**
2	**2**	Explain Ripple counters.	**L3**
3	**2**	Design 4-bit binary counter.	**L4**
4	**2**	Explain Shift registers and types.	**L3**
5	**2**	Analyze Von-Neumann architecture.	**L5**
6	**2**	Explain functional units of computer.	**L4**
7	**2**	Describe bus structures.	**L3**
8	**2**	Compare multiprocessors and multicomputers.	**L5**
9	**2**	Explain computer generations.	**L4**
10	**2**	Explain the procedure of implementing a synchronous sequential circuit with minimal usage of flipflops.	**L3**
11	**2**	Explain system performance metrics.	**L4**

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S.No.	CO	Questions	BT
Unit III: (Computer Arithmetic & Processor Organization**)**			
1	**3**	a) Explain signed number addition & subtraction. b) Design Fast Adder.	**L4**
2	**3**	Explain signed operand multiplication.	**L3**
3	**3**	Perform integer division algorithm.	**L4**
4	**3**	Explain floating point operations.	**L3**
5	**3**	Comment on the Booth's algorithm and its efficiency for multiplication representing the steps as a flow chart with example.	**L5**
6	**3**	Explain multi-bus organization.	**L4**
7	**3**	Differentiate hardwired & microprogrammed control.	**L3**
8	**3**	Design Arithmetic Logic Unit (ALU).	**L5**
9	**3**	Explain processor organization with block diagram.	**L4**
10	**3**	Explain multiplication of positive numbers.	**L3**
11	**3**	Describe control unit functions.	**L3**

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S.No.	CO	Questions	BT
Unit IV: (Memory Organization**)**			
1	**4**	a) Explain memory hierarchy. b) Compare RAM & ROM.	**L4**
2	**4**	Explain semiconductor RAM memories.	**L3**
3	**4**	Explain how cache memory is organized and managed for performance optimization.	**L4**
4	**4**	Discuss memory speed and cost tradeoff.	**L3**
5	**4**	Analyze virtual memory concepts.	**L5**
6	**4**	Explain memory management requirements.	**L4**
7	**4**	Describe memory performance considerations.	**L3**
8	**4**	Evaluate secondary storage devices.	**L5**
9	**4**	Explain associative memory.	**L4**
10	**4**	Define memory hierarchy.	**L3**
11	**4**	Compare SRAM and DRAM.	**L3**

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S.No.	CO	Questions	BT
Unit V: (**Input / Output Organization**)			
1	5	a) Explain programmed I/O. b) Explain interrupt driven I/O.	L4
2	5	Explain Direct Memory Access (DMA).	L3
3	5	Describe processor examples for I/O.	L4
4	5	Explain standard I/O interfaces.	L3
5	5	Analyze interrupt handling mechanism.	L5
6	5	Explain bus structures in I/O organization.	L4
7	5	Discuss the evolution and significance of USB in computer architecture	L3
8	5	Evaluate advantages of DMA over programmed I/O.	L5
9	5	Explain accessing I/O devices.	L4
10	5	Define interrupts and types.	L3
11	5	Explain data transfer techniques.	L3

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Note: L1-Remembering, L2-Understanding, L3-Applying, L4-Analyzing, L5-Evaluating, and L6-Creating

Instruction to Faculty Members:

The Six Levels of Bloom's Taxonomy:

1. **Remembering:** Retrieving, recognizing, and recalling relevant knowledge from long-term memory (e.g., list, define, name, locate).
2. **Understanding:** Constructing meaning, explaining ideas, or concepts (e.g., summarize, interpret, classify, compare).
3. **Applying:** Using information in new situations or implementing procedures to solve problems (e.g., solve, use, demonstrate, implement).
4. **Analyzing:** Breaking material into constituent parts, determining how the parts relate to one another and to an overall structure (e.g., contrast, categorize, distinguish, diagram).
5. **Evaluating:** Making judgments based on criteria and standards through checking and critiquing (e.g., judge, critique, justify, defend, argue).
6. **Creating:** Putting elements together to form a coherent or functional whole; reorganizing elements into a new pattern or structure (e.g., design, construct, develop, formulate).