SREENIVASA INSTITUTE OF TECHNOLOGY AND MANAGEMENT STUDIES
(Autonomous)
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

II B.Tech. - II Semester

23ECE242	ELECTRONIC CIRCUITS ANALYSIS	L T P C 2 1 - 3

PRE-REQUISITES: Engineering Mathematics

COURSE EDUCATIONAL OBJECTIVES:

1. Understand the characteristics of multistage and Differential amplifiers.
2. Analyze the frequency response of BJT and FET amplifiers
3. Understand the characteristics of feedback amplifiers.
4. Categorize different oscillator circuits based on the application and analyze the tuned amplifiers.
5. Analyze the power amplifiers for various applications.

UNIT 1: MULTISTAGE AND DIFFERENTIAL AMPLIFIERS (9)

Introduction –Classification of Amplifiers- Distortion in amplifiers, Coupling Schemes, RC Coupled Amplifier using BJT, Cascaded RC Coupled BJT Amplifiers, Cascode amplifier, Darlington pair, the MOS Differential Pair, Small-Signal Operation of the MOS Differential Pair, The BJT Differential Pair, and other Nonideal Characteristics of the Differential Amplifier.

UNIT –2: FREQUENCY RESPONSE (9)

Low-Frequency Response of the CS and CE Amplifiers, Internal Capacitive Effects and the High-Frequency Model of the MOSFET and the BJT, High-Frequency Response of the CS, follower, CE, CG and Cascode Amplifiers.

UNIT –3: FEEDBACK AMPLIFIERS (9)

Feedback Amplifiers: Introduction, The General Feedback Structure, Some Properties of Negative Feedback, The Four Basic Feedback Topologies, The Feedback Voltage Amplifier (Series—Shunt), The Feedback Transconductance Amplifier (Series—Series), The Feedback Trans-Resistance Amplifier (Shunt—Shunt), The Feedback Current Amplifier (Shunt—Series).

UNIT –4: OSCILLATORS AND TUNED AMPLIFIERS (9)

Oscillators: General Considerations, Phase Shift Oscillator, Wien-Bridge Oscillator, LC Oscillators, Relaxation Oscillator, Crystal Oscillators, Illustrative Problems.

Tuned Amplifiers: Basic Principle, Use of Transformers, Single Tuned Amplifiers, Amplifiers with multiple Tuned Circuits, Stagger Tuned Amplifiers.

UNIT –5: POWER AMPLIFIERS (9)

Introduction, Classification of Output Stages, Class A Output Stage, Class B Output Stage, Class AB Output Stage, Biasing the Class AB Circuit, CMOS Class AB Output Stages, Power BJTs, Variations on the Class AB Configuration, Class C amplifier, MOS Power Transistors.

Total Hours: 45

SREENIVASA INSTITUTE OF TECHNOLOGY AND MANAGEMENT STUDIES
(Autonomous)
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE OUTCOMES:

On successful completion of the course, students will be able to		Pos
CO1	Understand the characteristics of multistage and differential amplifiers.	PO1, PO2, P03, PO4
CO2	Examine the frequency response of multistage and differential amplifier circuits using BJT & MOSFETs at low and high frequencies.	PO1, PO2, P03, PO4
CO3	Investigate different feedback amplifiers based on the application.	PO1, PO2, P03, PO4
CO4	Derive the expressions for frequency of oscillation and condition for oscillation of RC and LC oscillator circuits. Evaluate the performance of different tuned amplifiers	PO1, PO2, P03, PO4
CO5	Understand the characteristics of power amplifiers.	PO1, PO2, P03, PO4

TEXT BOOKS:

1. Millman, C Chalkias, "Integrated Electronics", 4thEdition, McGraw Hill Education (India) Private Ltd., 2015.
2. Adel. S. Sedra and Kenneth C. Smith, "Micro Electronic Circuits," 6th Edition, Oxford University Press, 2011.

REFERENCE BOOKS:

1. Behzad Razavi, "Fundamentals of Micro Electronics", Wiley, 2010.
2. Donald A Neamen, "Electronic Circuits – Analysis and Design," 3rdEdition, McGraw Hill (India), 2019.
3. Robert L. Boylestad and Louis Nashelsky, "Electronic Devices and Circuits Theory", 9th Edition, Pearson/Prentice Hall, 2006.

REFERENCE WEBSITE:

1. https://nptel.ac.in/courses/112/103/112103109/
   https://nptel.ac.in/courses/122/104/122104015/
2. https://www.digimat.in/nptel/courses/video/112106180/L01.html
3. https://nptel.ac.in/courses/112/106/112106286/
4. https://nptel.ac.in/courses/112/105/112105164/
5. https://nptel.ac.in/courses/112/103/112103108/
6. https://nptel.ac.in/courses/122/104/122104014/

CO-PO MAPPING:

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO.1	3	2	2	2	-	-	-	-	-	-	-	-
CO.2	3	2	2	2	-	-	-	-	-	-	-	-
CO.3	3	2	2	2	-	-	-	-	-	-	-	-
CO.4	3	2	2	2	-	-	-	-	-	-	-	-
CO.5	3	2	2	2	-	-	-	-	-	-	-	-
CO*	3	2	2	2	-	-	-	-	-	-	-	-

23ECE242 - Electronic Circuits Analysis

Unit-I
Multistage and Differential Amplifiers

Syllabus:- Introduction.- classification of Amplifiers Distortion in amplifiers, coupling Scheme, RC coupled Amplifier using BJT, Cascaded RC coupled BJT Amplifier, cascode amplifier, Darlington pair, the MOS Diff. pair, small-signal Operation of the MOS Differential pair, The BJT Differenial pair, and other Nonideal Char. of the Differantial Amplifier.

Introduction:-

* **Amplifier :**

- A CKT used to increases the Magnitude of I/p ct or volt. at the o/p by means of energy drawn from an external source.

- when signal is applied b/w B & E of properly biased transistor, a base ct starts flowing, due to transistor action, a large ac ct flow thru' collector load. Thus large volt. appears across the collector.

- In this way, a week signal applied b/w B & E is amplified.

Classification of amplifier:-

Amplifiers are classified according to their mode of operations.

① Based on Input:

(a) Small signal amplifier: (SSA)

When the I/p signal is so weak so as to produce small fun fluctuations in collector ct, compared to its quiescent value the amplifier is known as SSA.

(or)

The amplifier of I/p signal is less than threshold voltage (V_T) of transistor ($V_i < V_T$)

(b) Large Signal Amplifier:-

when the fluctuation in collector current are large, the amplifier is Large signal amplifier.

(or)

$V_i > V_T$

② Based on the output

(a) voltage amplifier: Amplifier high voltage level of I/p

(b) power amplifier: Amp. ckt applifamplified high power.

(c) Current amplifier: Amp ckt amplifier high current level of I/p

③ Based on Transistor configuration:-

(a) CE amplifier: The amplifier ckt formed using CE configuration

(b) CB amplifier: ckt formed using CB configuration.

(c) CC amplifier: ckt formed using CC configuration.

④ Based on number of stages:-

(a) single stage: using one transistor for amplification.

(b) Multi-stage: using ormore than one transistor ckt for amplification.

⑤ Based on Bandwidth:

(a) undecined amplifier: wideband amplifing.

(b) Tuned amplifier : Narrow band amplifier.

⑥ Based on Freq Response.

(a) Audio Freq. (AF) amplifier (20 Hz to 20KHz)

(b) Radio Freq (RF) amplifier (20 KHz to 300 GHz).

(c) Intermediate Freq Amplifier (455KHz)

⑦ Based on biasing condition:

(a) Class-A
(b) Class-B
(c) Class-AB
(d) Class-C
(e) Class-D
(f) Class-S

(3) Based on coupling :-

(a) Rc coupled Amplifier : A multistage amplifier ckt that is coupled to next stage using R & C combination.

(b) Transformed coupled : multistage amplifier ckt is coupled to next stage using transformer.

(c) Direct coupled (DC) Amplifier : A multistage amplifier ckt that is coupled to next stage directly.

Methods of Drawing small signal Equivalent ckt :-

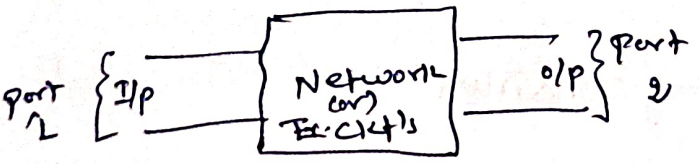
* port : is a pair of terminal in a network / circuit.

1st port – I/p terminal

2nd port - o/p terminal.

most of the ckt's are analyzed using 2 port N/w.

* The transistor may be regarded as two port N/w with 4 - variables as V_1, V_2 and I_1 & I_2



In them 2 variables are independent or other 2 variables dependents on independent variables.

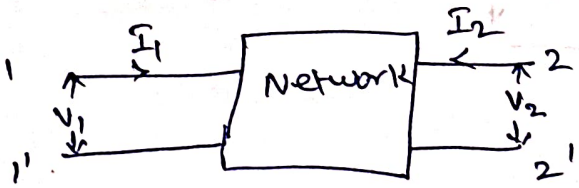
This leads to various parameters such as,

(1) Z-parameters (or) open ckt parameters.
- determined under either I/p or O/p is being kept open ckt condition.

(2) Y-parameters (or) short ckt parameters.
- determined under short ckt condition.

(3) H-parameters (or) Hybrid parameters:
- short ckt o/p and o/p ckt I/p.
- The parameter is easier to analyze and design a ckt.

Hybrid parameters:-



h_{11} - I/p Impe.
h_{12} - Rev. volt gain
h_{21} - Forward ct gain
h_{22} - O/p admitt.

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

Here I_1 & I_2 are taken as independent variables

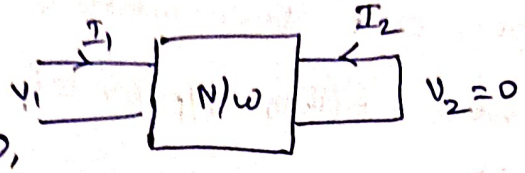
The 'h' parameters equi are

$$V_1 = h_{11} I_1 + h_{12} V_2 \quad \text{——— (1)}$$

$$I_2 = h_{21} I_1 + h_{22} V_2 \quad \text{——— (2)}$$

where, h_{11}, h_{21} - are determined by making o/p - SC
h_{12}, h_{22} - are determined by making I/p - OC

O/p short ckt $\rightarrow V_2 = 0$



from eqn ①,

$V_1 = h_{11} I_1$

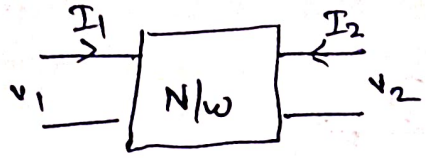
$$h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2=0} \Rightarrow h_{11} = h_i = \text{I/p impedance}$$

From eqn ②,

$I_2 = h_{21} I_1$

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0} \Rightarrow \text{Forward current gain} = h_{21} = h_f$$

I/p open ckt $\Rightarrow I_1 = 0$



from eqn ①

$V_1 = h_{12} V_2$

$$h_{12} = h_r = \left.\frac{V_1}{V_2}\right|_{I_1=0} \Rightarrow \text{Reverse volt. gain}$$

From eqn ②,

$$h_{22} = h_o = \left.\frac{I_2}{V_2}\right|_{I_1=0} \Rightarrow \text{output Admittance.}$$

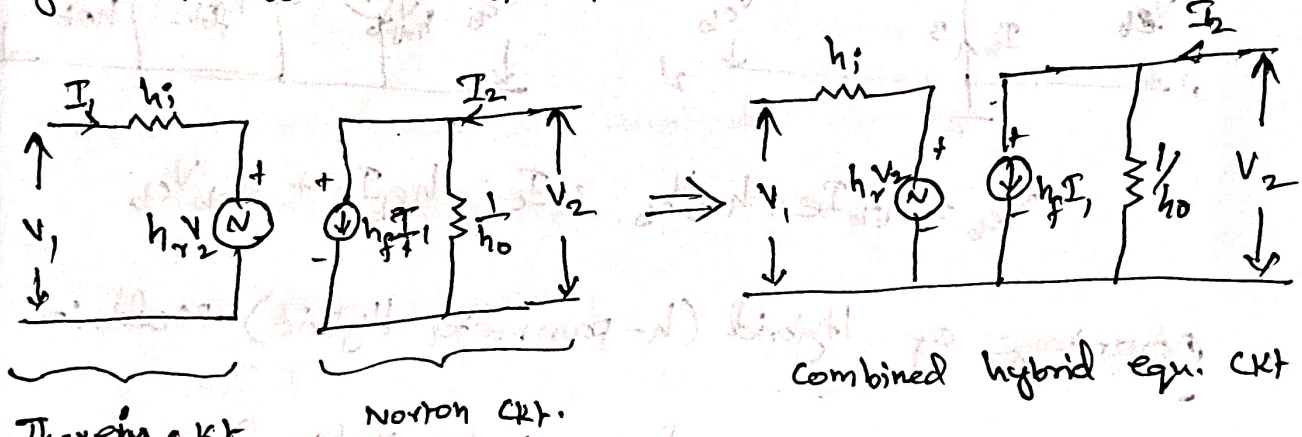
h-parameter equivalent ckt:-

$V_1 = h_{11} I_1 + h_{12} V_2$ — Thevein's equ ckt

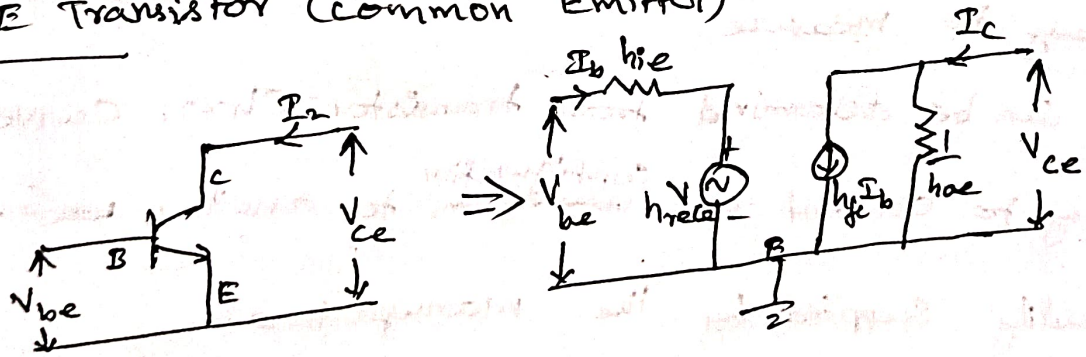
$I_2 = h_{21} I_1 + h_{22} V_2$ — Norton equ ckt.

* hybrid equivalent ckt is a combination of Theveins equ ckt and Norton equ ckts.

* I/p equ ckts is a Theveins equ ckt (voltage generator with series Resist and o/p portion is a Norton equ ckt (or) current generator with shunt resistance



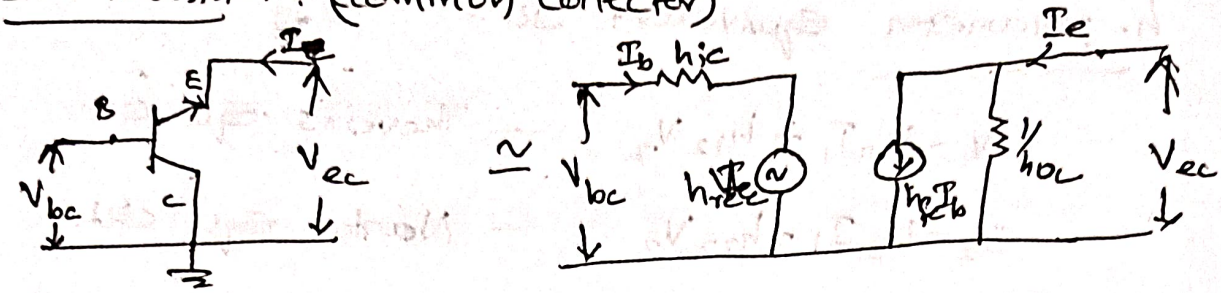
CE Transistor (common Emitter)



$V_{be} = h_{ie} I_b + h_{re} V_{ce}$

$I_c = h_{fe} I_b + h_{oe} V_{ce}$

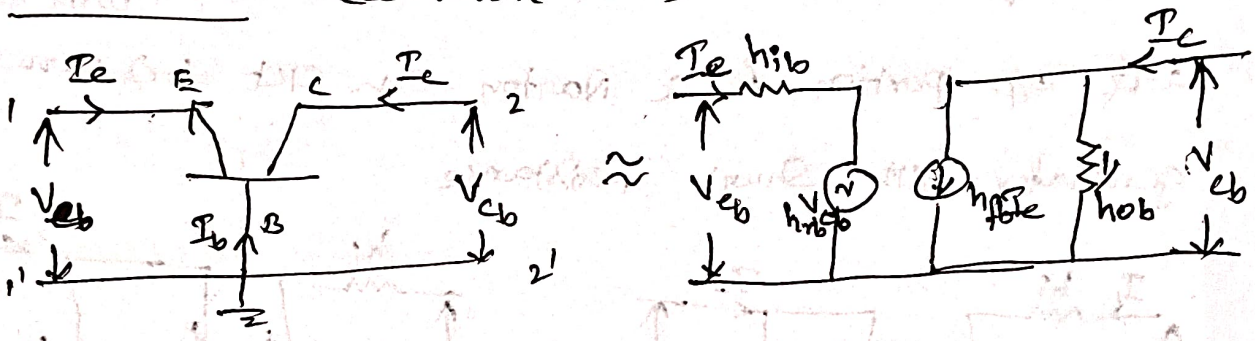
CC Transistor : (common collector)



$$V_{bc} = h_{ic} I_b + h_{rc} V_{ec}$$

$$I_e = h_{fc} I_b + h_{oc} V_{ec}$$

CB Transistor (common base)



$$V_{eb} = h_{ib} I_e + h_{rb} V_{cb} \quad ; \quad I_c = h_{fb} I_e + h_{ob} V_{cb}$$

Advantage of Hybrid (h-parameter Hybrid) Model :-

1. h-parameters are real no. upto radio freq.
2. Easy to measure
3. It can be determined from transistor Char. curve.
4. Easy to convert one configuration to another configuration.
5. Readily supplied by the manufacturers.
6. They are convenient to use in circuit analysis and design.

Distortion in Amplifier

* Ideally output should be a faithful reproduction of the Input. This is called fidelity. of course there would be changes in amplitude levels.

* In practical case, o/p waveform tends to be differed from the input, called as distortion

* distortion arise either from inherent non-linearity in the transistor char. or from the influence of the associated circuits.

Type : (1) non-Linear or amplitude distortion.

(2) Freq. distortion

(3) phase distortion

(4) Inter modulation distortion.

① Non-Linear distortion :-

This is produced when the operation is over the non-linear part of the transfer char. of the transistor. Since the amplifier amplifies diff. parts of the input differently.

Ex :- some time waveform clipped, Harmonics in signal

② Freq. Distortion: When the different frequency components in the input signal are amplified differently called as Freq Distortion.

* Various freq reactance (C & L) presents in the circuit produces freq distortion

③ phase Distortion:-

* This occurs due to different frequency components of the input signal suffering different phase shifts.

* occurs due to reactive effects and active devices

Ex: TV picture reception

④ Inter Modulation Distortion:-

* The harmonics introduced in the amplifier can combine with each other or with the original frequency to produces new frequency. This is called inter-modulation distortion.

* Ex:- This distortion results in unpleasant hearing.

Multistage Amplifiers

* single stage of amplifier - amplified very weak source such as microphone.

* no. of stages is increasing in amplifier Power level ~~more power~~.

That ~~the~~ type is called Multistage Amplifier.

Need for Cascading

(1) When the amplification of a Single stage amplifier is not sufficient

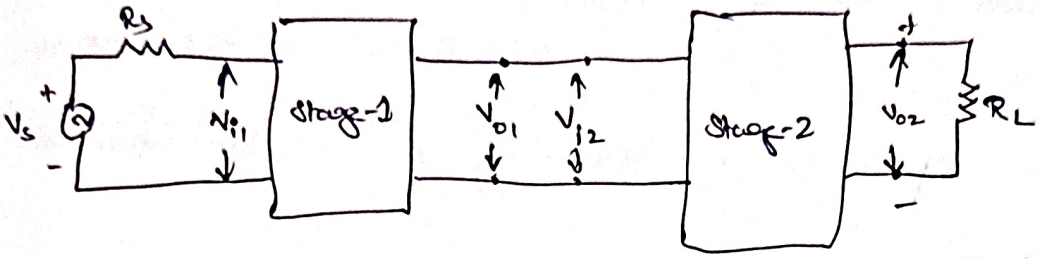
(2) When I/p (or) O/p impe. is not of the correct magnitude for a particular application two (or) more amplifier stages are connected, in cascade. Such amplifier, with two (or) more stages is also known an multistage amplifier.

Limitation of Multistage Amplifiers:-

(1) BW of Multistage amplifier is always ~~less than~~ than that of the BW of a Single-Stage amplifier.

(2) NonLinear ~~distortion~~ is more in multistage amplifiers than single stage amplifiers.

Two stage Cascade Amplifier



→ * overall volt. gain of the amplifier,

$$A_V = \frac{V_{o2}}{V_{i1}} = \frac{V_{o2}}{V_{i2}} \cdot \frac{V_{i2}}{V_{i1}}$$

where, $V_{o1} = V_{i2}$

$$A_V = \frac{V_{o2}}{V_{i2}} \cdot \frac{V_{o1}}{V_{i1}} = A_{V2} A_{V1}$$

→ ∴ n-stage cascade amplifier volt. gain is,

$$A_V = A_{V1} \cdot A_{V2} \cdots A_{Vn}$$

k^{th} stage is given by,

$$A_{Vk} = \frac{A_{ik} R_{Lk}}{R_{ik}}$$

[R_{Lk} - effective load resistance of k^{th} stage
R_{ik} - I/p impe. of k^{th} stage

→ Gain in decibels:

no. N decibels, $N = 10 \log \frac{P_2}{P_1}$ | $P_1 = \frac{V_i^2}{R_i}$, $P_2 = \frac{V_o^2}{R_o}$

$$N = 10 \log \frac{V_o^2/R_o}{V_i^2/R_i}$$

If $R_i = R_o = R$, then

$$N = 10 \log_{10} \frac{V_o^2}{V_i^2} = 10 \log_{10} \left(\frac{V_o^2}{V_i^2} \right) = 20 \log_{10} \left(\frac{V_o}{V_i} \right)$$

Methods of coupling Multistage Amplifiers.

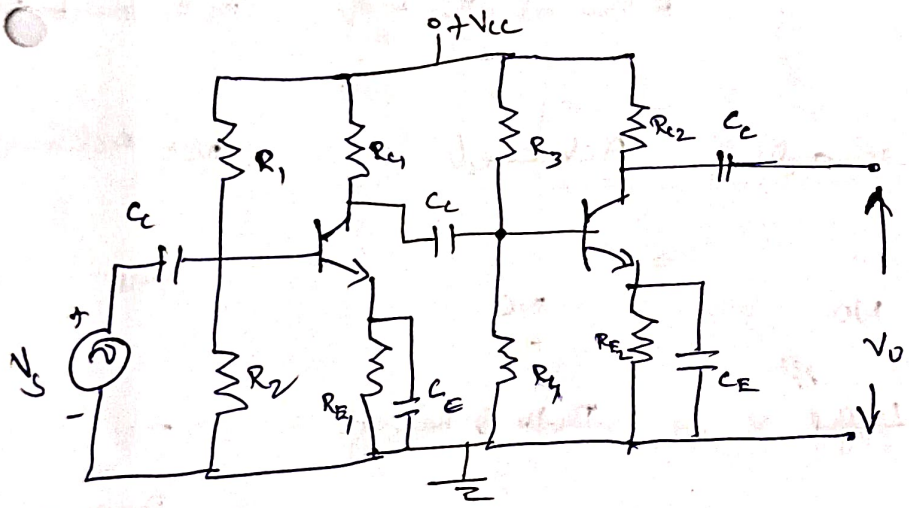
(1) RC Coupling

(2) Transformer Coupling

(3) Direct coupling. ← Directly coupled from 1st stage o/p to 2nd stage I/p terminal

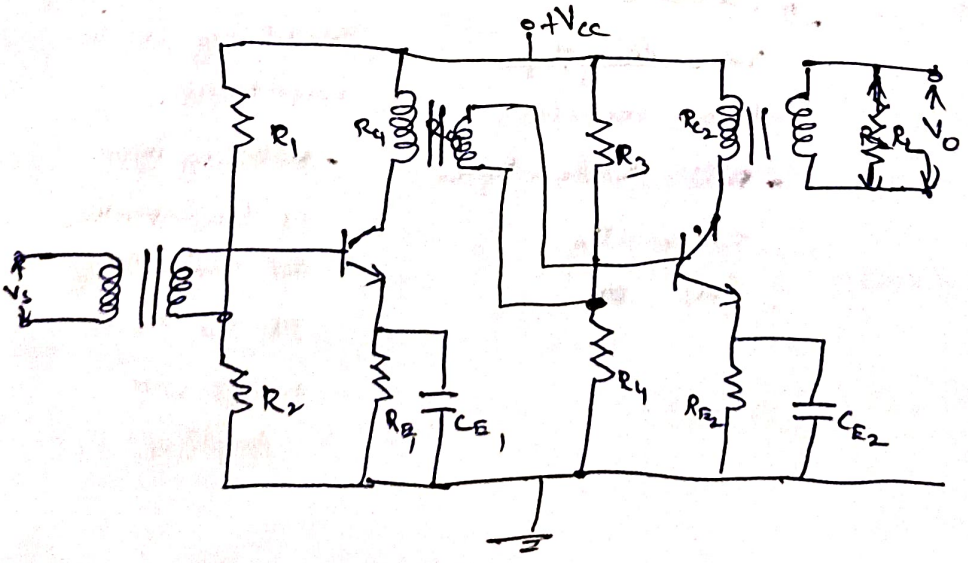
RC Coupling

1st stage o/p is coupled by coupling capacitor with load Resistor R is called RC coupling amplifier.



Transformer coupling :-

1st stage o/p is coupled by Transforms with 2nd stage I/p terminal is called transformer coupled Amplifier circuit

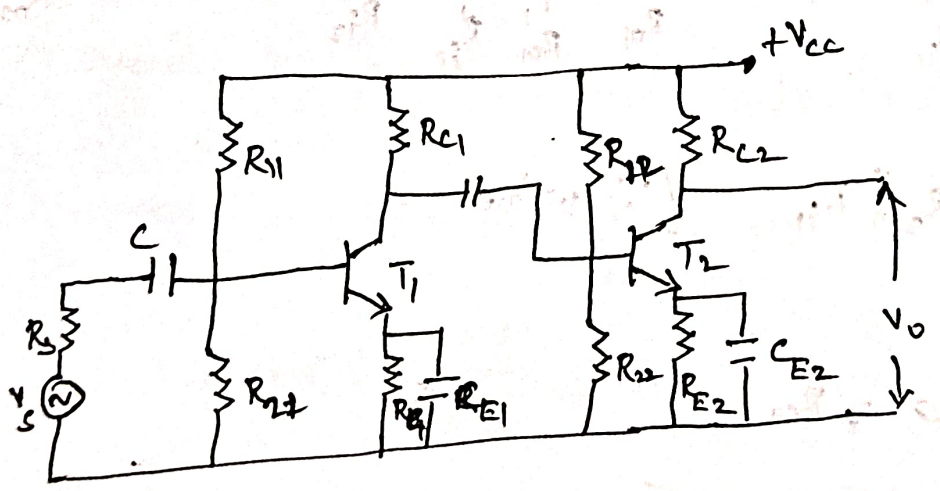


Comparison b/w Various Cascading Methods

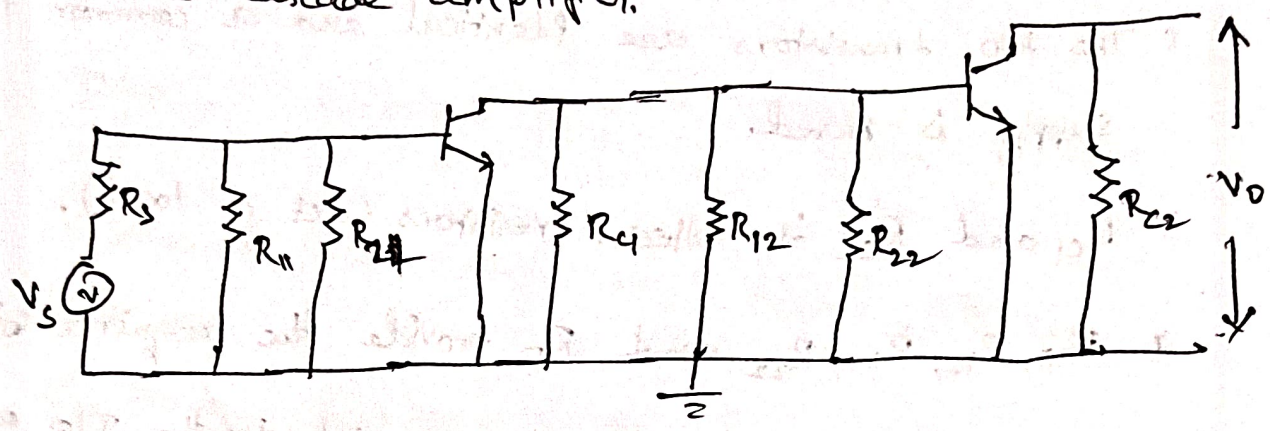
S.No	Parameter	RC Coupled	Transformer coupled	Direct Coupled
1.	Coupling component	Resistor & Capacitor	Impedance matching Transformer	—
2.	Block DC	Yes	Yes	—
3.	Freq. Response	Flat at Middle freq	Not uniform, high at resonant freq & low at other freq	Flat at middle freq & Improvement in the low freq resp
4.	Impe. Matching	Not achieved	Achieved	Not Achieved
5.	DC Amplification	NO	NO	Yes
6.	Weight	Light	Bulk & heavy	—
7.	Drift	Not present	Not present	Present.
8.	Hum	Not present	Present.	Not present.
10.	Application	- All audio - record~~ing~~ player - tape recorder - Public address system - Radio Rx - TV Rx	- Where Impe. matching is an important. - matching impe. of loudspeaker. - RF ampli. stage of Rx as a tuned volt. Amplifier.	- used in Amplification of slow varying

Two Stage RC Coupled CE-CE cascade Amplifier:-

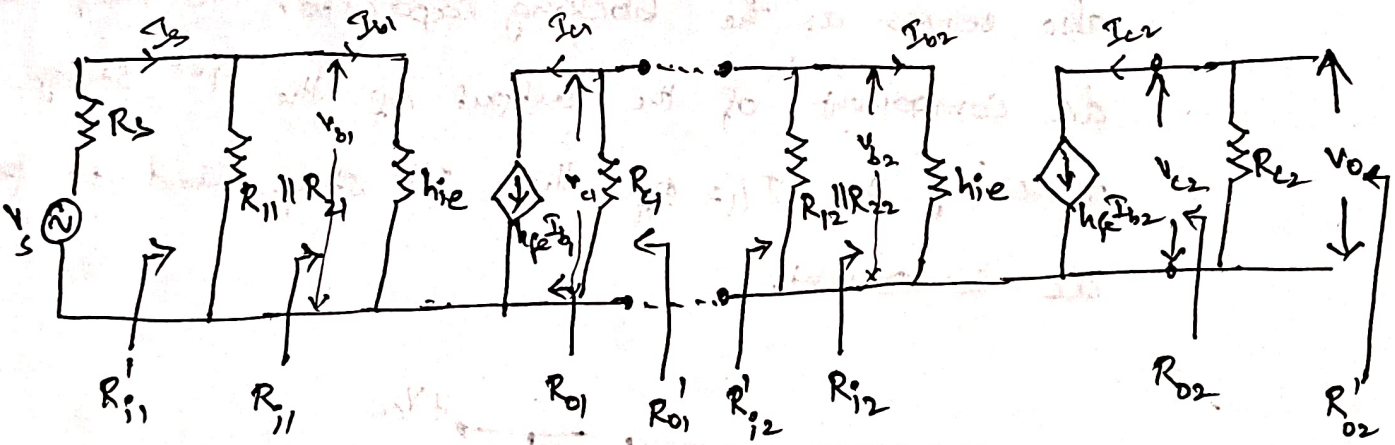
* The two transistors are identical and a common power supply is used.
* R_{C1} and R_{C2} is.. collector resistors (act as load).
* R_{11}, R_{12}, R_{21}, R_{22} and R_E provide the required bias.
* The o/p of 1st stage gets coupled to the I/p of the 2nd stage via coupling capacitor (C_c) which also serves as the blocking capacitor to keep the dc component of the output of the 1st stage from reaching the I/p of the 2nd stage and to pass ac component.



Assuming all capacitors arbitrarily large and act as a short circuit for ac signal we can draw CE-CE cascade amplifier.



by using h-parameter model, (using approximation model)



$R'_{i1} = R_{11} \| R_{21} \| R_{i1}$ $\quad [\because R_{i1} = h_{ie}$

$R_{01} = \infty$

$R'_{01} = R_{C1} \| \infty \simeq R_{C1}$

$R'_{i2} = R_{12} \| R_{22} \| R_{i2}$ $\quad [R_{i2} = h_{ie}$

$R_{02} = \infty$

$R'_{02} = R_{C2} \| \infty = R_{C2}$

Analysis of 2nd stage CE amplifier:

① Current Gain $(A_{i2}) = \frac{I_o}{I_{b2}} = \frac{-I_{c2}}{I_{b2}} = \frac{-h_{fe}I_{b2}}{I_{b2}} = -h_{fe}$

② Input Resistance $(R_{i2}) = \frac{V_{b2}}{I_{b2}} = \frac{h_{ie}I_{b2}}{I_{b2}} = h_{ie}$

③ overall I/p resistance $R'_{i2} = R_{12} \| R_{22} \| R_{i2}$

④ Voltage Gain $(A_{v2}) = A_{i2} * \frac{R_{c2}}{R_{i2}}$ [we know, $A_v = A_i * \frac{R'_L}{R_i}$]

Analysis of 1st stage:

⑤ $A_{i1} = \frac{-I_{c1}}{I_{b1}} = \frac{-h_{fe}I_{b1}}{I_{b1}} = -h_{fe}$

⑥ Input resistance $(R_{i1}) = \frac{V_{b1}}{I_{b1}} = \frac{h_{ie}I_{b1}}{I_{b1}} = h_{ie}$

⑦ overall I/p resistance, $R'_{i1} = R_{11} \| R_{21} \| R_{i1}$

⑧ Voltage again $(A_{v1}) = A_i \frac{R'_L}{R_i}$ ← we know

so, $A_{v1} = A_{i1}\left[\frac{R'_2}{R_{i1}}\right]$

$R'_2 = R_{c1} \| R_{12} \| R_{22} \| R_{i2}$

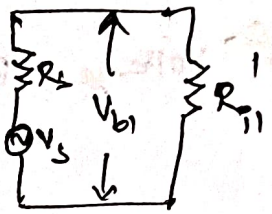
⑨ Overall Voltage Gain (A_{Vs}) (or) Volt gain with Source Resistance.

$$A_{Vs} = \frac{V_{c2}}{V_s} = \frac{V_{c2}}{V_{b2}} \times \frac{V_{b2}}{V_{c1}} \times \frac{V_{c1}}{V_{b1}} \times \frac{V_{b1}}{V_s} = \frac{V_{c2}}{V_{b2}} \times \frac{V_{c1}}{V_{c1}} \times \frac{V_{c1}}{V_{b1}} \times \frac{V_{b1}}{V_s}$$

$$= A_{V2} * A_{V1} \times \frac{V_{b1}}{V_s}$$

where, $V_{b1} = V_s \times \left[\frac{R_{i1}'}{R_s + R_{i1}'}\right]$

$$\therefore \frac{V_{b1}}{V_s} = \frac{R_{i1}'}{R_s + R_{i1}'}$$



$$A_{Vs} = A_{V1} * A_{V2} * \left[\frac{R_{i1}'}{R_s + R_{i1}'}\right]$$

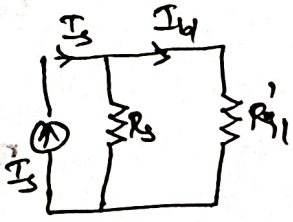
⑩ Overall Current Gain (A_{is}) or current gain with Source Resistance.

$$A_{is} = \frac{I_L}{I_s} = \frac{I_L}{I_{c2}} \times \frac{I_{c2}}{I_{b2}} \times \frac{I_{b2}}{I_{c1}} \times \frac{I_{c1}}{I_{b1}} \times \frac{I_{b1}}{I_s} \qquad [I_L = -I_{c2}$$

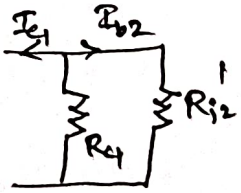
$$= \frac{-I_{c2}}{I_{c2}} \times A_{i2} * \frac{I_{b2}}{I_{c1}} \times A_{i1} \times \frac{I_{b1}}{I_s}$$

$$= -1 * A_{i2} * \frac{I_{b2}}{I_{c1}} * A_{i1} * \frac{I_{b1}}{I_s}$$

where, $I_{b1} = I_s * \frac{R_s}{R_s + R_{i1}'} \Rightarrow \frac{I_{b1}}{I_s} = \frac{R_s}{R_s + R_{i1}'}$ $\Rightarrow$



$$I_{b2} = -I_{c1} * \frac{R_{c1}}{R_{c1} + R_{i2}'} \Rightarrow \frac{I_{b2}}{I_{c1}} = -\left[\frac{R_{c1}}{R_{c1} + R_{i2}'}\right] \Rightarrow$$



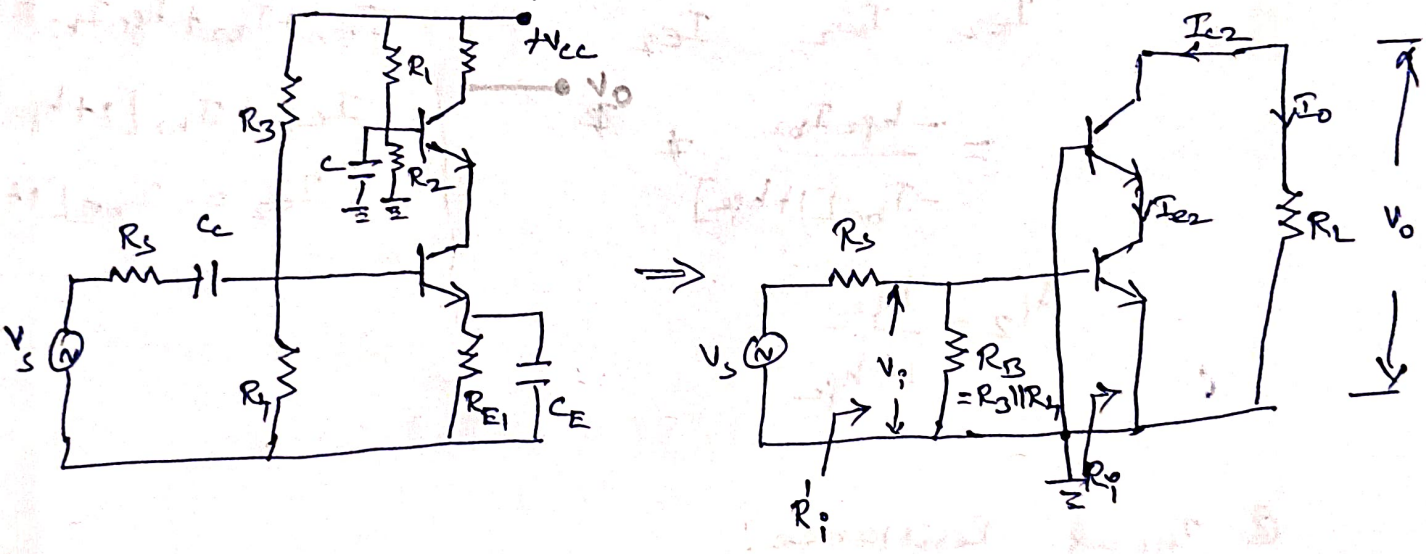
$$A_{is} = A_{i1} * A_{i2} * \left[\frac{R_s}{R_s + R_{i1}'}\right] * \left[\frac{-R_{c1}}{R_{c1} + R_{i2}'}\right]$$

Cascade Amplifier

* Consist of CE stage in series with a CB amplifier stage.

* It gives high I/p. impedance of a CE amplifier as well as good voltage gain and high freq performance of a common base (CB) circuit.

* It is a composite amplifier pair with large BW used for radio freq applications and as a video amplifier

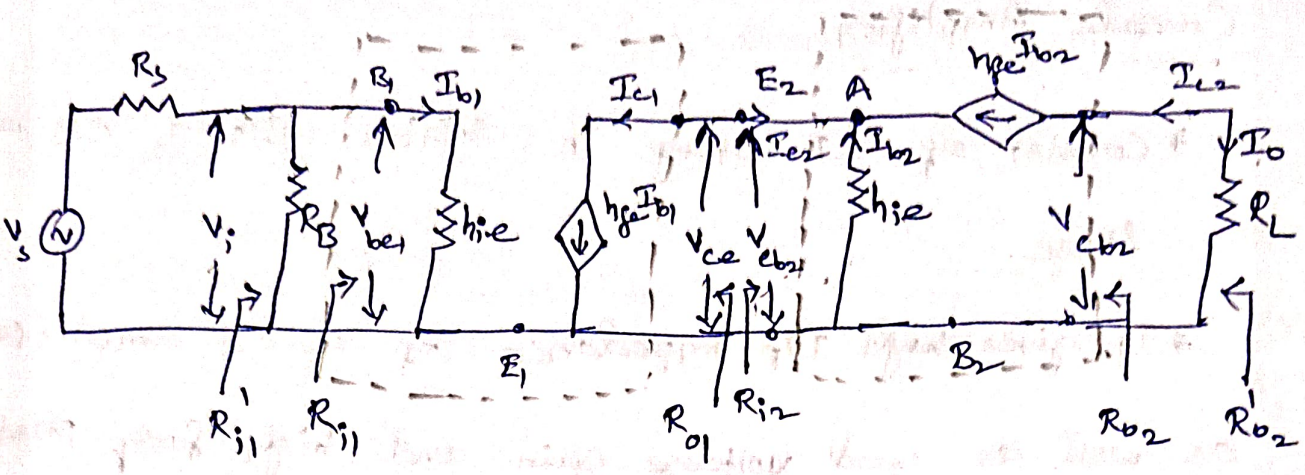


AC Equivalent circuit

* Collector current $I_{c_1} \approx I_{e_1}$ & I_{e_2} is same as I_{c_1}

$$\therefore I_{c_2} \approx I_{e_1}$$

* The simplified h-parameter equ. ckt for cascade amplifier is drawn by replacing transistor with their simplified equivalent circuit as shown in figure.



Analysis of 2nd stage [CB Amplifier]

① Current gain (A_{i2})

$$A_{i2} = \frac{I_o}{I_{e2}} = \frac{-I_{c2}}{I_{e2}} = \frac{-h_{fe}I_{b2}}{I_{e2}}$$

$$= \frac{-h_{fe}I_{b2}}{-I_{be}[1+h_{fe}]}$$

$$A_{i2} = \frac{h_{fe}}{1+h_{fe}}$$

At node 'A'.

$$I_{e2} + I_{b2} + I_{c2} = 0$$

$$I_{e2} + I_{b2} + h_{fe}I_{b2} = 0$$

$$I_{e2} + I_{b2}[1+h_{fe}] = 0$$

$$I_{e2} = -I_{b2}[1+h_{fe}]$$

② Input Resistance:

$$R_{i2} = \frac{V_{eb2}}{I_{e2}} = \frac{-h_{ie}I_{b2}}{I_{e2}} = \frac{-h_{fe}I_{b2}}{I_{e2}} = \frac{-h_{ie}I_{b2}}{-I_{b2}[1+h_{fe}]}$$

$$R_{i2} = \frac{h_{ie}}{1+h_{fe}}$$

③ Voltage Gain:-

$-I_c = -h_{fe}I_{b2}$

$$A_{v2} = \frac{V_{cb2}}{V_{eb2}} = \frac{I_o R_L}{-h_{ie}I_{b2}} = \frac{-h_{fe}I_{b2}R_L}{-h_{fe}I_{b2}} = \left[\frac{h_{fe}}{h_{ie}}\right]R_L$$

Analysis of 1st Stage:- [CE Amplifier]

① Current Gain (A_{i1}):

$$A_{i1} = \frac{-I_{c1}}{I_{b1}} = \frac{-h_{fe} I_{b1}}{I_{b1}} = -h_{fe}$$

$$\left[A_{i1} = \frac{I_o}{I_{b1}} = \frac{-I_{c1}}{I_{b1}} \right.$$

② I/p Resistance,

$$R_{i1} = \frac{V_{be1}}{I_{b1}} = \frac{h_{ie} I_{b1}}{I_{b1}} = h_{ie}$$

③ Voltage gain,

$$A_V = A_{i1} \left[\frac{R_{L1}}{R_{i1}} \right] \qquad \text{where, } R_{L1} = R_{i2}$$

$$= A_{i1} \left[\frac{R_{i2}}{R_{i1}} \right] = -h_{fe} \left[\frac{R_{i2}}{R_{i1}} \right]$$

where, $R_{i1} = h_{ie}$

$$R'_{i1} = R_B \| R_{i1} = R_3 \| R_4 \| R_{i1}$$

④ Overall I/p Resistance

$$R'_{i1} = R_B \| R_i = R_3 \| R_4 \| R_{i1}$$

⑤ Overall output Resistance,

$$R'_{o2} = R_{o2} \| R_L$$

$$= \infty \| R_L$$

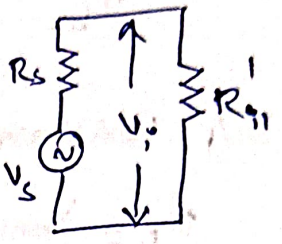
$$= R_L$$

⑥ Overall voltage Gain, $A_V = A_{V1} * A_{V2}$

⑦ Overall Voltage gain (A_V) with Source Resistance (A_{VS})

$$A_{VS} = \frac{V_o}{V_s} = \left(\frac{V_o}{V_i}\right)^{A_V} \times \frac{V_i}{V_s} = A_V * \frac{V_i}{V_s} = A_{V1} * A_{V2} * \frac{V_i}{V_s}$$

$$V_i = V_s \left[\frac{R_{i1}'}{R_s + R_{i1}'}\right]$$



$$\frac{V_i}{V_s} = \frac{R_{i1}'}{R_s + R_{i1}'}$$

$$\therefore \boxed{A_{VS} = A_V * \left[\frac{R_{i1}'}{R_s + R_{i1}'}\right]}$$

where, $R_{i1}' = R_{i1} \,||\, R_3 \,||\, R_4$

⑧ Overall Current Gain (A_i) with Source Resistance

$$A_{iS} = \frac{I_o}{I_s} = \frac{I_o}{I_{c2}} * \frac{I_{e2}}{I_{e2}} * \frac{I_{e2}}{I_{c1}} * \frac{I_{c1}}{I_{b1}} * \frac{I_{b1}}{I_s}$$

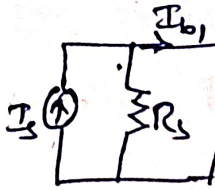
$I_o = -I_{c2}$, $I_{e2} = -I_{c1}$

$$= (-1) * (A_{i2}) * \frac{I_{e2}}{I_{c1}} * (-A_{i1}) * \frac{I_{b1}}{I_s}$$

$$= -1 \times -A_{i2} \times -1 \times -A_{i1} * \frac{I_{b1}}{I_s}$$

where,

$$I_{b1} = I_s \left[\frac{R_s}{R_s + R_i'}\right]$$



Norton's eqn.

$$\frac{I_{b1}}{I_s} = \frac{R_s}{R_s + R_i'}$$

$$\boxed{A_{iS} = A_{i1} * A_{i2} * \frac{R_s}{R_s + R_i'}}$$

1. Techniques of Improving I/p Impedance:-

* In emitter follower (or) CC ckt i/p imped. is high. ie; 200KΩ to 500 KΩ.

* for single stage emitter follwer ckt can give I/p impe. upto 500KΩ.

* However, In biasing resistors, I/p imped. is less because $R_i' = R_1 \| R_2 \| R_i$.

So I/p imped is improved by two stages of emitter follower amplifier.

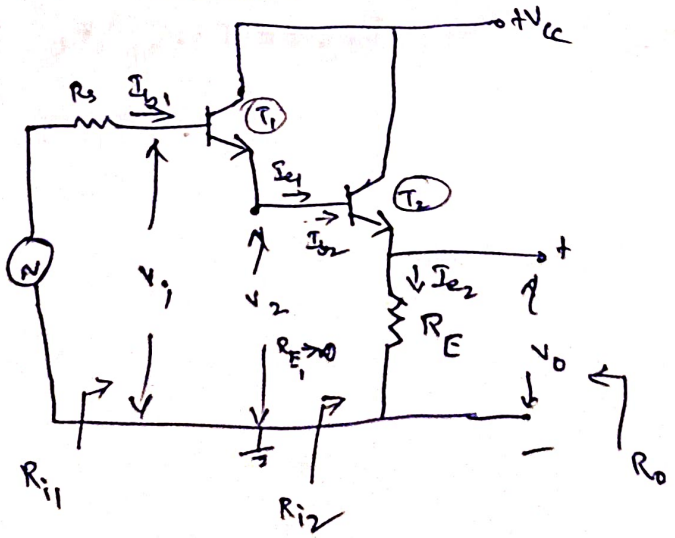
* Two tech. for Improving I/p impe.

(1) using direct coupling (Darlington Connection)

(2) using Bootstrap tech.

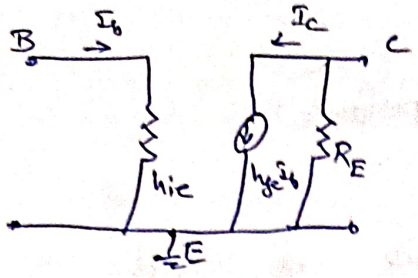
(1) Darlington Transistors:-

Two stages of emitter follower ckts are connected in cascaded.



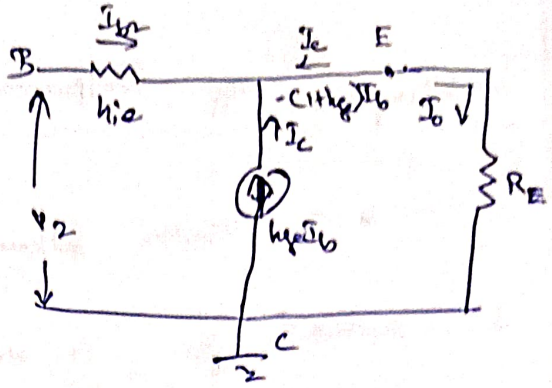
* Assume that R_L is ie; $R_L h_{oe} < 0.1$, therefore using approximate analysis method for analysing 2nd stage.

* draw equ. ckt for ie; h-parameter ckt for CC configuration.



CE config.

⇒ converting to CC



Analysis of 2nd Stage

(1) CC Gain: $A_{i2} = \frac{I_o}{I_b} = \frac{-I_e}{I_b} = \frac{(1+h_{fe})I_b}{I_b} = 1+h_{fe}$

$I_b + I_c + I_e = 0$

$[I_e = -(I_b + h_{fe}I_b)$

$I_e = I_b(1+h_{fe})$

(2) I/p Resistance $(R_{i2}) = \frac{V_2}{I_{b2}}$

Applying KVL to outer loop we get,

$$V_2 - I_{b2}h_{ie} - I_o R_E = 0$$

$$V_2 = I_{b2}h_{ie} + I_o R_E$$

$$\frac{V_2}{I_{b2}} = h_{ie} + \frac{I_o}{I_{b2}} R_E$$

$$R_{i2} = h_{ie} + A_{i2} R_E$$

$$\boxed{R_{i2} = h_{ie} + (1+h_{fe}) R_E}$$

$$R_{i2} \approx (1+h_{fe}) R_E \quad \because h_{ie} << (1+h_{fe}) R_E$$

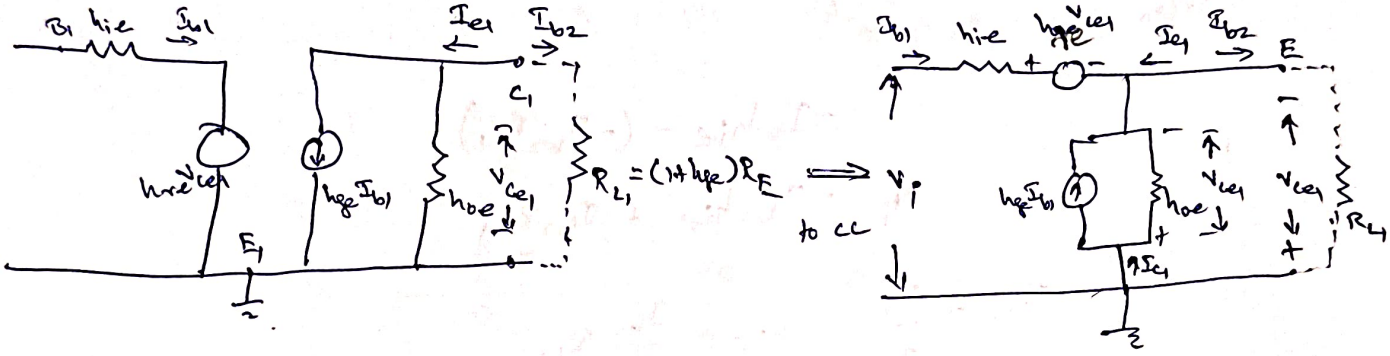
[3) $A_{i2} = \frac{I_o}{I_b} = \frac{-I_e}{I_b} = -(-1)$ ... $= \frac{1}{h_{ie}}$

Analysis of 1st stage:-

* load resistor of 1st stage is I/p resistance for of 2nd stage ckt. (i.e; R_{i2}).

* here, R_{i2} is high, i.e; $h_{oe}R_{i2} < 0.1$ - not satisfied

So here using exact analysis method for analysis of 1st stage.



* Ct Gain (A_{i1}):

$$A_{i1} = \frac{I_{b2}}{I_{b1}} = -\frac{I_{e1}}{I_{b1}}$$

$$I_{e1} = -(I_{b1} + I_{e1})$$

and $I_{e1} = h_{fe}I_{b1} + h_{oe}V_{ce1}$ (in figure) $= h_{fe}I_{b1} + h_{oe}(-I_{b2}R_{L1})$ $\left[V_{ce} = I_{e1}R_{L1} \simeq -I_{b2}R_{L1}\right]$

$= h_{fe}I_{b1} + h_{oe}I_{e1}R_{L1}$

Sub value of I_{c1} into I_{e1}.

$$I_{e1} = -(I_{b1} + h_{fe}I_{b1} + h_{oe}I_{e1}R_{L1}) = -I_{b1} - h_{fe}I_{b1} - h_{oe}I_{e1}R_{L1}$$

$$\therefore I_{e1} + h_{oe}I_{e1}R_{L1} = -I_{b1}(1+h_{fe})$$

$$A_{i1} = -\frac{I_{e1}}{I_{b1}} = \frac{1+h_{fe}}{1+h_{oe}R_{L1}} = \frac{1+h_{fe}}{1+h_{oe}(1+h_{fe})R_E} \quad [\because R_{L1} = (1+h_{fe})R_E$$

$\hookrightarrow h_{oe}R_E + h_{oe}h_{fe}R_E$

$$A_{i1} \simeq \frac{1+h_{fe}}{1+h_{oe}h_{fe}R_E} \quad [\because h_{fe} \gg 1]$$

I/p Resistance (R_i) =

$$R_{i1} = \frac{V_i}{I_{b1}}$$

Applying KVL to o/p loop we get,

$$V_i - I_{b1} h_{ie} - h_{re} V_{ce1} + V_{ce1} = 0$$

$$V_i = I_{b1} h_{ie} + h_{re} V_{ce1} - V_{ce1}$$

The terms $h_{re} V_{ce1}$ is negligible since h_{re} is in the order of 2.5×10^{-4}

$$= I_{b1} h_{ie} - (-I_{b2} R_{L1}) \qquad [V_{ce1} = I_e R_L = -I_{b2} R_L$$

$$V_i = I_{b1} h_{ie} + I_{b2} R_{L1}$$

$$R_{i1} = \frac{V_i}{I_{b1}} = h_{ie} + \frac{I_{b2}}{I_{b1}} R_{L1}$$

$$= h_{ie} + A_{i1} R_{L1}$$

$$\boxed{R_{i1} = h_{ie} + A_{i1} (1 + h_{fe}) R_E}$$ ✓

Sub value of A_{i1} we get,

$$R_{i1} = \frac{V_i}{I_{b1}} = h_{ie} + \frac{(1+h_{fe})(1+h_{fe}) R_E}{1 + h_{oe} h_{fe} R_E}$$

$$\boxed{R_{i1} = h_{ie} + \frac{(1+h_{fe})^2 R_E}{1 + h_{oe} h_{fe} R_E}}$$

$$R_{i1} \approx \frac{(1+h_{fe})^2 R_E}{1 + h_{oe} h_{fe} R_E} \qquad \left[h_{fe} << \frac{(1+h_{fe})^2 R_E}{1 + h_{oe} h_{fe} R_E} \right.$$

3(a) Overall Ct Gain (A_i)

$$A_i = A_{i1} \times A_{i2} = \frac{1+h_{fe}}{1+h_{oe}(1+h_{fe})R_E} \times (1+h_{fe}) = \frac{(1+h_{fe})^2}{1+h_{oe}(1+h_{fe})R_E}$$

(b) Overall volt. Gain

$$A_v = \frac{A_i R_L}{R_i}$$

By subtracting '1' on both sides we get

$$1 - A_v = 1 - \frac{A_i R_L}{R_i}$$

$$1 - A_v = \frac{R_i - A_i R_L}{R_i} = \frac{h_{ie} + h_{rc} A_i R_L - A_i R_L}{R_i}$$

(R_i)

$$= \frac{h_{ie}}{R_i} \quad [\text{since } h_{ic} = h_{ie} \text{ and } h_{rc} = 1 - h_{re}(A_i)]$$

$$A_v = 1 - \frac{h_{ie}}{R_i}$$

* Overall volt. gain in multistage Amplifier is,

$$A_v = A_{v1} \cdot A_{v2} = \left(1 - \frac{h_{ie}}{R_{i1}}\right)\left(1 - \frac{h_{ie}}{R_{i2}}\right)$$

$$A_v = 1 - \frac{h_{ie}}{R_{i2}} - \frac{h_{ie}}{R_{i1}} + \frac{h_{ie}^2}{R_{i1} R_{i2}}$$

we know, I/p resistance $R_{i1} >> R_{i2}$, so neglect the terms 2 3 & 4 in the eqn.

$$\boxed{A_v \approx 1 - \frac{h_{ie}}{R_{i2}}}$$

Output Impe. (R_{o2}):

$$R_o = \frac{1}{\text{o/p Admittance}} = \frac{1}{Y_o}$$

$$Y_o = Y_{o1} = h_{oc} - \frac{h_{fc} \cdot h_{rc}}{h_{ic} + R_s} = h_{oe} - \frac{-(1+h_{fe})}{h_{ie}+R_s}$$

since, $h_{oc} = h_{oe}$,

$h_{fc} = -(1+h_{fe})$

and $h_{ic} = h_{ie}$

$$Y_{o1} = h_{oe} + \frac{(1+h_{fe})}{h_{ie}+R_s}$$

$$\boxed{Y_{o1} = \frac{1+h_{fe}}{R_s + h_{ic}}}$$

$$h_{oe} << \frac{(1+h_{fe})}{h_{ic}+R_s}$$

$$R_{o1} = \frac{1}{Y_{o1}}$$

$$R_{o1} = \frac{h_{ie1} + R_s}{1+h_{fe}}$$

similiarly,

$$R_{o2} = R_{o1}$$

$$R_{o2} = \frac{R_{s2} + h_{ie2}}{1+h_{fe}}$$

After simplification $= \frac{R_s}{(1+h_{fe})^2} + \frac{h_{ie2}}{(1+h_{fe})}$

Notes:-

① * 1st stage DC o/p Ct is $-(1+h_{fe})I_{b1}$

* 1st stage o/p Ct is given to 2nd stage Ckt,

So 2nd stage o/p Ct is $(1+h_{fe})^n$ times I_{b1}

∴ o/p Ct is large & no. of stages is more in power stages.

② leakage Ct of the 1st stage is amplified into 2nd stage. so overall leakage Ct is high.

The MOS Differential Pair:-

* Mos Differential pair is a fundamental analog circuit.
* used to amplify the difference b/w two I/p voltage while rejecting common mode signals (noise).
* It is widely used in op-amps, comparators, ADC and analog IC's

⇒ Differential mode signal component; $V_{Id} = V_2 - V_1$

⇒ common mode signal components: $V_{cm} = \frac{V_2 + V_1}{2}$

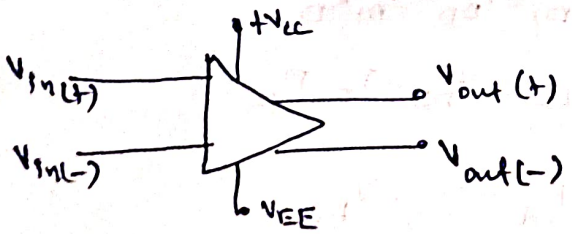
⇒ $V_o = A_d V_{Id} + A_{cm} V_{CM}$ [where, A_d - Differential Gain, A_{cm} - common mode Gain

* Typically reference or noise level not desired.

* Common mode Rejection Ratio (CMRR): Differential to common mode power gain ratio

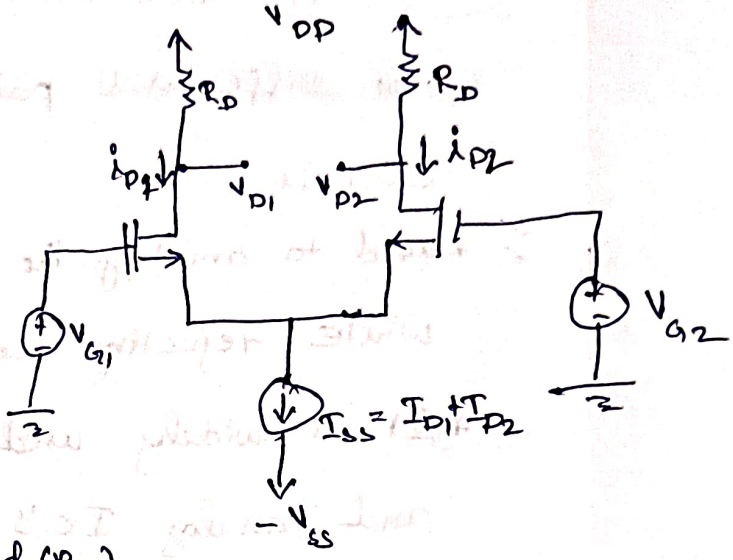
$$CMRR = 20 \log_{10}\left(\frac{A_d}{A_{cm}}\right)$$

*



- Differential structure Rejects coupled noise at the I/P
- Differential structure Rejects coupled noise at the power supply
- Differential structure Rejects coupled noise at the o/p.

Implementation of MOS Differential Amplifier:-



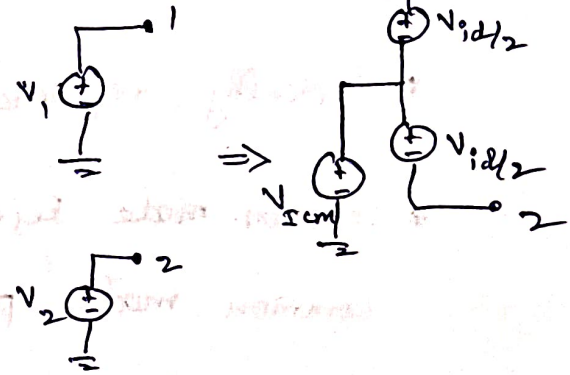
* Two matched MOS transistors Q_1 & Q_2 joined.
  ie; Same Technology, Same V_{TH}, same W and L transistor.
* Two CKts arranged symmetrically. ie; same Load (R_D), Source terminals joined, Equal gate bias V_{GS} (Zero Signal).
* Devices are biased using a constant current source (I_{SS})
* FET's should not enter ohmic region (operating region) of operation.
  ie; where it will become Volt-Controlled resistor

Signals in Diff. Amplifier:

Input signals.

$$V_{G1} = V_{cm} + \frac{V_{id}}{2} \quad ; \quad V_{G1} = \frac{V_{id}}{2}$$

$$V_{G2} = V_{cm} - \frac{V_{id}}{2} \quad ; \quad V_{G2} = -\frac{V_{id}}{2}$$



Output signals:

Individual output: $V_{D1} = V_{DD} - I_{D1} R_D$

$$V_{D2} = V_{DD} - I_{D2} R_D$$

Differential output: $V_{od} = V_{D1} - V_{D2}$

$$I_{OD} = I_{D1} - I_{D2}$$

Voltage Gain: $A_d = \frac{V_{od}}{V_{id}} = \frac{V_{D1} - V_{D2}}{V_{id}}$

⇒ Ex:- A MOS Differential pair is driven with a input CM level of 1.6V, If $I_{SS} = 0.5\,mA$, $V_{TH} = 0.5V$, and $V_{DD} = 1.8V$, what is the maxi. allowable load resistance (R_D) = ?

$$V_{DD} - R_D \frac{I_{SS}}{2} \geq V_{CM} - V_{TH}$$

$$R_D \leq 2\,\frac{V_{DD} - V_{CM} + V_{TH}}{I_{SS}}$$

$$\boxed{R_D < 2.8\ K\Omega}$$

Differential operation:-

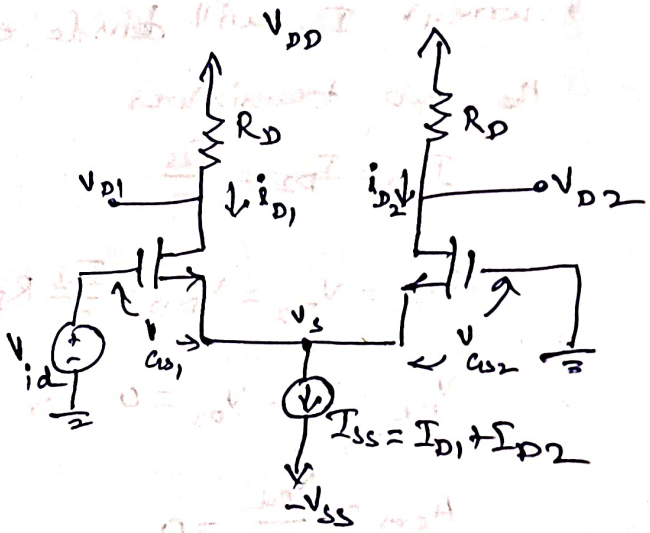
If V_{id} is applied to differential amplifier,

ie; $V_{id} \neq 0$

Let,

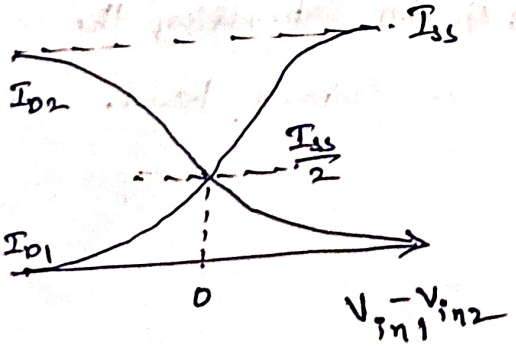
$V_{id} = V_{GS1} - V_{GS2} > 0$,

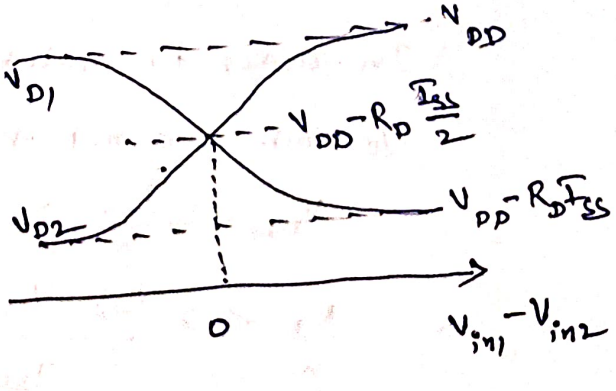
ie; $V_{GS1} > V_{GS2}$



V_{id} applied to Q_1 & Q_2 grounded

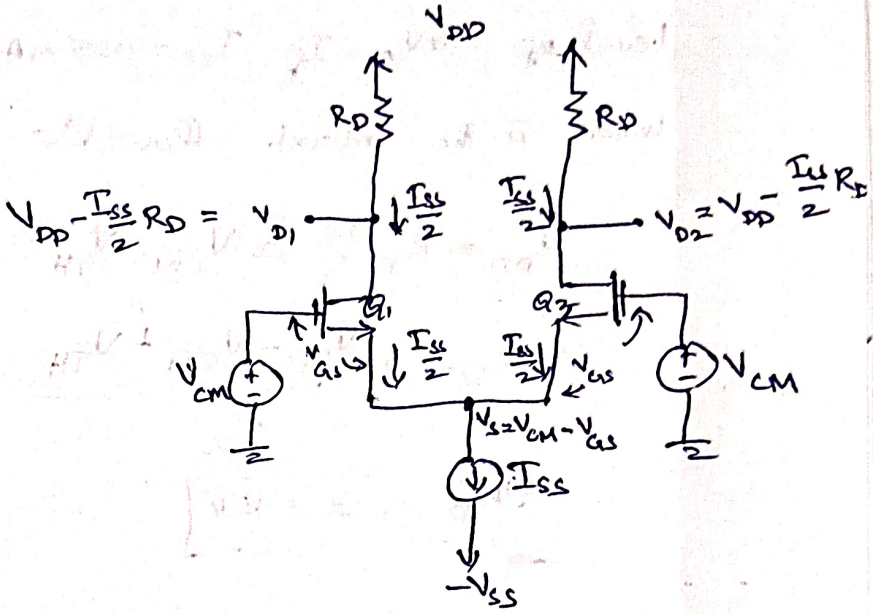
$I_{D1} > I_{D2}$





Common Mode operation:-

* Consider case when two gate terminals are joined together and connected to a common-mode voltage (V_{CM})



ie; $V_{G1} = V_{G2} = V_{CM}$

(or)

$V_{id} = V_{G1} - V_{G2} = 0$

$$\left[V_{GS} = V_t + V_{OV} = V_t + \sqrt{\frac{I}{(K_n' \frac{W}{L})}} \right]$$

* Current I_{SS} will divide equally b/w the two transistors

$$I_{D1} = I_{D2} = \frac{I_{SS}}{2}$$

$$V_{D1} = V_{D2} = V_{DD} - \frac{I_{SS}}{2} R_D$$

$V_{od} = V_{o1} - V_{o2} = 0$ $\Rightarrow$ o/p volt does not respond to common signal.

$$A_{cm} = \frac{V_{od}}{V_{icm}} = 0$$

Minimum common-mode output voltage:

$$V_{D1} = V_{D2} = V_{DD} - \frac{I_{SS}}{2} R_D$$

In order to maintain Q_1 & Q_2 in saturation, the common mode o/p volt can not fall below a certain level.

$$V_{DD} - R_D \frac{I_{SS}}{2} > V_{CM} - V_{TH}$$

$$R_D < 2 \frac{V_{DD} - V_{CM} + V_{TH}}{I_{SS}}$$

↑ This value usually limits voltage gain

Highest differential I/p,

$$i_{D1} = \frac{1}{2} K_n' \frac{W}{L} (V_{GS_1} - V_t)^2 = \frac{1}{2} \beta_1 (V_{GS} - V_t)^2$$

$$i_{D2} = \frac{1}{2} K_n' \frac{W}{L} (V_{GS_2} - V_t)^2 = \frac{1}{2} \beta_2 (V_{GS_2} - V_t)^2$$

$$(V_{GS} - V_t)^2 = \frac{2}{\beta_1} I_D$$

$$V_{GS} = V_t + \sqrt{\frac{2}{\beta_1} I_D}$$

$$= 0$$

$$V_{GS} = \left[\frac{2}{\beta_1} I_D\right]^{1/2}$$

Maximum $I_{D1} = I_{SS}$, when $I_{D2} = 0$

$$V_{ID} = V_{G1} - V_{G2} = V_{GS1} - V_{GS2} = \left[\frac{2I_{D1}}{\beta_1}\right]^{1/2} - \left[\frac{2I_{D2}}{\beta_2}\right]^{1/2}$$

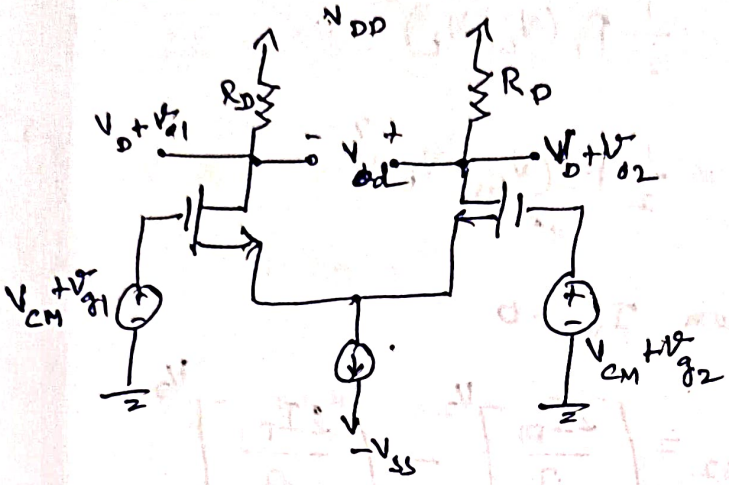
$$V_{ID} = \left[\frac{2I_{SS}}{\beta}\right]^{1/2} = \sqrt{2}\, V_{OV} \qquad \left[\because I_{D2} = 0\right.$$

$$-\sqrt{2}\, V_{OV} < V_{id} < \sqrt{2} V_{OV}$$

V_{OV} - overdrive voltage

To steer the current completely to one side of the pair, a difference input voltage V_{id} of at least $2^{1/2} V_{OV}$ (or) $\left[\frac{2I_{SS}}{\beta}\right]^{1/2}$ is needed.

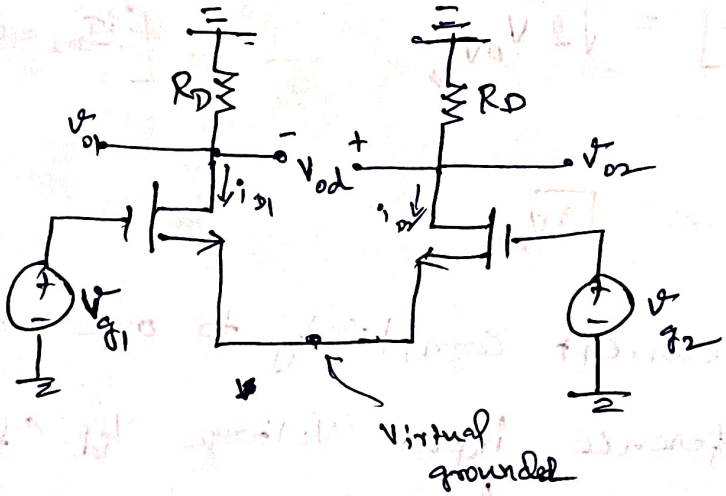
Small Signal Analysis:-



V_D - Drain voltage due to DC biasing volt.

v_{d1} - Drain volt. due to AC signal

AC Equivalent circuit,



$$V_{id} = V_{g1} - V_{g2}$$

Instantaneous signal values:-

$$i_{D1} = \frac{I_{SS}}{2} + g_m \frac{V_{id}}{2}$$

$$i_{D2} = \frac{I_{SS}}{2} - g_m \frac{V_{id}}{2}$$

g_m - transconductance

$$V_{D1} = V_{DD} - R_D\left(\frac{I_{SS}}{2} + g_m \frac{V_{id}}{2}\right)$$

$$V_{D2} = V_{DD} - R_D\left(\frac{I_{SS}}{2} - g_m \frac{V_{id}}{2}\right)$$

AC signal Components

$$i_{o1} = +g_m \frac{v_{id}}{2}$$

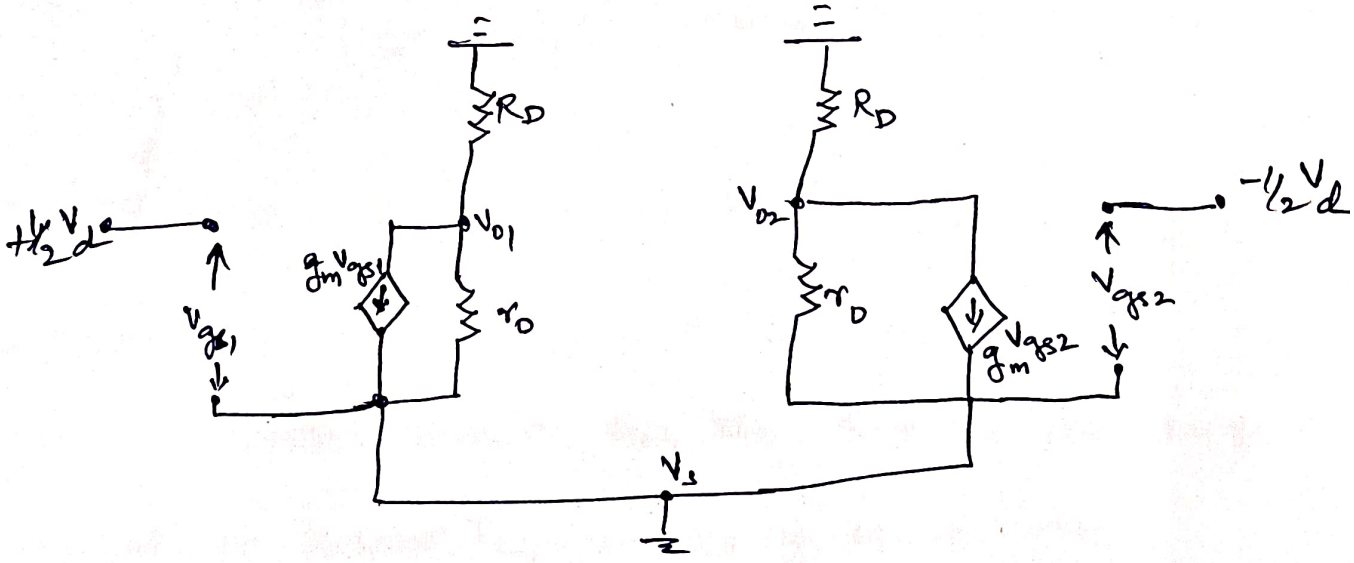
$$i_{o2} = -g_m \frac{v_{id}}{2}$$

$$v_{o1} = -\frac{g_m R_D v_{id}}{2}$$

$$v_{o2} = \frac{g_m R_D v_{id}}{2}$$

$$\therefore V_{od} = V_{D1} - V_{D2} = -\frac{g_m R_D v_{id}}{2} + \frac{g_m R_D v_{id}}{2} = -g_m R_D v_{id}$$

$$A_d = \frac{V_{od}}{v_{id}} = \frac{v_{o1} - v_{o2}}{v_{id}} = -g_m R_D \qquad \left[A_d = \frac{g_m R_D v_{id}}{v_{id}} = -g_m R_D \right.$$

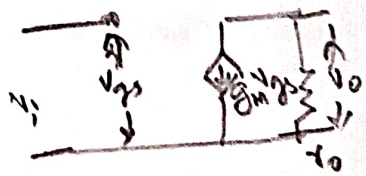


Input AC signal :-

$$v_{id} = v_{g1} - v_{g2}$$

$$i_{o1} = +g_m \frac{v_{id}}{2}$$

$$i_{o2} = -g_m \frac{v_{id}}{2}$$



Output ac signals

$$v_{o1} = -g_m \frac{v_{id}}{2} (r_o \| R_D)$$

$$v_{o2} = g_m \frac{v_{id}}{2} (r_o \| R_D)$$

$$v_{od} = v_{o1} - v_{o2} = -g_m (r_o \| R_D) v_{id}$$

$$A_d = \frac{v_{od}}{v_{id}} = -g_m (r_o \| R_D)$$

(or)

$$A_d = \frac{g_m}{g_o + g_D}$$

[where g_D – Transconductance of R_D

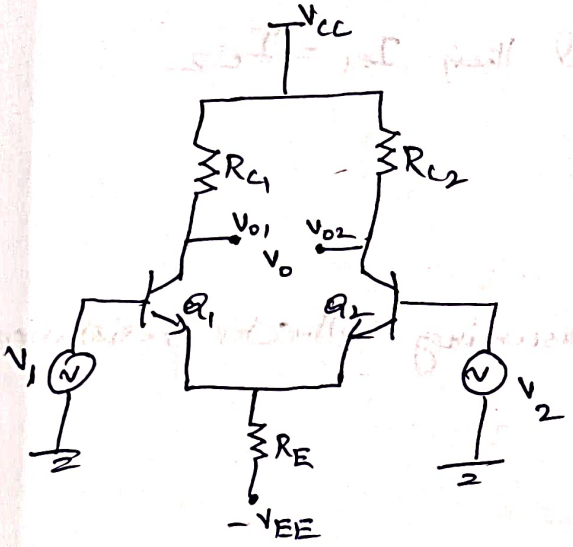
g_o – Transconductance of r_o

g_m – Transconductance.

BJT- Differential Amplifier Pair:-

* Differential amplifier basically uses emitter biased circuits which are identical in characteristics.

* This amplifier is also called emitted coupled differential amplifier



* I/p-1 of differential amplifier is connected to the base of transistor Q_1 and input-2 of the diff. amplifier is connected to the base of another transistor.

* V_{CC} and V_{EE} are 2- supplies for diff. amplifier.

Working:

* If I/p applied base of Q_1, then there is volt. drop across collector Resistor R_{C_1}. so, o/p of Q_1 is Low.

* When there is no I/p volt. to the transistor Q_1, the volt. drop across resistor R_{C_1} is very less as a result o/p transistor Q_1 is high.

* When Q_1-ON, Ie in Re increases ($I_e \approx I_c$). As a result, volt. drop across R_e increases and makes emitter of both transistor positive. In this condition, Q_2 does not conducts as there is no bias volt.

* As a result collector volt. of transistor Q_2 is high, Hence it is clear that the o/p is produced at the collector of Q_2 when I/p is applied to the base of Q_1,

* where, Q_1 & Q_2 same characteristics, two R_e Resistances and R_c Resistances also equal (ie; $R_{e1}=R_{e2}$ & $R_{c1}=R_{c2}$)

* mag. of supply volt. $+V_{cc}$ and $-V_{ee}$ also same.

If I_e V_{s1} & V_{s2} are equal then $I_{e1}=I_{e2}$

By ie; $I_e = I_{e1}+I_{e2}$

$$V_e = V_b - V_{be}$$

$V_{c1}=V_{c2}=V_{cc}-I_cR_c$ assuming collector resistance.

Application:-

- used as volt. comparator.
- volt. subtractors.
- used in operational amplifier to amplify the I/p signal.
- voltage follower.

Two modes of operation:-

① common mode operation.

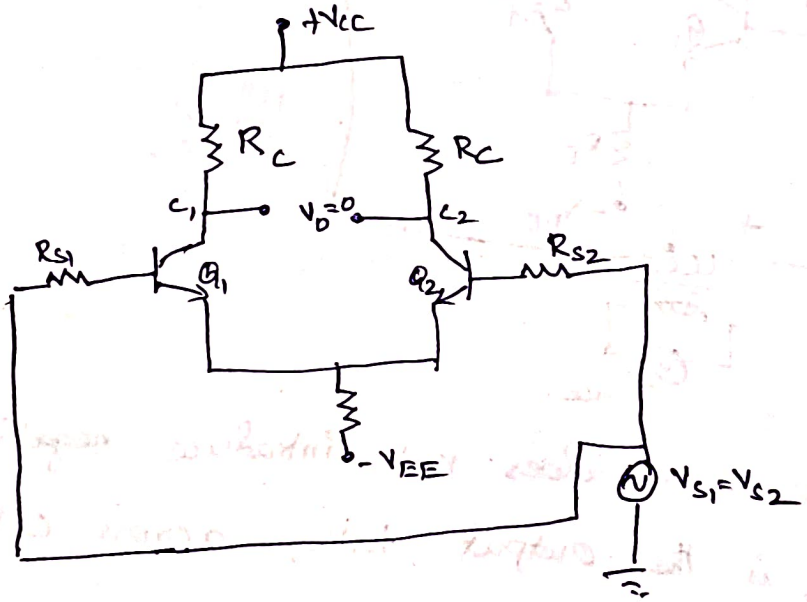
② Diff. mode operation.

① Common mode operation:

* I/p for Q_1 & Q_2 are derived from the same source. so two I/p are equal magnitude and same ~~&~~ phase.

* R_E - carries signal ct and provides a negative feedback at the condition of in-phase signal at the base of Q_1 & Q_2.

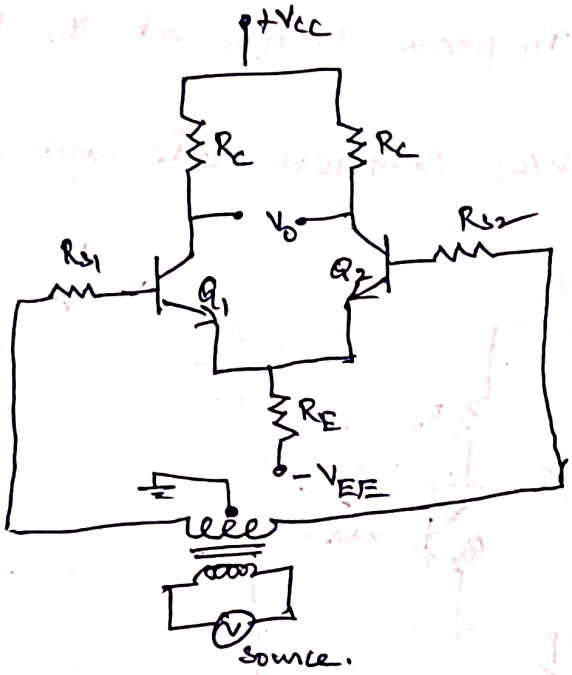
* This F.B reduces common mode gain of diff. amplifier



* The ~~If~~ two collector volt. of Q_1 & Q_2 is same magnitude & phase at the condition of same I/p. so ideally output of differential amplifier is zero. But practically flowing small amount of amount of ct and small volt. drops in o/p.

② Differential Mode operation:-

* Two I/p signals are different from each other. (180° out of phase)
* These signals, with opposite phase can be obtained from the Center tap transformer.



* R_E in this case does not introduce negative feedback while V_o is the output taken across collector of Q_1 and collector of Q_2.
* V_o is diff. b/w two signals ie; $V_o = V_{o1} - V_{o2}$

* Difference configuration of Diff. Amplifier:

① Dual I/p balanced o/p diff. amplifier. (Fig.1)

② Dual I/p, unbalanced o/p diff amplifier. (Fig.2)

③ Single I/p, balanced o/p diff. amplifier. (Fig.3)

④ Single I/p, unbalanced o/p diff amplifier. (Fig.4)

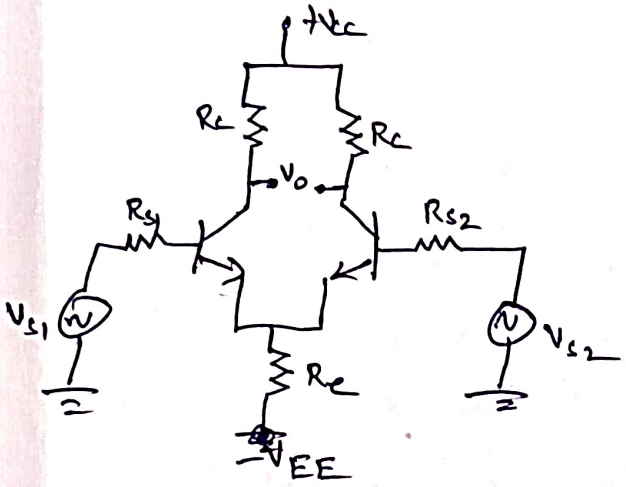


Fig-1

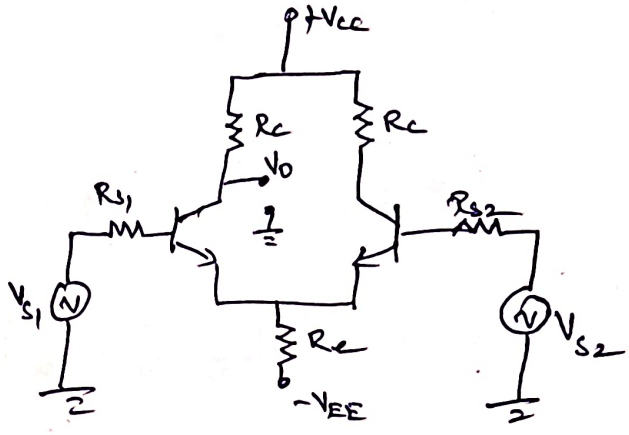


Fig-2

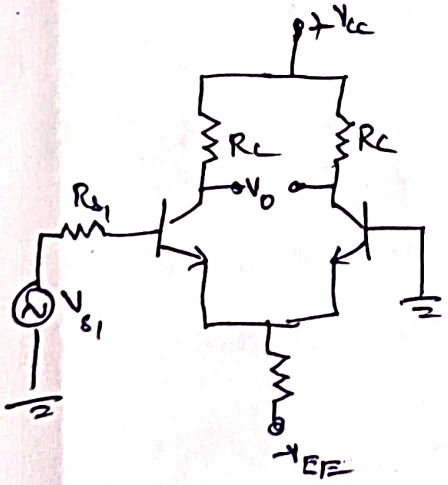
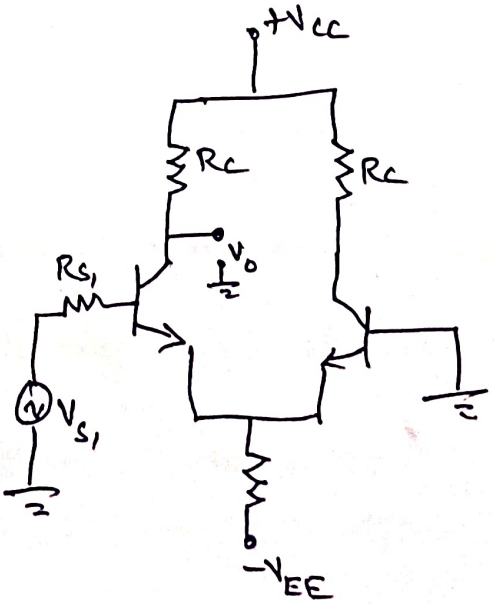


Fig-3



Non-Ideal Characteristics of Differential Amplifier:-

A diff. amplifier ideally amplifies only the difference b/w two I/p signals. In practise, it shows several non-ideal char. The main ones are explained below,

① DC - Errors & Biasing:

(a) I/p offset volt. (V_{os}): A small volt. needed at the I/p to make the o/p zero when I/p should be identical.

(b) I/p Bias current: (I_B)

Average current flowing into the input terminals.

(c) I/p offset current: (I_{os})

Difference b/w the bias currents of the two I/p. (i.e; $I_{os} = |I_{B1} - I_{B2}|$).

(d) Total output offset voltage:

The overall DC error at the o/p, influenced by V_{os}, I_B & I_{os}.

② Gain & Rejection Errors:-

(a) Finite open-loop Gain: Actual gain isn't infinite, causing gain errors, especially in closed-loop systems.

(b) Finite common-mode Rejection Ratio (CMRR):

The amplifier doesn't perfectly reject unwanted common-mode signals, leading to common-mode gain Errors.

③ Frequency & Transient Issues:-

*Slew Rate: The maxi. rate of change of the o/p volt, Limiting Large signal bandwidth.

* Frequency-Dependent Gain & Impedance: Gain and I/p & o/p impedances vary with freq, Introducing phase shift and Limiting bandwidth.

④ Impedances Issues:-

* Finite I/p Impedance. (Real I/p draw some ct, affecting R_L)

* Non-Zero o/p Impedance (Reducing gain)

⑤ Other nonidealities:-

* o/p volt / current Limits: o/p exceed power supply rails (sat.) or provide infinite ct.

* Noise (random signal generated by amplifier)

* Nonlinearity / Distortion: o/p is not perfectly proportional to I/p.

— x —