SREENIVASA INSTITUTE OF TECHNOLOGY AND MANAGEMENT STUDIES
(AUTONOMOUS)

QUESTION BANK

Year / Semester: III B.Tech VI Semester **Regulation: R23**

Subject and Code: VLSI DESIGN – 23ECE363T

SYLLABUS

UNIT 1 - INTRODUCTION TO IC TECHNOLOGY & ELECTRICAL PROPERTIES (9)
Introduction: Brief Introduction to IC technology MOS, PMOS, NMOS, CMOS & BiCMOS Technologies. Basic Electrical Properties of MOS and BiCMOS Circuits: IDS - VDS relationships, MOS transistor Threshold Voltage, figure of merit, Transconductance, Pass transistor, NMOS Inverter, Various pull ups, CMOS Inverter analysis and design, Bi-CMOS Inverters

UNIT 2 - VLSI CIRCUIT DESIGN PROCESSES (9)
VLSI Circuit Design Processes: VLSI Design Flow, MOS Layers, Stick Diagrams, Design Rules and Layout, Lambda(λ)-based design rules for wires, contacts and Transistors, Layout Diagrams for NMOS and CMOS Inverters and Gates, Scaling of MOS circuits, Limitations of Scaling.

UNIT 3 - GATE LEVEL DESIGN & BASIC CIRCUIT CONCEPTS (9)
Gate level Design: Logic gates and other complex gates, Switch logic, Alternate gate circuits. Basic Circuit Concepts: Sheet Resistance Rs and its concepts to MOS, Area Capacitances calculations, Inverter Delays, Driving large Capacitive Loads, Wiring Capacitances, Fan-in and fan-out

UNIT 4 - SUBSYSTEM DESIGN & VLSI DESIGN STYLES (9)
Subsystem Design: Shifters, Adders, ALUs, Multipliers, Parity generators, Comparators, Counters. VLSI Design styles: Full-custom, Standard Cells, Gate-arrays, FPGAs, CPLDs and Design Approach for Full-custom and Semi-custom devices, parameters influencing low power design.

UNIT 5 - CMOS TESTING (9)
CMOS Testing: Need for testing, Design for testability - built in self-test (BIST) – testing combinational logic –testing sequential logic – practical design for test guidelines – scan design techniques.

Prepared by Dr.S.Vijay Kumar, Mrs.R.Anitha, Mrs.K.Yasmin

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Max Marks: 10

S.No.	CO	Questions	BT
Unit I: (Introduction to IC Technology & Electrical Properties)			
1	**1**	a. Explain MOS, PMOS, NMOS and CMOS technologies. b. Compare MOS and BiCMOS technologies.	**L4**
2	**1**	Explain IDS–VDS characteristics of MOS transistor.	**L3**
3	**1**	Describe threshold voltage and transconductance of MOSFET.	**L4**
4	**1**	Explain figure of merit of MOS transistor.	**L3**
5	**1**	Analyse the operation of NMOS inverter with diagram	**L5**
6	**1**	Explain CMOS inverter operation and its advantages	**L4**
7	**1**	Discuss various pull-up configurations in MOS circuits.	**L3**
8	**1**	Evaluate CMOS inverter performance parameters.	**L5**
9	**1**	Explain pass transistor logic and its limitations.	**L4**
10	**1**	Describe Bi-CMOS inverter with circuit diagram.	**L3**
11	**1**	Compare NMOS, CMOS and BiCMOS inverters.	**L3**

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S.No.	CO	Questions	BT
Unit II: (VLSI Circuit Design Processes)			
1	**2**	Explain the VLSI design flow and discuss MOS layers used in fabrication.	**L4**
2	**2**	Explain stick diagrams and their significance	**L3**
3	**2**	Describe lambda-based design rules.	**L4**
4	**2**	Explain layout design rules for contacts and wires.	**L3**
5	**2**	Evaluate scaling issues in VLSI technology.	**L5**
6	**2**	Explain layout diagrams for NMOS inverters.	**L4**
7	**2**	Explain layout diagrams for CMOS gates.	**L3**
8	**2**	Analyse limitations of scaling in VLSI.	**L5**
9	**2**	Explain fabrication steps of MOS circuits.	**L4**
10	**2**	Discuss design rule checking and verification.	**L3**
11	**2**	Explain advantages of stick diagram before layout.	**L4**

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S.No.	CO	Questions	BT
Unit III: (Unit Name)			
1	**3**	a.Explain switch logic implementation of gates and alternate gate circuits.	**L4**
2	**3**	Explain sheet resistance concept in MOS circuits.	**L3**
3	**3**	Describe area capacitance and its effects.	**L4**
4	**3**	Explain wiring capacitances in VLSI circuits.	**L3**
5	**3**	Evaluate delay in CMOS inverter.	**L5**
6	**3**	Explain methods to drive large capacitive loads.	**L4**
7	**3**	Explain fan-in and fan-out effects in digital circuits.	**L3**
8	**3**	Analyse propagation delay in MOS circuits.	**L5**
9	**3**	Explain RC delay model for interconnects.	**L4**
10	**3**	Discuss power dissipation in CMOS circuits.	**L3**
11	**3**	Compare static and dynamic performance of CMOS.	**L3**

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S.No.	CO	Questions	BT
Unit IV: (Subsystem Design & VLSI Design Styles**)**			
1	**4**	Explain shifter circuits and parity generators.	**L4**
2	**4**	Explain CMOS adder circuits.	**L3**
3	**4**	Describe multiplier architecture in VLSI.	**L4**
4	**4**	Explain comparator circuits with diagram.	**L3**
5	**4**	Evaluate ALU design considerations.	**L5**
6	**4**	Explain different counter implementations.	**L4**
7	**4**	Discuss full-custom design methodology.	**L3**
8	**4**	Analyse standard cell design approach	**L5**
9	**4**	Explain FPGA and CPLD based design.	**L4**
10	**4**	Discuss gate-array based design approach.	**L3**
11	**4**	Explain low power design parameters.	**L3**

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S.No.	CO	Questions	BT
Unit V: (CMOS Testing)			
1	**5**	Explain need for testing in VLSI and fault models.	**L4**
2	**5**	Explain design for testability concepts	**L3**
3	**5**	Describe Built-In Self Test (BIST).	**L4**
4	**5**	Explain testing of combinational logic.	**L3**
5	**5**	Evaluate sequential circuit testing methods.	**L5**
6	**5**	Explain scan design techniques.	**L4**
7	**5**	Discuss test pattern generation methods.	**L3**
8	**5**	Analyse fault coverage metrics.	**L5**
9	**5**	Explain boundary scan testing.	**L4**
10	**5**	Discuss practical test guidelines.	**L3**
11	**5**	Explain advantages of DFT techniques.	**L3**

RememberingUnderstandingApplyingAnalyzingEvaluatingCreating