UNIT-I

IC Technologies

- Introduction

- MOS

- PMOS

- NMOS

- CMOS

    &

- BiCMOS

    Technologies

BasicElectricalPropertiesof MOS and BiCMOS Circuits

- I_{DS}-V_{DS}relationships
- MOS transistor Threshold Voltage - V_T figure of merit-$\omega 0$
- Transconductance-g_m,g_{ds};
- Passtransistor
- NMOS Inverter, Various pull ups, CMOS Inverter analysis and design
- Bi-CMOSInverters

INTRODUCTIONTOICTECHNOLOGY

The development of electronics endless with invention of vaccum tubes and associated electronic circuits. This activity termed as vaccum tube electronics, afterward the evolution of solid state devices and consequent development of integrated circuits are responsible for the present status of communication, computing and instrumentation.

• Thefirstvaccumtubediodewasinventedby**johnambraseFleming**in1904.

• Thevaccumtriodewas inventedby**leedeforest**in1906.

Earlydevelopments oftheIntegratedCircuit(IC) gobackto1949.Germanengineer Werner Jacobi filed a patent for an IC likesemiconductoramplifyingdeviceshowingfive transistorsonacommonsubstrateina2-stageamplifierarrangement. Jacobi disclosed small cheap of hearing aids.

Integrated circuits were made possible by experimental discoveries which showed that semiconductor devices could perform the functions of vacuum tubes and by mid-20th-century technology advancements in semiconductor device fabrication.

The integration of large numbers of tiny transistors into a small chip was an enormous improvement over the manual assembly of circuits using electronic components.

The integrated circuits mass production capability, reliability, and building-block approach to circuit design ensured the rapid adoption of standardized ICs in place of designs using discrete transistors.

An integrated circuit (IC) is a small semiconductor-based electronic device consisting of fabricated transistors, resistors and capacitors. Integrated circuits are the building blocks of most electronic devices and equipment. An integrated circuit is also known as a chip or microchip.

There are two main advantages of ICs over discrete circuits: cost and performance. Cost islow because the chips, with all their components, are printed as a unit by photolithography ratherthan beingconstructedonetransistor at atime. Furthermore, much lessmaterialis used to construct a packaged IC die than a discrete circuit. Performance is high since the components switch quicklyand consume little power (compared to their discrete counterparts) because the components are small and positioned close together. As of 2006, chip areas range from a few square millimeters to around 350 mm^2, with up to 1 million transistors per mm

ICInvention:

Inventor	Year	Circuit	Remark
Fleming	1904 1906	Vacuumtubediode Vacuumtriode	largeexpensive,power-hungry, unreliable
WilliamShockley (Bell labs)	1945	Semiconductorreplacing vacuum tube	--
Bardeen and Brattain and Shockley(Belllabs)	1947	Point Contact transfer resistancedevice"BJT"	Drivingfactorofgrowthof the VLSI technology
WernerJacobi(SiemensAG)	1949	1stICcontainingamplifying Device 2stage amplifier	Nocommercialusereported
Shockley	1951	JunctionTransistor	"Practicalformof transistor"
Jack Kilby (Texas Instruments)	July 1958	Integrated Circuits F/F With2-TGermaniumslice and gold wires	FatherofICdesign
NoyceFairchild Semiconductor	Dec.1958	IntegratedCircuitsSilicon	"TheMayorofSilicon Valley"
KahngBellLab	1960	FirstMOSFET	Start of new era for semiconductorindustry
FairchildSemic onductorAnd Texas	1061	FirstCommercial IC	
FrankWanlass (Fairchild Semiconductor)	1963	CMOS	
FedericoFaggin (Fairchild Semiconductor)	1968	SilicongateICtechnology	Later Joined Intel to lead firstCPUIntel4004in1970 2300T on 9mm^2
Zarlink Semiconductors	Recently	M2Acapsulefor endoscopy	takephotographsof digestivetract2/sec.

Moore'sLaw:

- GordonE.Moore-ChairmanEmeritusofIntelCorporation
- 1965-observedtrendsinindustry-oftransistorson ICsvsreleasedates
- Noticednumberoftransistorsdoublingwithreleaseofeachnew IC generation
- Releasedates(separategenerations)wereall18-24monthsapart

"Thenumberoftransistorsonanintegratedcircuitwilldoubleevery18months"

ThelevelofintegrationofsilicontechnologyasmeasuredintermsofnumberofdevicesperIC Semiconductor industry has followed this prediction with surprising accuracy.
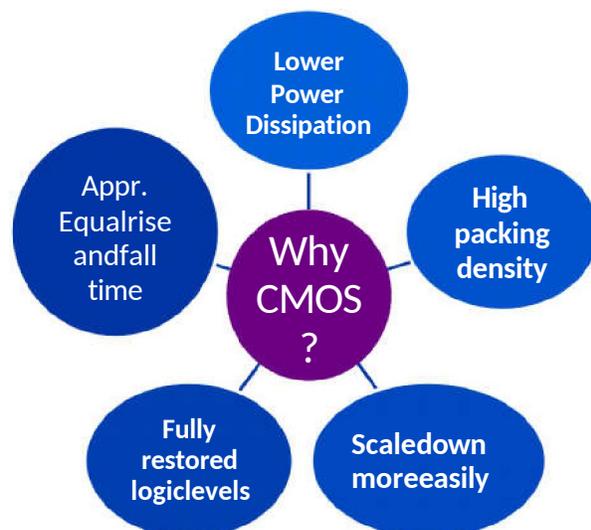
ICTechnology:

- Speed/Powerperformanceofavailabletechnologies
- Themicroelectronicsevolution
- SIARoadmap
- SemiconductorManufacturers2001Ranking

CircuitTechnology

ICTechnology

| Bipolar | CMOS | BiCMOS | SOI | SiGe | GaAs |
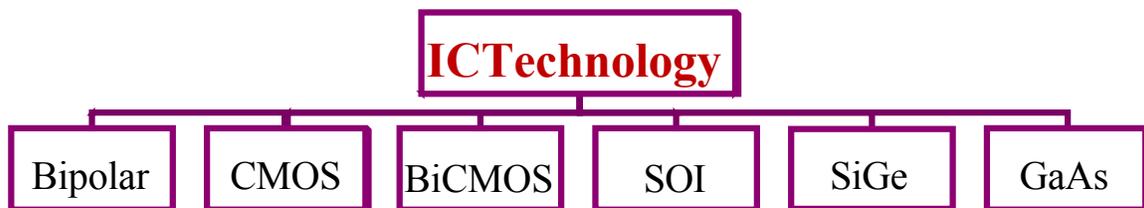
Category	BJT	CMOS
Power Dissipation	Moderate toHigh	less
Speed	Faster	Fast
Gm	4ms	0.4ms
Switch implementation	poor	Good
Technology improvement	slower	Faster

Why CMOS ?
- Lower Power Dissipation
- High packing density
- Scaledown moreeasily
- Fully restored logiclevels
- Appr. Equalrise andfall time

ScaleofIntegration:

- **Smallscaleintegration(SSI)--1960**

    Thetechnologywasdevelopedbyintegratingthenumberoftransistorsof1-100 on a

    single chip. Ex: Gates, flip-flops, op-amps.

- **Mediumscaleintegration(MSI)--1967**

    Thetechnologywasdevelopedbyintegratingthenumberoftransistorsof100- 1000on

    a singlechip. Ex: Counters, MUX, adders, 4-bit microprocessors.

- **Largescaleintegration(LSI)--1972**

    Thetechnologywasdevelopedbyintegratingthenumberoftransistorsof1000- 10000

    on a single chip. Ex:8-bit microprocessors,ROM,RAM.

- **Verylargescaleintegration(VLSI)-1978**

    Thetechnologywasdevelopedbyintegratingthenumberoftransistorsof10000-

    1Million on a single chip. Ex:16-32 bit microprocessors, peripherals,

    complimentaryhigh MOS.

- **Ultralargescaleintegration(ULSI)**

    Thetechnologywasdevelopedbyintegratingthenumberoftransistorsof1Million- 10

    Millions on a single chip. Ex: special purpose processors.

- **Giantscaleintegration(GSI)**

    Thetechnologywasdevelopedbyintegratingthenumberoftransistorsofabove10 Millions on a

    single chip. Ex: Embedded system, system on chip.

- ✓ Fabricationtechnologyhasadvancedtothepointthatwecanputacompletesystemona single chip.
- ✓ SinglechipcomputercanincludeaCPU,bus,I/Odevices and memory.
- ✓ This reduces the manufacturing cost than the equivalent   boardlevel   systemwithhigher performance and lower power.

MOSTECHNOLOGY:

MOS technologyis considered as one of the veryimportant and promisingtechnologies in the VLSI design process. The circuit designs are realized based on pMOS, nMOS, CMOS and BiCMOSdevices.

The pMOS devices are based on the p-channel MOS transistors. Specifically,thepMOS channel is part of a n-type substrate lying between two heavily doped p+ wells beneath thesource and drain electrodes. Generally speaking, a pMOS transistor is only constructed inconsort with an NMOS transistor.

The nMOS technology and design processes provide an excellent background for other technologies. In particular, some familiarity with nMOS allows a relatively easy transition to CMOS technology and design.

The techniques employed in nMOS technology for logic design are similar to GaAs technology.. Therefore, understanding the basics of nMOS design will help in the layout of GaAs circuits

In addition to VLSI technology, the VLSI design processes also provides a new degree of freedom for designers which helps for the significant developments. With the rapid advances in technology the the size of the ICs is shrinking and the integration density is increasing. Theminimumlinewidthofcommercialproducts overthe yearsisshowninthegraph below.
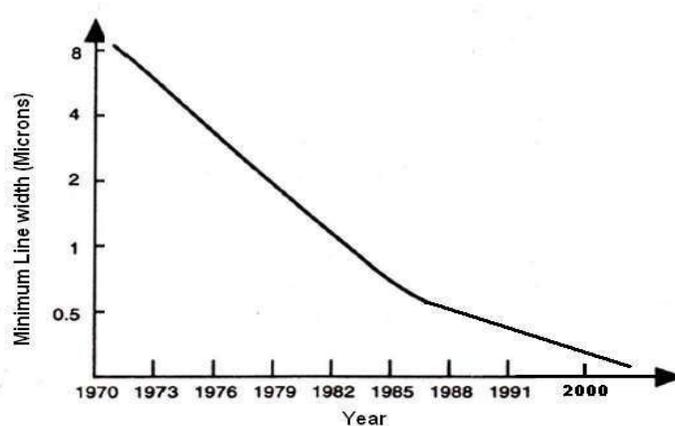
Thegraphshowsasignificantdecreaseinthesizeofthechipinrecentyearswhichimplicitly indicates the advancements in the VLSI technology.

MOSTransistorSymbol:
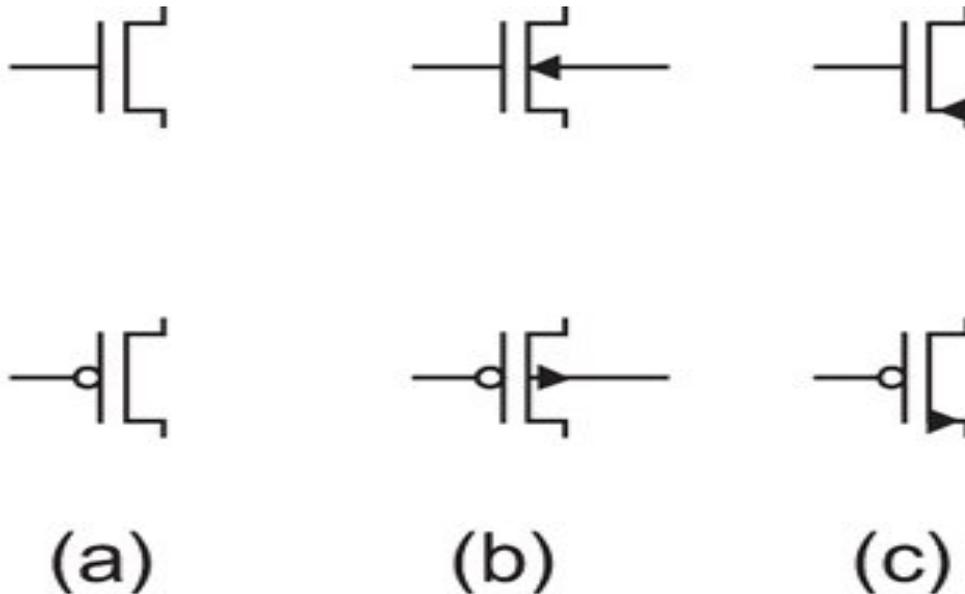
FIG 2.1 MOS transistor symbols

ENHANCEMENTANDDEPLETIONMODEMOSTRANSISTORS

MOS Transistors are built on a silicon substrate. Silicon which is a group IV material is the eighth most common element in the universe bymass, but veryrarelyoccurs as the pure free element in nature. It is most widely distributed in dusts, sands, planetoids, and planets as various forms of silicon dioxide (silica) or silicates. It forms crystal lattice with bonds to four neighbours. Silicon is a semiconductor. Pure silicon has no free carriers and conducts poorly. But adding dopants to silicon increases its conductivity. If a group V material i.e. an extra electron is added, it forms an n-type semiconductor. If a group III material i.e. missing electron pattern is formed (hole), the resulting semiconductor is called a p-type semiconductor.

A junction between p-type and n-type semiconductor forms a conduction path. Source and DrainoftheMetalOxideSemiconductor(MOS)Transistorisformedbythe"doped"regionsonthe

surface of chip. Oxide layer is formed by means of deposition of the silicon dioxide (SiO$_2$) layer which forms as an insulator and is a very thin pattern. Gate of the MOS transistor is the thin layer of "polysilicon (poly)"; used to apply electric field to the surface of silicon between Drain and Source,to form a "channel" of electrons or holes. Control by the Gate voltage is achieved by modulating the conductivity of the semiconductor region just below the gate. This region is known as the channel.

The Metal–Oxide–Semiconductor Field Effect Transistor (MOSFET) is a transistor which is a voltage-controlled current device, in which current at two electrodes, drain and source is controlledby the action of an electric field at another electrode gate having in-between semiconductor and a very thin metal oxide layer. It is used for amplifying or switching electronic signals.

The Enhancement and Depletion mode MOS transistors are further classified as N-type named NMOS (or N-channel MOS) and P-type named PMOS (or P-channel MOS) devices. Figure 1.5 shows the MOSFETs along with their enhancement and depletion modes.
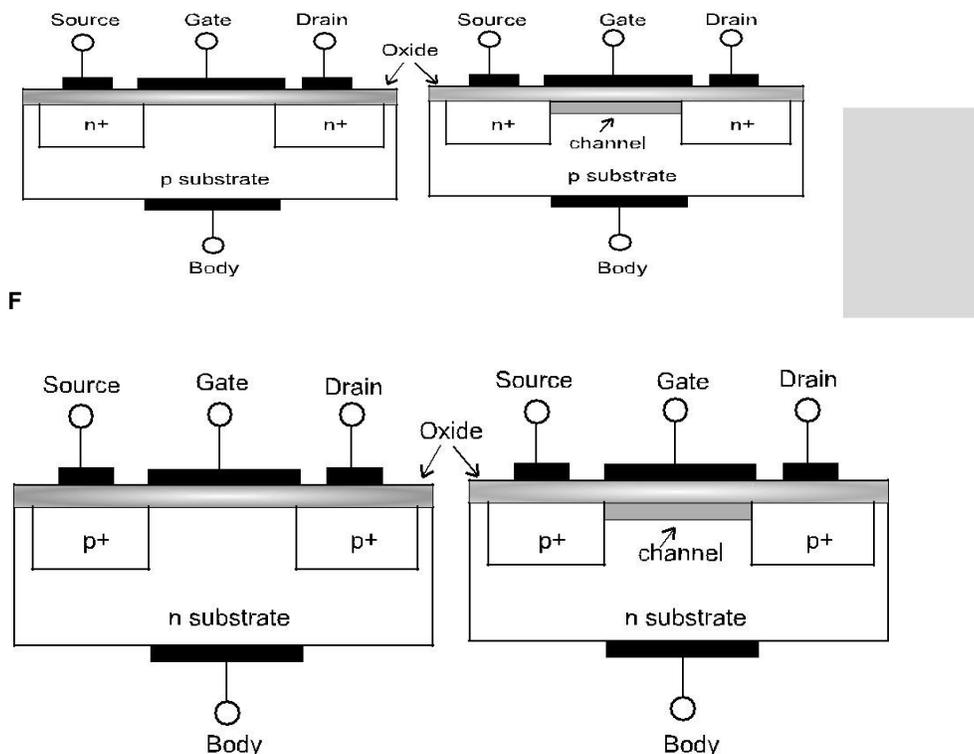
Figure1.5:(c)EnhancementP-typeMOSFET(d)DepletionP-typeMOSFET

The depletion mode devices are doped so that a channel exists even with zero voltage from gate to source during manufacturing of the device. Hence the channel always appears in the device. To controlthechannel,anegativevoltageisappliedtothegate(foranN-channeldevice),depletingthe

channel, which reduces the current flow through the device. In essence, the depletion-mode device is equivalent to a closed (ON) switch, while the enhancement-mode device does not have the built in channel and is equivalent to an open (OFF) switch. Due to the difficulty of turning off the depletion mode devices, they are rarely used

WorkingofEnhancementModeTransistor

Theenhancement mode devices donot havethein-built channel. Byapplyingtherequired potentials, the channel can be formed. Also for the MOS devices, there is a threshold voltage (V_t), below which not enough charges will be attracted for the channel to be formed. This threshold voltage for a MOS transistor is a function of doping levels and thickness of the oxide layer.

Case1:V_{gs}=0VandV_{gs}<V_t

Thedeviceisnon-conducting,whennogatevoltageisapplied(V_{gs}=0V)or(V_{gs}<V_t)andalsodrain to source potential V_{ds} = 0. With an insufficient voltage on the gate to establish the channel region as N-type, there will be no conduction between the source and drain. Since there is no conducting channel, there is no current drawn, i.e. I_{ds} = 0, and the device is said to be in the **cut-off region**. This is shown in the Figure 1.7 (a).
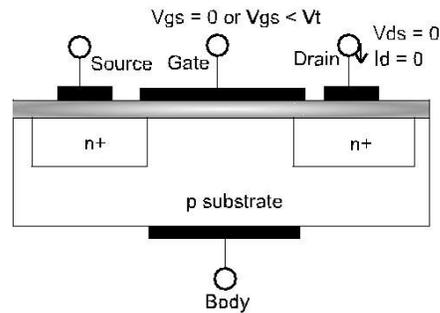
Figure1.7:(a)Cut-offRegion

Case2:Vgs>Vt

When a minixmum voltage greater than the threshold voltage V_t (i.e. V_{gs}> V_t) is applied, a high concentration of negative charge carriers forms an inversion layer located by a thin layer next to the interface between the semiconductor and the oxide insulator. This forms a channel between thesource and drain of the transistor. This is shown in the Figure 1.7 (b).
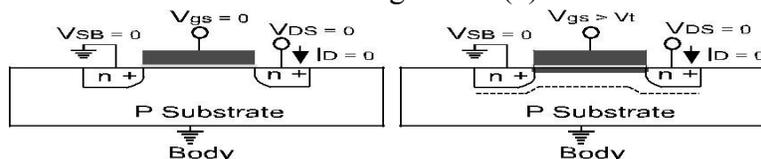

Figure1.7:(b)FormationofaChannel

A positive V_{ds} reverse biases the drain substrate junction, hence the depletion region around the drain widens, and since the drain is adjacent to the gate edge, the depletion region widens in the channel. This is shown in Figure 1.7 (c). This results in flow of electron from source to drainresulting in current Ids.. The device is said to operate in **linear region** during this phase. Further increase in $V_{ds,}$ increases the reverse bias on the drain substrate junction in contact with the inversion layer which causes inversion layer density to decrease. This is shown in Figure 1.7 (d). The point at which the inversion layer density becomes very small (nearly zero) at the drain end is termed pinch- off. The value of V_{ds} at pinch-off is denoted as $V_{ds,sat}$. This is termed as **saturation region** for the MOS device. Diffusion current completes the path from source to drain in this case, causing the channel to exhibit a high resistance and behaves as a constant current source.
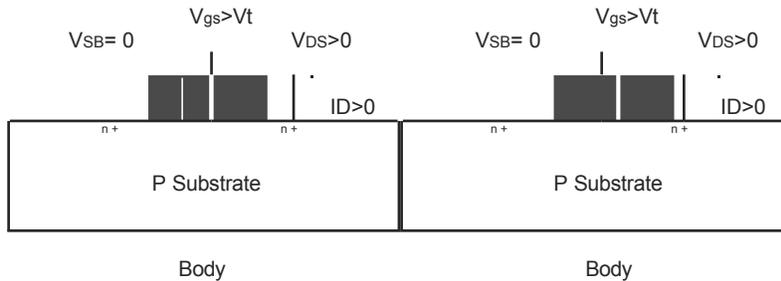
Figure1.7:(c)LinearRegion.(d)SaturationRegion

TheMOSFET$I_D$versusV_{DS}characteristics(V-ICharacteristics)isshownintheFigure1.8.ForV_{GS} $< V_t,$ $I_D = 0$ and device is in cut-off region. As V_{DS} increases at a fixed V_{GS}, I_D increases in the linear region due to the increased lateral field, but at a decreasing rate since the inversion layer density is decreasing. Once pinch-off is reached, further increase in V_{DS} results in increase in I_D; due to the formation of the high field region which is very small. The device starts in linear region, and moves into saturation region at higher V_{DS}.
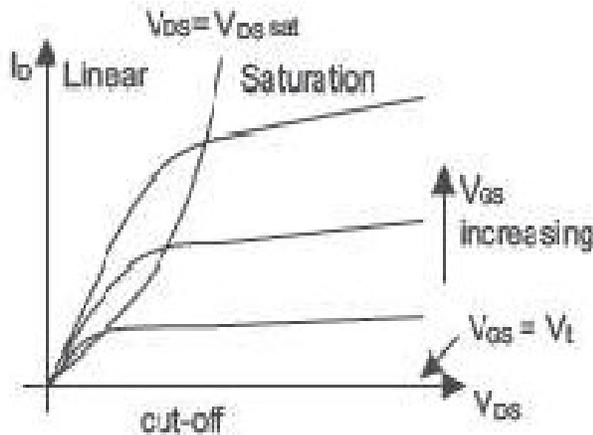

Figure 1.8: MOS V-I Characteristics

NMOSFABRICATION

Thefollowingdescriptionexplainsthebasicstepsusedintheprocessoffabrication.

(a) Thefabricationprocessstartswiththeoxidationofthesiliconsubstrate. It is

shown in the Figure 1.9 (a).

(b) Arelativelythicksilicondioxidelayer,alsocalledfieldoxide,iscreatedonthesurfaceofthe substrate.

This is shown in the Figure 1.9 (b).

(c) Then,thefieldoxideisselectivelyetchedtoexposethesiliconsurfaceonwhichtheMOS transistor will

be created. This is indicated in the Figure 1.9 (c).

(d) This is followed by covering the surface of substrate with a thin, high-quality oxide layer, which

will eventually form the gate oxide of the

MOStransistorasillustratedinFigure1.9(d).

(e) On top of the thin oxide, a layer of polysilicon(polycrystallinesilicon)is deposited as is shown in

the Figure 1.9 (e). Polysilicon is used both as gate electrode material for MOS transistors and also as

an interconnect medium in silicon integrated circuits. Undoped polysilicon has relatively high

resistivity. The resistivity of polysilicon can be reduced, however, by doping it with impurity atoms.

(f) After deposition, the polysilicon layer is patterned and etched to form the interconnects and the

MOS transistor gates. This is shown in Figure 1.9 (f).

(g) The thin gate oxide not covered by polysilicon is also etched along, which exposes the bare

silicon surface on which the source and drain junctions are to be formed (Figure 1.9 (g)).

(h) The entire silicon surface is then doped with high concentration of impurities, either through

diffusion or ion implantation (in this case with donor atoms to produce n-type doping). Diffusion is

achieved byheatingthe waferto ahightemperature andpassingthe gascontainingdesiredimpurities over

the surface. Figure 1.9 (h) shows that the doping penetrates the exposed areas on the silicon surface,

ultimately creating two n-type regions (source and drain junctions) in the p-type substrate. The

impurity doping also penetrates the polysilicon on the surface, reducing its resistivity.

(i) Once the source and drain regions are completed, the entire surface is again covered with an

insulating layer of silicon dioxide, as shown in

Figure 1.9 (i).(*j*) The insulating oxide layer is then patterned in order to provide contact windows for

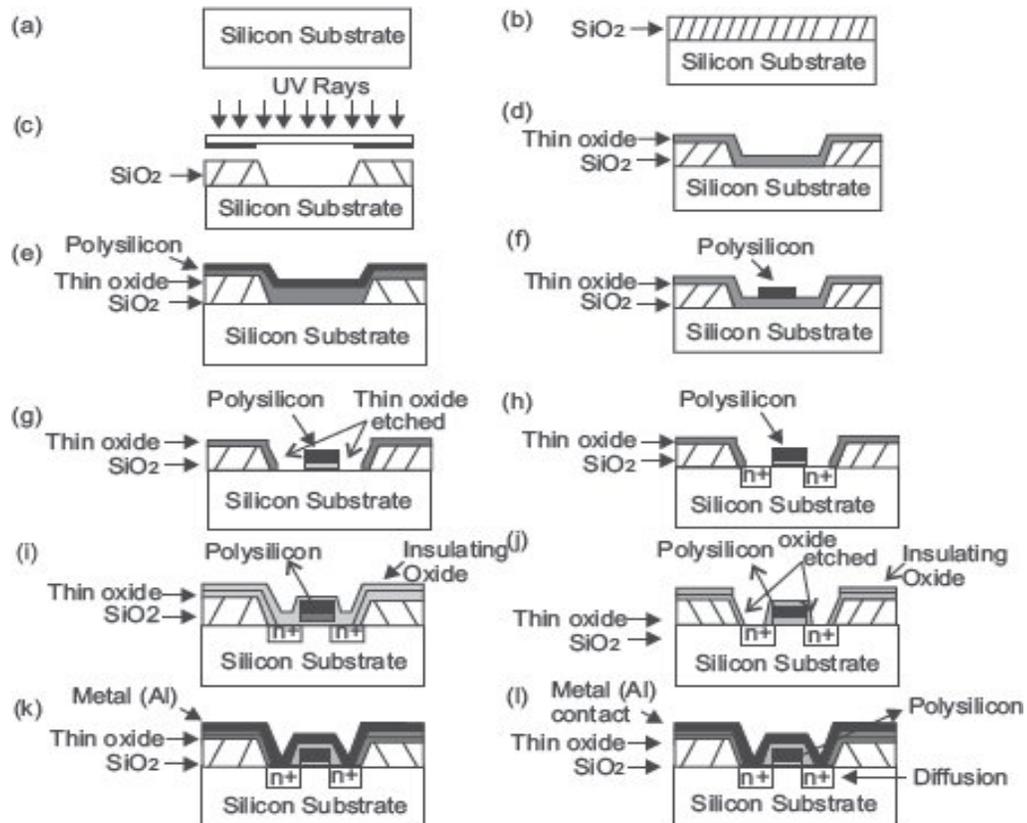the drain and source junctions, as illustrated in Figure 1.9 (j).

Figure 1.9: Fabrication Process of NMOS Device

CMOSFABRICATION:

CMOSfabricationcanbeaccomplishedusingeitherofthethreetechnologies:

- • N-welltechnologies/P-welltechnologies
- • Twinwelltechnology
- • SiliconOnInsulator(SOI)

The fabrication of CMOS can be done by following the below shown twenty steps, by which CMOS can be obtained byintegrating both the NMOS and PMOS transistors on the same chip substrate. For integrating these NMOS and PMOS devices on the same chip, special regions called as wells or tubs are required in which semiconductor type and substrate type are opposite to each other.

A P-well has to be created on a N-substrate or N-well has to be created on a P-substrate. In this article, the fabrication of CMOS is described using the P-substrate, in which the NMOS transistor is fabricated on a P-type substrate and the PMOS transistor is fabricated in N-well.

Thefabricationprocessinvolvestwentysteps,whichareas follows:

N-WellProcess

Step1: Substrate

Primarily,starttheprocesswithaP-substrate.

Step2: Oxidation

Theoxidationprocessisdonebyusinghigh-purityoxygen andhydrogen,whichareexposedinan oxidation furnace approximately at 1000 degree centigrade.

Step3: Photoresist

Alight-sensitivepolymerthatsoftenswheneverexposedtolightiscalledasPhotoresistlayer.

Itis formed.
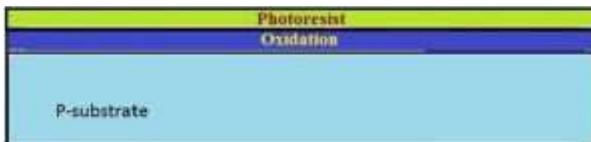
Step4: Masking

ThephotoresistisexposedtoUVraysthroughtheN-wellmask
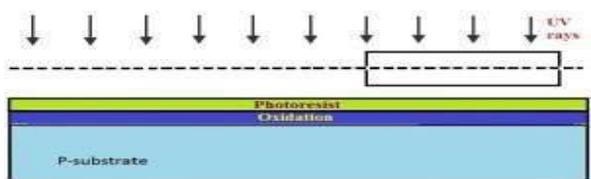
Step5:Photoresistremoval

Apartofthephotoresistlayerisremovedbytreatingthewaferwiththebasicoracidicsolution.
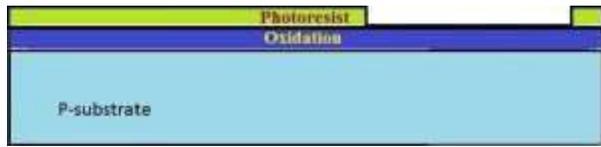
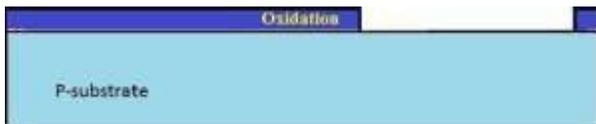## Step6:RemovalofSiO2usingacid etching

TheSiO2oxidationlayer isremovedthroughtheopenareamadebytheremovalofphotoresistusing hydrofluoric acid.

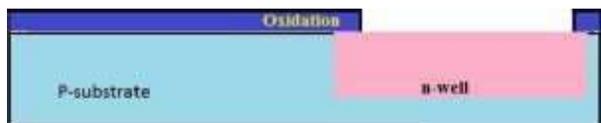## Step7:Removalof photoresist

Theentirephotoresistlayer isstrippedoff,asshowninthebelow figure.

Step8:FormationoftheN-well

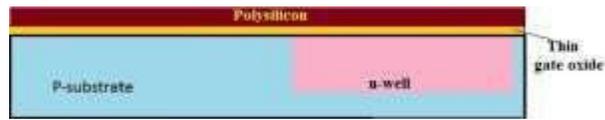ByusingionimplantationordiffusionprocessN-wellisformed.

Step9:RemovalofSiO2

Usingthehydrofluoricacid,theremainingSiO2is removed.

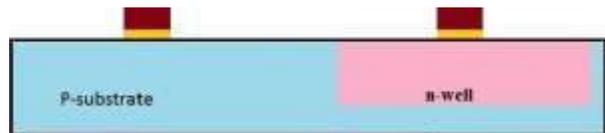## Step10:Depositionofpolysilicon

ChemicalVaporDeposition(CVD)processisusedtodepositaverythinlayer ofgateoxide.

Step11:RemovingthelayerbarringasmallareafortheGates

Exceptthetwosmallregionsrequiredforformingthe GatesofNMOSandPMOS,theremaining layer is stripped off.

Step12:Oxidationprocess
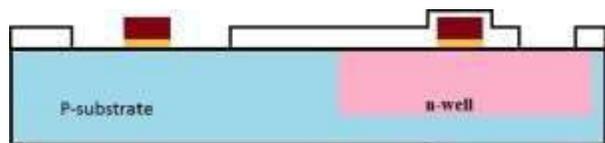
Next,anoxidationlayerisformedonthislayerwithtwosmallregionsfortheformationofthegate terminals of NMOS and PMOS.
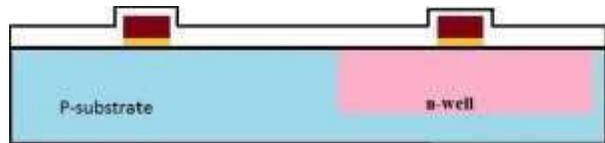
Step13:MaskingandN-diffusion

Byusingthemaskingprocesssmall gapsaremadefor thepurposeofN-diffusion.

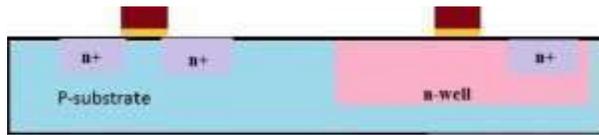Then-type(n+)dopants arediffusedorionimplanted,andthethreen+areformedfortheformation of the terminals of NMOS.
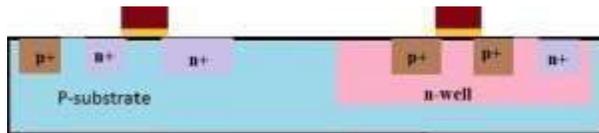

Step14:Oxide stripping

The remaining oxidation layer is stripped off.

Step15:P-diffusion

Similar to the above N-diffusion process, the P-diffusion regions are diffused to form the terminals of the PMOS.

Step16:Thick field oxide

A thick-field oxide is formed in all regions except the terminals of the PMOS and NMOS.

Step17: Metallization

Aluminum is sputtered on the whole wafer.

Step18:Removal of excess metal

The excess metal is removed from the wafer layer.
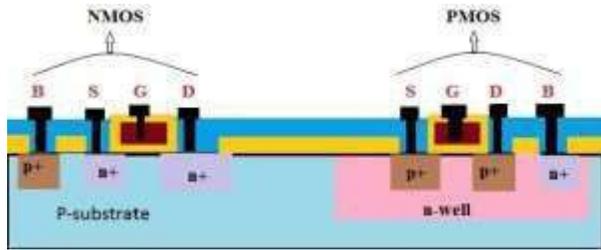

Step19: Terminals

The terminals of the PMOS and NMOS are made from respective gaps.

Step20:Assigning the names of the terminals of the NMOS and PMOS

FabricationofCMOSusingP-wellprocess

Among all the fabrication processes of the CMOS, N-well process is mostly used for the fabrication of the CMOS. P-well process is almost similar to the N-well. But the only difference in p-well process is that it consists of a main N-substrate and, thus, P-wells itself acts as substrate for the N-devices.

Twintub-CMOSFabricationProcess
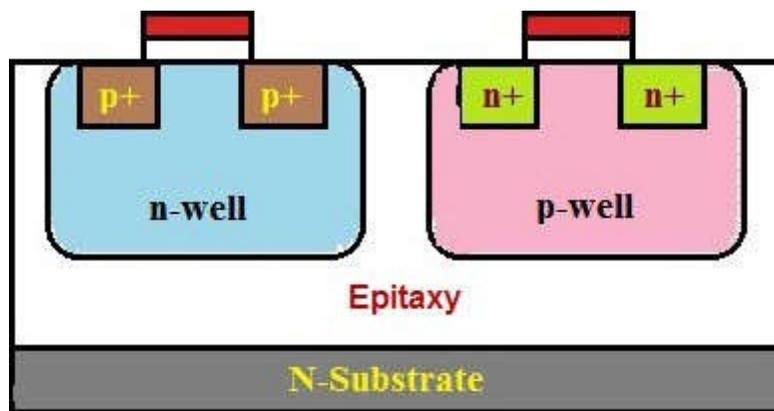
In this process, separate optimization of then-type and p-type transistorswill be provided. The independent optimization of Vt, body effect and gain of the P-devices, N-devices can be made possible with this process.

DifferentstepsofthefabricationoftheCMOSusingthetwintubprocessareasfollows:

- Lightlydopedn+orp+substrateistakenand,toprotectthelatchup, epitaxiallayerisused.
- Thehigh-puritycontrolledthicknessofthelayersofsiliconaregrownwithexactdopant concentrations.
- ThedopantanditsconcentrationinSiliconareusedtodetermineelectrical properties.
- Formationofthetub
- Thin oxide construction

- Implantationofthesourceanddrain
- Cutsformakingcontacts
- Metallization

Byusingtheabovesteps wecan fabricateCMOSusingtwintubprocessmethod.

Silicon-on-Insulator(SOI)CMOSProcess

Rather than using silicon as the substrate material, technologists have sought to use an insulating substrate to improve process characteristics such as speed and latch-up susceptibility. The SOI CMOS technology allows the creation of independent, completely isolated nMOS and pMOS transistors virtually side-by-side on an insulating substrate. The main advantages of this technology arethehigherintegration density(becauseoftheabsenceofwellregions), completeavoidanceofthe latch-up problem, and lower parasiticcapacitances compared to the conventional p &n-well or twin- tub CMOS processes. A cross-section of nMOS and pMOS devicesusingSOI processis shownbelow.
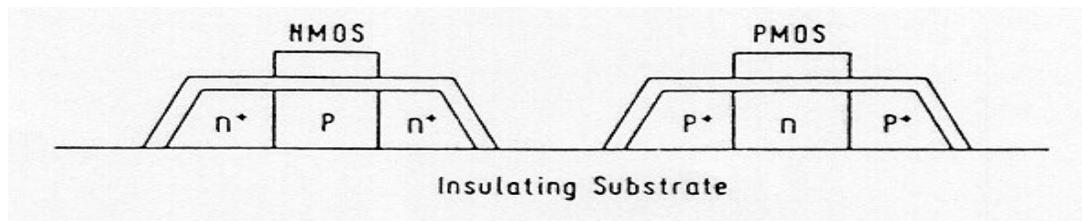
TheSOICMOSprocess isconsiderablymorecostlythanthestandardp&n-wellCMOSprocess. Yet the improvements of device performance and the absence of latch-up problems can justifyits use, especially for deep-sub-micron devices.

BasicElectricalPropertiesofMOSandBiCMOScircuits

I_D-V_{DS}CharacteristicsofMOSTransistor:

The graph below shows the ID Vs VDS characteristics of an n- MOS transistor for several values of VGS .It is clear that there are two conduction states when the device is ON. The saturated state and the non-saturated state. The saturated curve is the flat portion and defines the saturation region. For Vgs < VDS + Vth, the nMOS device is conducting and ID is independent of VDS. For Vgs > VDS + Vth,thetransistor is in thenon-saturation region and the curve is a half parabola. Whenthe transistor is OFF (Vgs < Vth), then ID is zero for any VDS value.
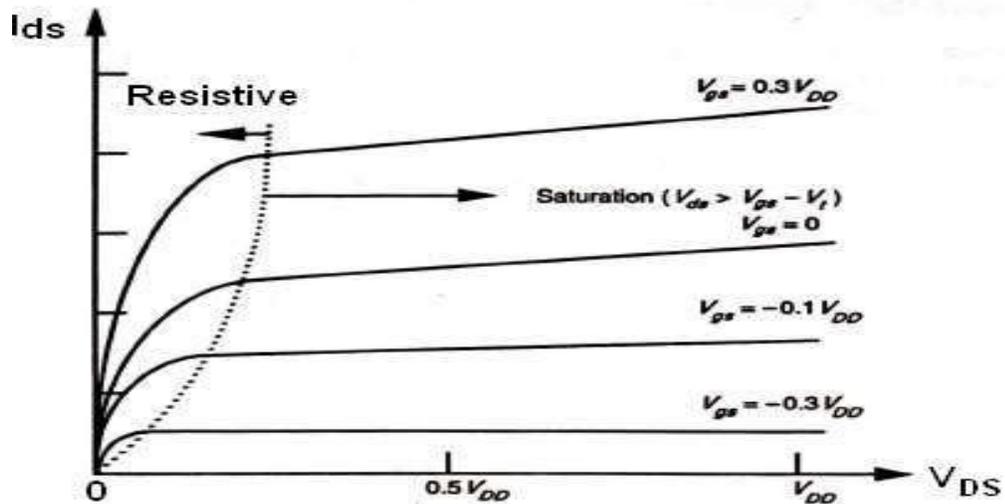

(a) Depletion mode device

Theboundaryofthesaturation/non-saturationbiasstatesisapointseenforeach curveinthegraphas the intersection of the straight line of the saturated region with the quadratic curve ofthe non- saturated region. This intersection point occurs at the channel pinch off voltage called VDSAT. The diamond symbol marks the pinch-off voltage VDSAT for each value of VGS. VDSAT is defined as theminimumdrain-sourcevoltagethatis requiredtokeepthetransistorinsaturationfora given VGS .In the non-saturated state, the drain current initially increases almost linearly from the origin before bending in a parabolic response. Thus the name ohmic or linear for the non- saturated region. ThedraincurrentinsaturationisvirtuallyindependentofVDSandthetransistoractsasacurrent

source. This is because there is no carrier inversion at the drain region of the channel. Carriers are pulled into the high electric field of the drain/substrate pn junction and ejected out of the drain terminal.
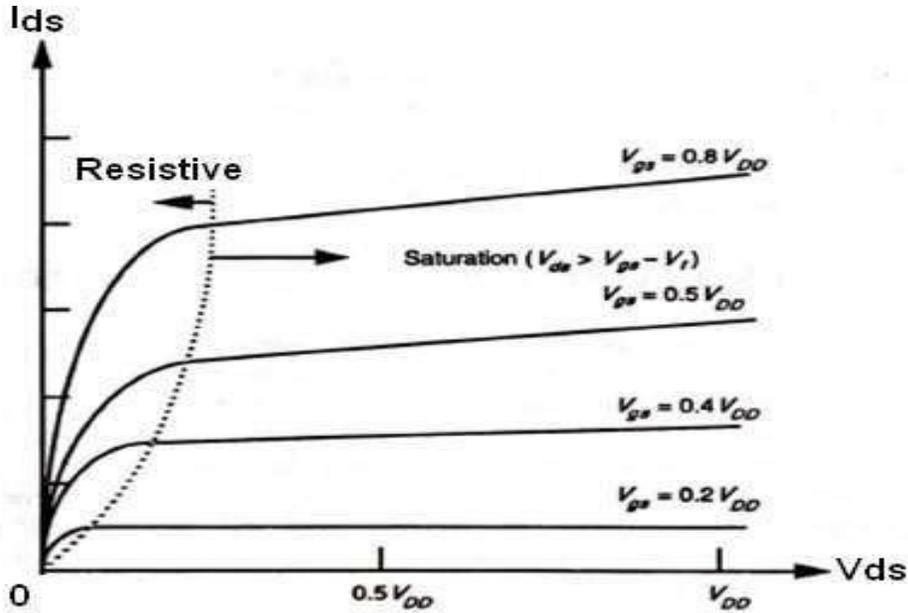

(b). Enhance mode device

Drain-to-SourceCurrentI$_{DS}$VersusVoltageV$_{DS}$Relationships:

Theworkingof a MOS transistoris based on the principle that the useof a voltage on the gate induce a charge in the channel between source and drain, which maythen be caused to move from source to drain under the influence of an electric field created by voltage Vds applied between drain andsource.SincethechargeinducedisdependentonthegatetosourcevoltageVgsthen   Idsisdependent on both Vgs and Vds.

Let us consider the diagram below in which electrons will flow source to drain .So,the drain currentis given by

Charge induced in channel(Qc) Ids =-Isd= Electron transit time(τ) Length of the channel Where the transit time is given byτsd=------------------------------
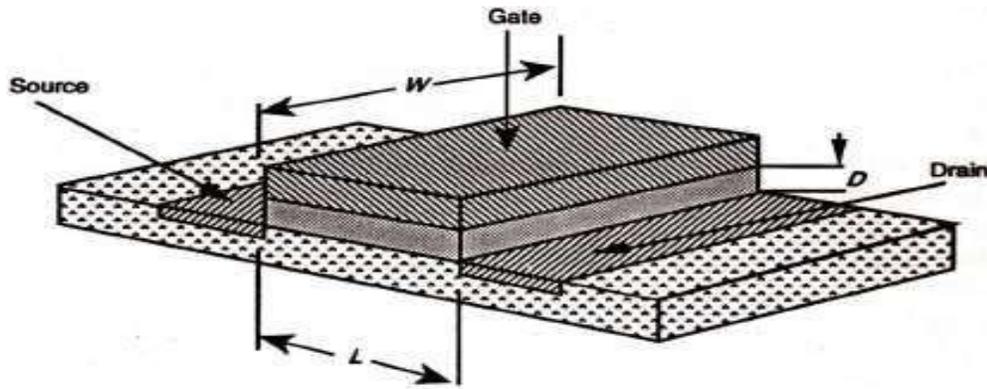
Velocity (v)

Butvelocityv=μEds

Whereμ=electronorholemobilityand　　　　Eds=Electricfieldalso,Eds=Vds/L

so,v=μ.Vds/Landτds=L^2/μ.Vds

Thetypicalvaluesofμatroomtemperaturearegiven below.

$$\mu_n \doteq 650 \ cm^2/V \ sec \ (surface)$$
$$\mu_p \doteq 240 \ cm^2/V \ sec \ (surface)$$

Non-saturatedRegion:

Let us consider theIdvsVdrelationships in the non-saturated region .The charge induced in the channel due to due to the voltage difference between the gate and the channel, Vgs (assuming substrateconnected to source).Thevoltagealongthechannel varies linearlywithdistance*X*from the source due to the IR drop in the channel .In the non-saturated state the average value is Vds/2. Also the effective gate voltage Vg = Vgs – Vt where Vt, is the threshold voltage needed to invert the charge under the gate and establish the channel.

HencetheinducedchargeisQc=EgεinsεoW.L Where

Eg=averageelectricfieldgatetochannel

εins=relativepermittivityofinsulationbetweengateandchannel εo=permittivity

$$E_g = \frac{\left((V_{gs} - V_t) - \frac{V_{ds}}{2} \right)}{D}$$

Here D is the thickness of the oxide layer. Thus

$$Q_c = \frac{WL\varepsilon_{ins}\varepsilon_0}{D}\left((V_{gs} - V_t) - \frac{V_{ds}}{2}\right)$$

So, by combining the above two equations, we get

$$I_{ds} = \frac{\varepsilon_{ins}\varepsilon_0\mu}{D}\frac{W}{L}\left((V_{gs} - V_t) - \frac{V_{ds}}{2}\right)V_{ds}$$

or the above equation can be written as

$$I_{ds} = K\frac{W}{L}\left((V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right)$$

In the non-saturated or resistive region where Vds < Vgs – Vt and

$$K = \frac{\varepsilon_{ins}\varepsilon_0\mu}{D}$$

Generally, a constant β is defined as

$$\beta = K\frac{W}{L}$$

So that, the expression for drain–source current will become

$$I_{ds} = \beta\left((V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right)$$

The gate/channel capacitance is

$$C_g = \frac{\varepsilon_{ins}\varepsilon_0 WL}{D} \text{ (parallel plate)}$$

Hencewecanwriteanotheralternativeformforthedraincurrentas

$$I_{ds} = \frac{C_g \mu}{L^2} \left((V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2} \right)$$

Sometimeitisalsoconvenienttousegate–capacitanceperunitarea,CgSo,thedraincurrentis

$$I_{ds} = C_0 \mu \frac{W}{L} \left((V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2} \right)$$

Thisistherelationbetweendraincurrentanddrain-sourcevoltageinnon-saturatedregion.

SaturatedRegion

Saturation begins when Vds = Vgs - V, since at this point the IR drop in the channel equals the effective gate to channel voltage at the drain and we may assume that the current remains fairly constant as Vds increases further. Thus

$$I_{ds} = K \frac{W}{L} \frac{(V_{gs} - V_t)^2}{2}$$

orwecanalsowritethat

$$I_{ds} = \frac{\beta}{2} (V_{gs} - V_t)^2$$

oritcanalsobewrittenas

$$I_{ds} = \frac{C_g \mu}{2L^2} (V_{gs} - V_t)^2$$

or

$$I_{ds} = C_0 \mu \frac{W}{2L} (V_{gs} - V_t)^2$$

The expressions derived above for I_{ds} hold for both enhancement and depletion mode devices. Here the threshold voltage for the nMOS depletion mode device (denoted as V_{td}) is negative.

MOSTransistorThresholdVoltageVt:

The gate structure of a MOS transistor consists, of charges stored in the dielectric layers and in the surface to surface interfaces as well as in the substrate itself. Switching an enhancement mode MOS transistor from the off to the on state consists in applying sufficient gate voltage to neutralize these charges and enable the underlying silicon to undergo an inversion due to the electric field from the gate. Switching a depletion mode nMOS transistor from the on to the off state consists in applying enough voltage to the gate to add to the stored charge and invert the 'n' implant region to 'p'.

ThethresholdvoltageVtmaybeexpressedas:

$$V_t = \phi_{ms} \frac{Q_B - Q_{SS}}{C_0} + 2\phi_{fN}$$

where   QD=thechargeper unit areain thedepletion layerbelowtheoxideQss=chargedensityat Si:

SiO2 interface

C0=Capacitanceperunitarea.

Φns=workfunctiondifferencebetweengateandSi

ΦfN=FermilevelpotentialbetweeninvertedsurfaceandbulkSi

For polynomial gate and silicon substrate, the value of Φns is negative but negligible and the magnitude and sign of Vt are thus determined by balancing the other terms in the equation. To evaluate the Vt the other terms are determined as below.

$$Q_B = \sqrt{2\varepsilon_0 \varepsilon_{Si} qN(2\phi_{fN} + V_{SB})} \text{ coulomb/m}^2$$

$$\phi_{fN} = \frac{kT}{q} \ln \frac{N}{n_i} \text{ volts}$$

$$Q_{SS} = (1.5 \text{ to } 8) \times 10^{-8} \text{ coulomb/m}^2$$

BodyEffect:

Generallywhile studying the MOS transistorsit is treated as a three terminal device. But, the body of the transistor is also an implicit terminal which helps to understand the characteristics of the transistor. Considering the bodyof the MOS transistor as a terminal is known as the bodyeffect. The potential difference between the source and the body (Vsb) affects the threshold

voltage of the transistor. In many situations, this Body Effect is relatively insignificant, so we can (unless **otherwise** stated) ignore the Body Effect. But it is not always insignificant, in some cases it can have a tremendous impact on MOSFET circuit performance.
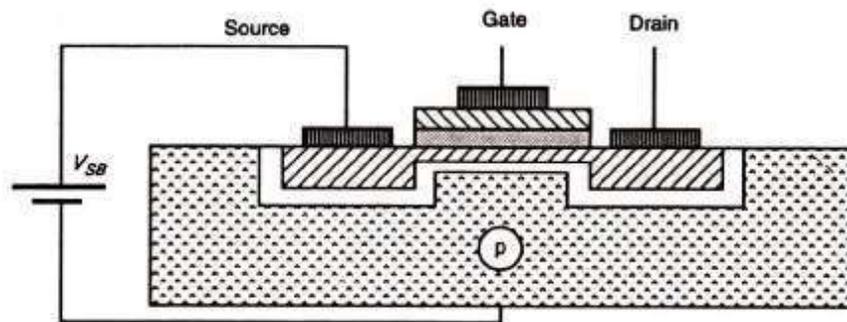
Bodyeffect-nMOSdevice

Increasing Vsb causes the channel to be depleted of charge carriers and thus the threshold voltage is raised.ChangeinVt is givenby$\Delta Vt=\gamma.(Vsb)^{1/2}$ whereγisaconstantwhichdependsonsubstrate doping so that the more lightly doped the substrate, the smaller will be the bodyeffect

Thethresholdvoltagecanbewrittenas

$$V_t = V_t(0) + \left(\frac{D}{\varepsilon_{ins}\varepsilon_0}\right)\sqrt{2\varepsilon_0\varepsilon_{Si}QN}.(V_{SB})^{1/2}$$

Where$Vt(0)$isthethresholdvoltagefor$V_{sd}=0$

For n-MOS depletion mode transistors ,the body voltage values at different V$_{DD}$ voltages are given below.

V$_{SB}$ = 0 V ; Vsd = -0.7V$_{DD}$ (= - 3.5 V for V$_{DD}$ =+5V) V$_{SB}$ = 5 V ; Vsd = -0.6V$_{DD}$ (= - 3.0 V for V$_{DD}$ =+5V)

nMOSINVERTER:

An inverter circuit is a veryimportant circuit for producing a complete range of logic circuits. This is needed for restoring logic levels, for Nand and Nor gates, and for sequential and memory circuits of various forms .

A simple inverter circuit can be constructed using a transistor with source connected to ground and a load resistor of connected from the drain to the positive supply rail VDD· The output is taken from the drain and the input applied between gate and ground .

But, during the fabrication resistors are not conveniently produced on the silicon substrate and even small values of resistors occupy excessively large areas .Hence some other form of load resistance is used. A more convenient way to solve this problem is to use a depletion mode transistor as the load, as shown in Fig. below.
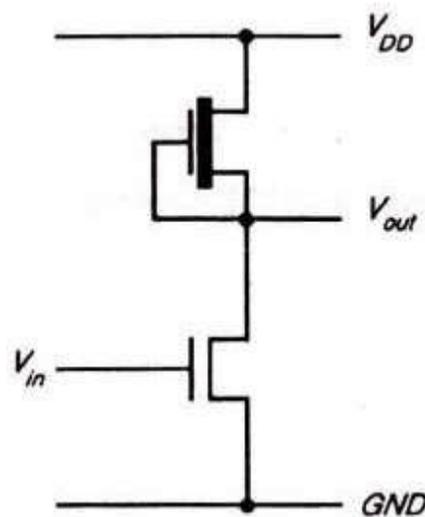

Thesalientfeaturesofthen-MOSinverterare

- Forthedepletionmodetransistor,thegateisconnectedtothesourcesoitisalwayson .
- In thisconfigurationthedepletionmodedeviceis calledthepull-up(P.U)andtheenhancement mode device the pull-down (P.D) transistor.
- Withnocurrentdrawnfromtheoutput,thecurrentsIdsforbothtransistorsmustbeequal.

nMOSInvertertransfercharacteristic.

The transfer characteristic is drawn by taking Vds on x-axis and Ids on Y-axis for both enhancement and depletion mode transistors. So,to obtain the inverter transfer characteristic for

Vgs = 0 depletion mode characteristic curve is superimposed on the family of curves for the enhancement mode device and from the graph it can be seen that , maximum voltage across the enhancement mode device corresponds to minimum voltage across the depletion mode transistor.
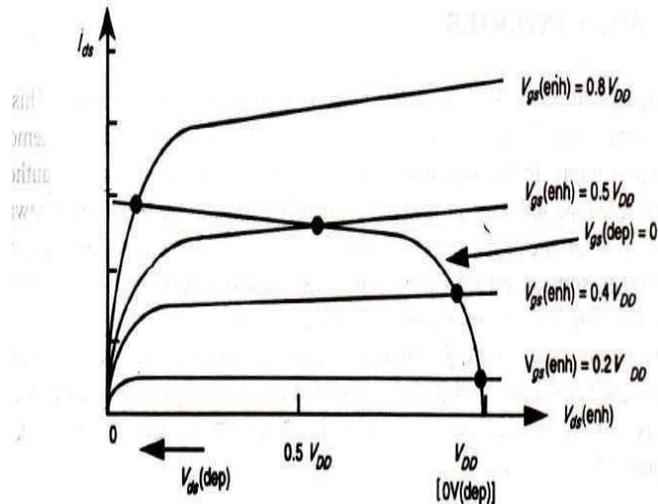
From the graph it is clear that as Vin(=Vgs p.d. transistor) exceeds the Pulldown threshold voltage current begins to flow. The output voltage Vout thus decreases and the subsequent increases in Vin will cause the Pull down transistor to come out of saturation and become resistive.

CMOSInverter:

The inverter is the very important part of all digital designs. Once its operation and properties are clearly understood, Complex structures like NAND gates, adders, multipliers, and microprocessors can also be easily done. The electrical behavior of these complex circuits can be almost completely derivedbyextrapolatingtheresultsobtained forinverters.Asshowninthe diagrambelowtheCMOS transistor is designed using p-MOS and n-MOS transistors.
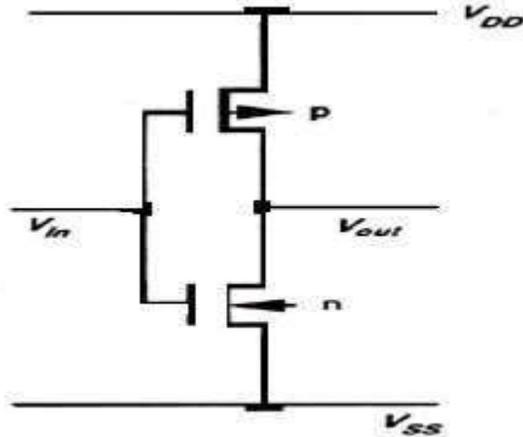
In the inverter circuit ,if the input is high .the lower n-MOS device closes to discharge the capacitive load.Similarly,iftheinputislow,thetopp-MOSdeviceisturnedontochargethecapacitiveload

.At no time both the devices are on ,which prevents the DC current flowing from positive power supply to ground. Qualitatively this circuit acts like the switching circuit, since the p-channel transistor has exactly the opposite characteristics of the n-channel transistor. In the transition region both transistors are saturated and the circuit operates with a large voltage gain. The C-MOS transfer characteristic is shown in the below graph.

Considering the static conditions first, it may be Seen that in region 1 for which Vi,. = logic 0, we have the p-transistor fully turned on while the n-transistor is fully turned off. Thus no current flows through the inverter and the output is directly connected to VDD through thep-transistor.
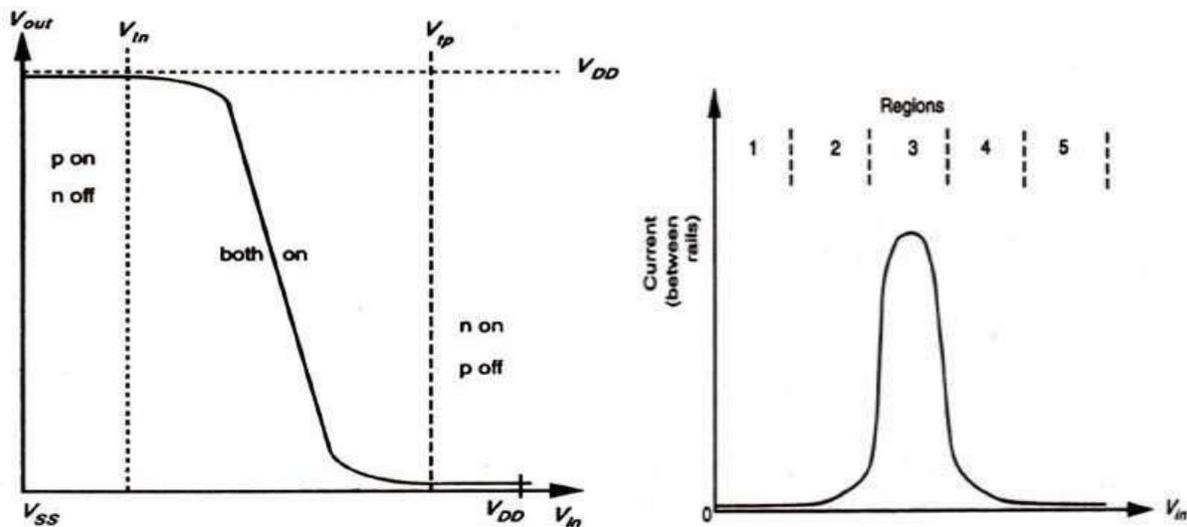
Hence the output voltage is logic 1 . In region 5 , Vin = logic 1 and the n-transistor is fully on while the p-transistor is fully off. So, no current flows and logic 0 appears at the output.

In region 2 the input voltage has increased to a level which just exceeds the threshold voltage of the n-transistor. The n-transistor conducts and has a large voltage between source and drain; so it is in saturation. The p-transistor is also conducting but with only a small voltage across it, it operates intheunsaturatedresistiveregion.AsmallcurrentnowflowsthroughtheinverterfromVDDtoVSS. If we wish to analyze the behavior in this region, we equate the p-device resistive region current with the n-device saturation current and thus obtain the voltage and current relationships.

Region 4 is similar to region 2 but with the roles of the p- and n-transistors reversed.However, the current magnitudes in regions 2 and 4 are small and most of the energy consumed in switching from one state to the other is due to the larger current which flows in region3.

Region 3 is the region in which the inverter exhibits gain and in which both transistors are in saturation.

Thecurrentsineachdevicemustbethesame,sincethetransistorsareinseries.So,wecanwritethat

$$I_{dsp} = - I_{dsn}$$

where

$$I_{dsp} = \frac{\beta_p}{2} (V_{in} - V_{DD} - V_{tp})^2$$

and

$$I_{dsn} = \frac{\beta_n}{2} (V_{in} - V_{tn})^2$$

Sincebothtransistorsarein saturation, theyact as current sources so that theequivalent circuit in this region is two current sources in series between VDD and Vss with the output voltage coming from their common point. The region is inherently unstable in consequence and the changeover from one logic level to the other is rapid.

Determination of Pull-up to Pull –Down Ratio *(Zp.u}Zp.d.)*for an nMOS Inverter driven by another nMOS Inverter :

Let us consider the arrangement shown in Fig.(a). in which an inverter is driven from the output of another similar inverter. Consider the depletion mode transistor for which Vgs = 0 under all conditions, and also assume that in order to cascade inverters without degradation the condition
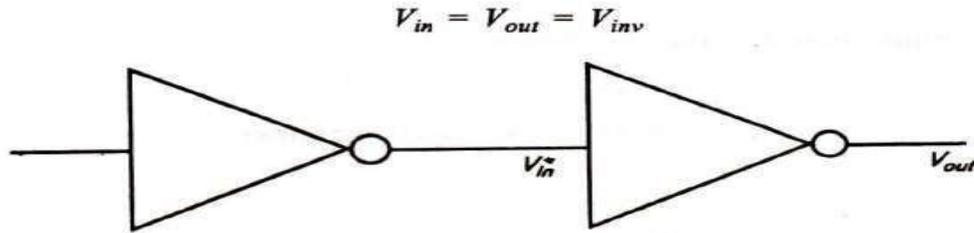
$$V_{in} = V_{out} = V_{inv}$$

Fig.(a).Inverterdrivenbyanotherinverter.

Forequalmarginsaroundtheinverterthreshold,wesetVinv=0.5VDD·Atthispointboth transistors are in saturation and we can write that

$$I_{ds} = K \frac{W}{L} \frac{(V_{gs} - V_t)^2}{2}$$

In the depletion mode $\quad I_{ds} = K \frac{W_{p.u.}}{L_{p.u.}} \frac{(-V_{td})^2}{2} \quad$ since $V_{gs} = 0$

and in the enhancement mode

$$I_{ds} = K \frac{W_{p.d.}}{L_{p.d.}} \frac{(V_{inv} - V_t)^2}{2} \quad \text{since } V_{gs} = V_{inv}$$

Equating (since currents are the same) we have

$$\frac{W_{p.d.}}{L_{p.d.}} (V_{inv} - V_t)^2 = \frac{W_{p.u.}}{L_{p.u.}} (-V_{td})^2$$

whereWp.d,Lp.d,Wp.u.andLp.uarethewidthsandlengthsofthepull-downandpull-up transistors respectively.

So,wecanwritethat

$$Z_{p.d.} = \frac{L_{p.d.}}{W_{p.d.}}; \; Z_{p.u.} = \frac{L_{p.u.}}{W_{p.u.}}$$

we have

$$\frac{1}{Z_{p.d.}} (V_{inv} - V_t)^2 = \frac{1}{Z_{p.u.}} (-V_{td})^2$$

whence

$$V_{inv} = V_t - \frac{V_{td}}{\sqrt{Z_{p.u.}/Z_{p.d.}}}$$

Thetypical,valuesforVt,VinvandVtdare

$$V_t = 0.2V_{DD}; \quad V_{td} = -0.6V_{DD}$$
$$V_{inv} = 0.5V_{DD} \text{ (for equal margins)}$$

Substitutingthesevaluesintheaboveequation,weget

$$0.5 = 0.2 + \frac{0.6}{\sqrt{Z_{p.u.}/Z_{p.d.}}}$$

Here

$$\sqrt{Z_{p.u.}/Z_{p.d.}} = 2$$

So,weget

$$\boxed{Z_{p.u.}/Z_{p.d.} = 4/1}$$

Thisistheratioforpull-uptopulldownratioforaninverterdirectlydrivenbyanotherinverter.

Pull-UptoPull-DownratioforannMOSInverterdriventhroughoneormorePass Transistors

Letusconsideranarrangementinwhichtheinputtoinverter2comesfromtheoutputofinverter1

butpassesthroughoneormorenMOStransistorsasshowninFig.below(Thesetransistorsarecalled   pass transistors).
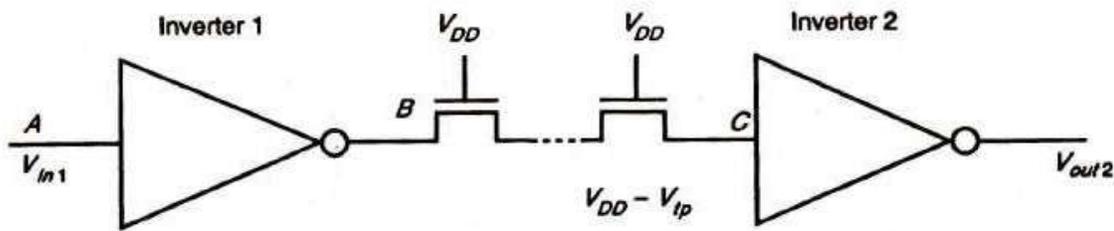
The connection of pass transistors in series will degrade the logic 1 level / into inverter 2 so that the output will not be a proper logic 0 level. The critical condition is , when point A is at 0 volts and B is thus at VDD. but the voltage into inverter 2at point C is now reduced from VDD by the threshold voltage of the series pass transistor. With all passtransistor gates connected to VDD there is a lossof Vtp, however many are connected in series, since no static current flows through them and there can be no voltage drop in the channels. Therefore, the input voltage to inverter 2 is

Vin2=VDD-VtpwhereVtp=thresholdvoltageforapasstransistor.

Let us consider the inverter 1 shown in Fig.(a) with input = VDD· If the input is at VDD , then the pull-down transistor T2 is conducting but with a low voltage across it; therefore, it is in its resistive region represented byR1 in Fig.(a)below. Meanwhile,thepull uptransistorT1is in saturation andis represented as a current source.

Forthepulldowntransistor

$$R_1 = \frac{V_{ds1}}{I_{ds}} = \frac{1}{K} \frac{L_{p.d.1}}{W_{p.d.1}} \left(\frac{1}{V_{DD} - V_t - \frac{V_{ds1}}{2}} \right)$$

$$I_{ds} = K \frac{W_{p.d.1}}{L_{p.d.1}} \left((V_{DD} - V_t) V_{ds1} - \frac{V_{ds1}^2}{2} \right)$$

SinceVdsissmall,Vds/2canbeneglectedintheaboveexpression.

(a) Inverter 1 with input = V_{DD} (b) Inverter 2 with input = $V_{DD} - V_{tp}$
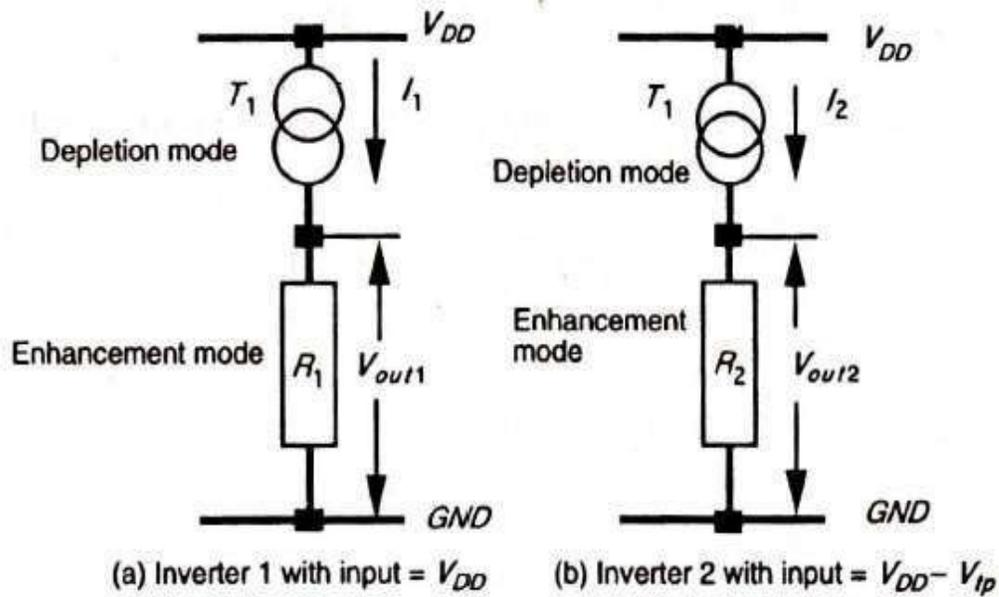
So,

$$R_1 \doteq \frac{1}{K} Z_{p.d.1} \left(\frac{1}{V_{DD} - V_t} \right)$$

Now, for depletion mode pull-up transistor in saturation with Vgs = 0

$$I_1 = I_{ds} = K \frac{W_{p.u.1}}{L_{p.u.1}} \frac{(-V_{td})^2}{2}$$

The product $1R1 = Vout1$ So,

$$V_{out1} = I_1 R_1 = \frac{Z_{p.d.1}}{Z_{p.u.1}} \left(\frac{1}{V_{DD} - V_t} \right) \frac{(V_{td})^2}{2}$$

Let us now consider the inverter 2 Fig.b. when input = $V_{DD} - V_{tp}$.

$$R_2 \doteq \frac{1}{K} Z_{p.d.2} \frac{1}{((V_{DD} - V_{tp}) - V_t}$$

$$I_2 = K \frac{1}{Z_{p.u.2}} \frac{(-V_{td})^2}{2}$$

Whence,

$$V_{out\,2} = I_2 R_2 = \frac{Z_{p.d.2}}{Z_{p.u.2}} \left(\frac{1}{V_{DD} - V_{tp} - V_t} \right) \frac{(-V_{td})^2}{2}$$

Ifinverter2istohavethesameoutputvoltageundertheseconditionsthenV_{out1}=V_{out2}.Thatis

I_1R_1=I_2R_2 , therefore

$$\frac{Z_{p.u.2}}{Z_{p.d.2}} = \frac{Z_{p.u.1}}{Z_{p.d.1}} \frac{(V_{DD} - V_t)}{(V_{DD} - V_{tp} - V_t)}$$

Consideringthetypical values

$$V_t = 0.2 V_{DD}$$
$$V_{tp} = 0.3 V_{DD}*$$

$$\frac{Z_{p.u.2}}{Z_{p.d.2}} = \frac{Z_{p.u.1}}{Z_{p.d.1}} \frac{0.8}{0.2}$$

Therefore

$$\frac{Z_{p.u.2}}{Z_{p.d.2}} \doteq 2 \frac{Z_{p.u.1}}{Z_{p.d.1}} = \frac{8}{1}$$

Fromtheabovetheoryit isclearthat,forann-MOS transistor

(i). An inverter driven directly from the output of another should have a $Z_{p.u}/Z_{pd.}$ ratio of $\geq$ 4/1.

(ii).AninverterdriventhroughoneormorepasstransistorsshouldhaveaZp.u./Zp.dratioof $\geq 8/1$

ALTERMTIVEFORMSOFPULL–UP

Generally the inverter circuit will have a depletion mode pull-up transistor as its load. But there are also other configurations .Let us consider four such arrangements.

(i).Load resistance RL : This arrangement consists of a load resistor as apull-up as shown in the diagram below.But it is not widely used because of the large space requirements of resistorsproduced in a silicon substrate.
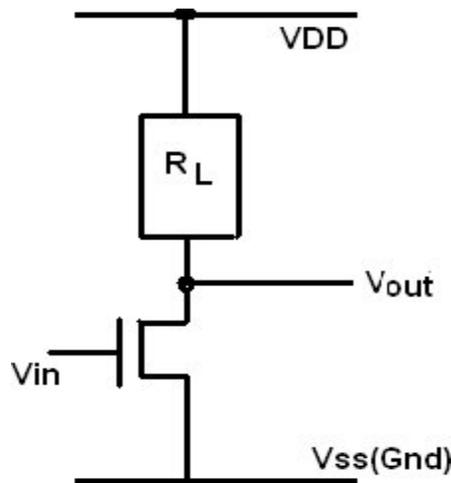
nMOS depletion mode transistor pull-up : This arrangement consists of a depletion mode transistoraspull-up.Thearrangementandthetransfercharacteristicareshownbelow.Inthistype of arrangement we observe
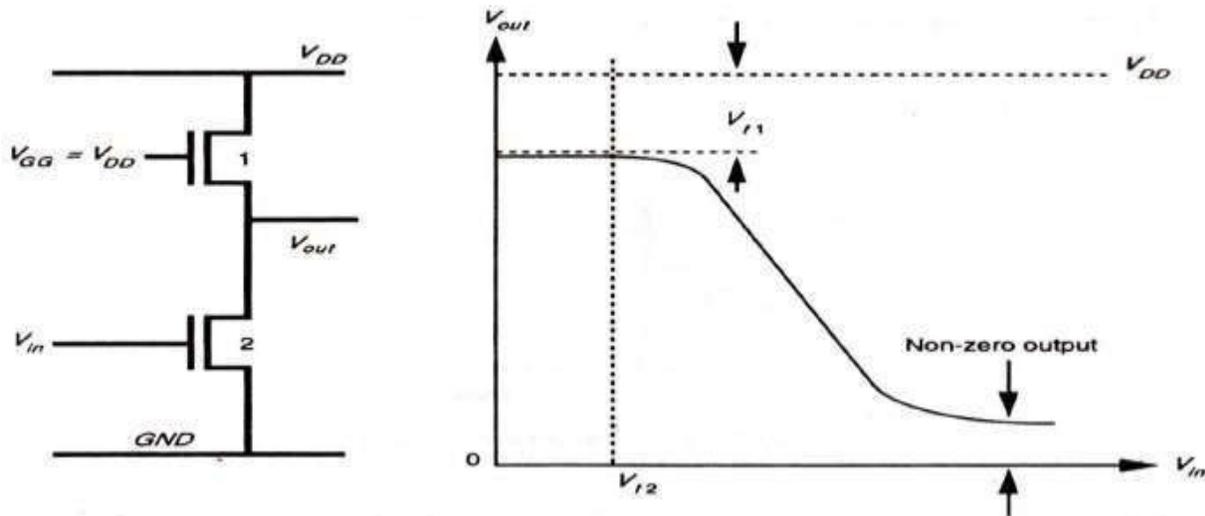
(a) Dissipationishigh,sincerailtorailcurrentflows whenVin=logical 1.

(b) Switchingofoutputfrom 1to0beginswhenVin exceedsVt,ofpull-downdevice.
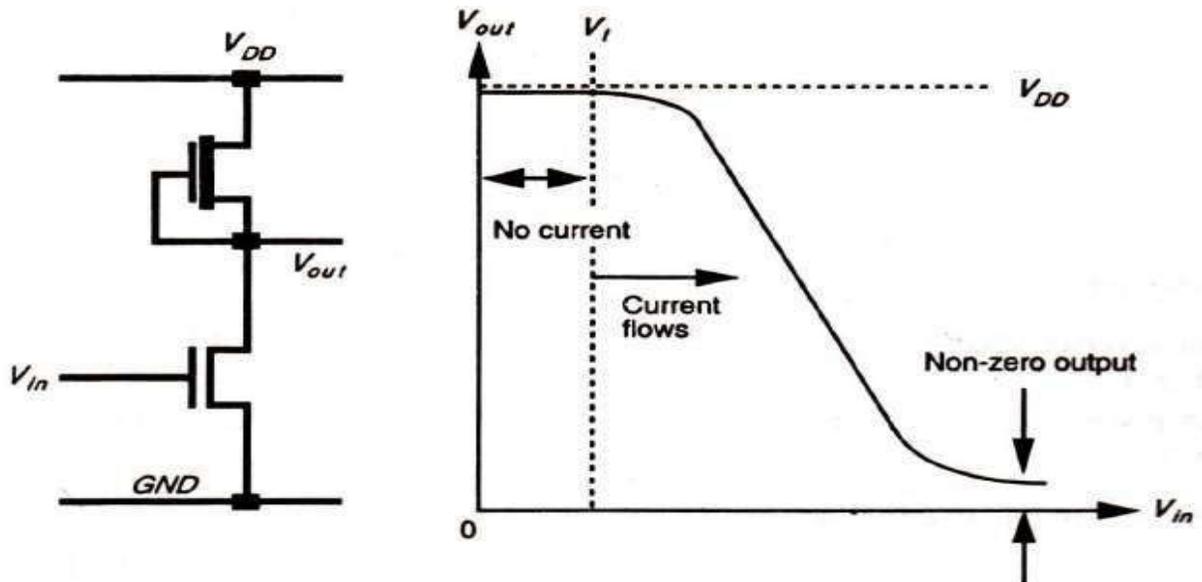
nMOSdepletionmodetransistorpull-upandtransfercharacteristic

(c) Whenswitchingtheoutputfrom1to0,thepull-updeviceisnon-saturatedinitiallyandthis presents lower resistance through which to charge capacitive loads .

(ii)**nMOSenhancementmodepull-up:**Thisarrangementconsistsofan-MOSenhancementmode transistor as pull-up. The arrangement and the transfer characteristic are shownbelow.


nMOSenhancementmodepull-upandtransfercharacteristic

Theimportantfeaturesofthisarrangementare

(a) DissipationishighsincecurrentflowswhenVin=logical1(VGGisreturnedtoVDD).

(b) Voutcanneverreach VDD(logical I)ifVGG=VDDasisnormallythecase.

(c) VGGmaybederivedfromaswitchingsource,for example,onephaseofa clock,sothat

dissipationcanbegreatlyreduced.

(d) IfVGGishigherthanVDDthenanextrasupplyrailisrequired.

(iii)**Complementarytransistorpull-up(CMOS):**ThisarrangementconsistsofaC-MOS arrangement as pull-up. The arrangement and the transfer characteristic are shown below


(a) Circuit   (b) Transfer characteristic
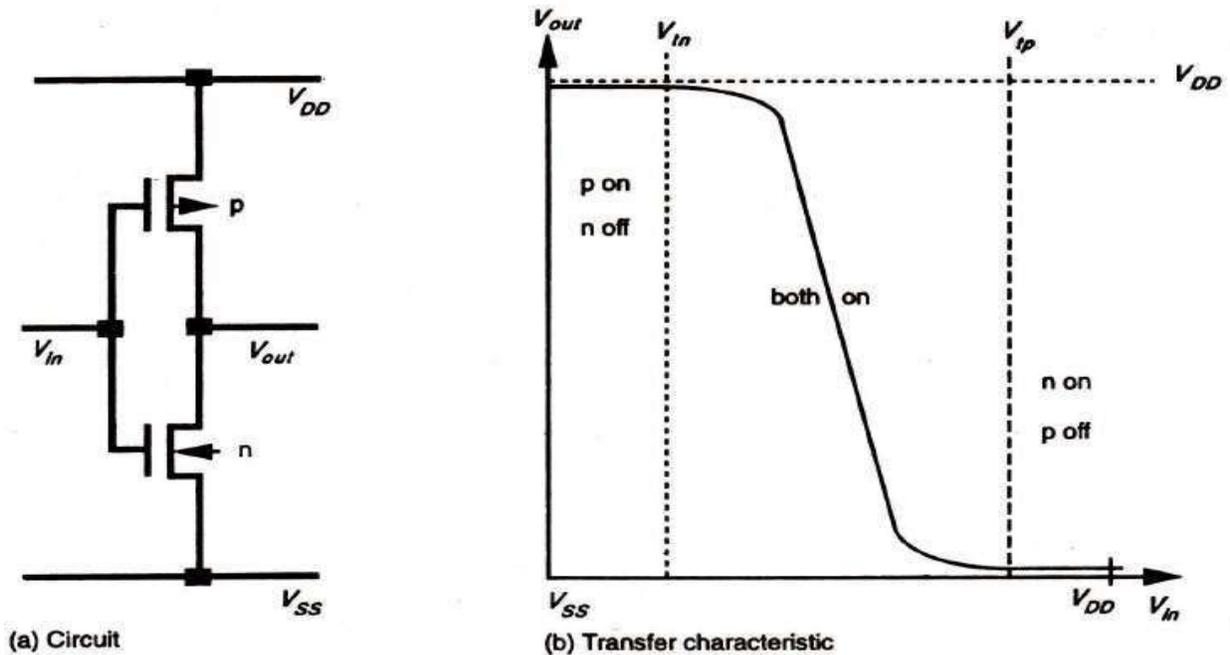
Thesalientfeaturesofthisarrangementare

(a) Nocurrentflowseitherforlogical0orforlogical 1inputs.

(b) Fulllogical1and0levelsarepresented attheoutput.

(c) Fordevicesofsimilardimensionsthep-channelisslowerthanthen-channeldevice.

**BiCMOSINVERTER:**

A BiCMOS inverter, consists of a PMOS and NMOS transistor (M2 andM1), twoNPN bipolar junction transistors,(Q2 and Q1), and two impedances which act as loads(Z2 and Z1) as shown inthe circuit below.
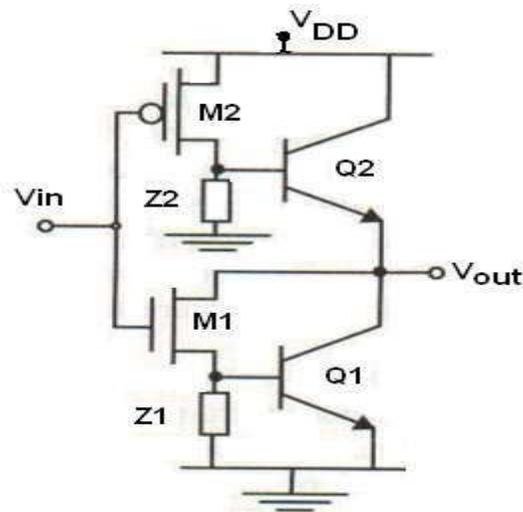
When input, Vin, is high (VDD), the NMOS transistor (M1), turns on, causing Q1 to conduct,while M2 and Q2 are off, as shown in figure (b) . Hence , a low (GND) voltage is translated to the output Vout. On the other hand, when the input is low, the M2 and Q2 turns on, while M1and Q1 turns off, resulting to a high output level at the output as shown in Fig.(b).

In steady-state operation, Q1 and Q2 never turns on or off simultaneously, resulting to a lower power consumption. This leads to a push-pull bipolar output stage. Transistors M1and M2, on the other hand, works as a phase-splitter, which results to a higher input impedance.
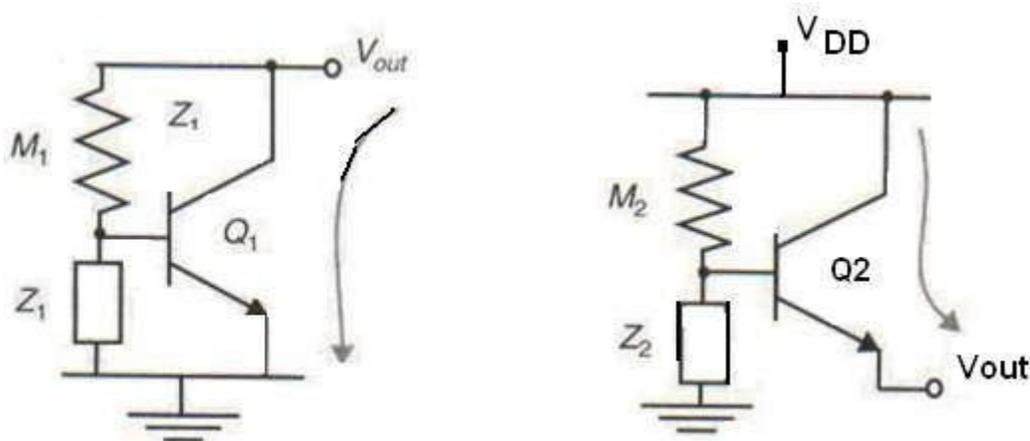
The impedances Z2 and Z1 are used to bias the base-emitter junction of the bipolar transistor and to ensure that base charge is removed when the transistors turn off. For example when the input voltage makes a high-to-low transition, M1 turns off first. To turn off Q1, the base charge must beremoved, whichcanbeachievedbyZ1.Withthiseffect,transitiontimereduces.However,

there exists a short time when both Q1 and Q2 are on, making a direct path from the supply (VDD) to the ground. This results to a current spike that is large and has a detrimental effect on boththe noise andpowerconsumption,which makesthe turning offof thebipolartransistor fast .

ComparisonofBiCMOSandC-MOStechnologies

The BiCMOS gates perform in the same manner as the CMOS inverter in terms of power consumption, because both gates display almost no static power consumption.

When comparing BiCMOS and CMOS in driving small capacitive loads, their performance are comparable, however, making BiCMOS consume more power than CMOS. On the other hand, driving larger capacitive loads makes BiCMOS in the advantage of consuming less power than CMOS, because the construction of CMOS inverter chains are needed to drive large capacitance loads, which is not needed in BiCMOS.

The BiCMOS inverter exhibits a substantial speed advantage over CMOS inverters, especially when driving large capacitive loads. This is due to the bipolar transistor's capability ofeffectively multiplying its current.

For very low capacitive loads, the CMOS gate is faster than its BiCMOS counterpart due tosmall values of *Cint*. This makes BiCMOS ineffective when it comes to the implementation of internal gates for logic structures such as ALUs, where associated load capacitances are small.

BiCMOS devices have speed degradation in the low supply voltage region and also BiCMOS is having greater manufacturing complexity than CMOS.

Assignment Questions:

1. Define threshold voltage? Drive the Vt equation for MOS transistor.
2. Explain with neat diagrams the various NMOS fabrication technology.
3. Draw and explain BiCMOS inverter circuit.
4. Discuss the Basic Electrical Properties of MOS and BiCMOS Circuits.
5. Derive the expression for estimation of Pull-Up to Pull-Down ratio of an n-MOS inverter driven by another n-MOS inverter.
6. Derive the relationship between I_{ds} and V_{ds}
7. Derive the expression for transfer characteristics of CMOS Inverter.
8. Write about BiCMOS fabrication in an-well process with a diagram.
9. Distinguish between Bipolar and CMOS devices technologies in brief.
10. Mention about the BICMOS Inverters and alternative BICMOS Inverters.
11. Determine the pull-up to pull down ratio for NMOS inverter driven by another NMOS Inverter
12. Draw the fabrication steps of CMOS transistor and explain its operation in detail.
13. Draw the fabrication steps of NMOS transistor and explain its operation in detail.