UNITII

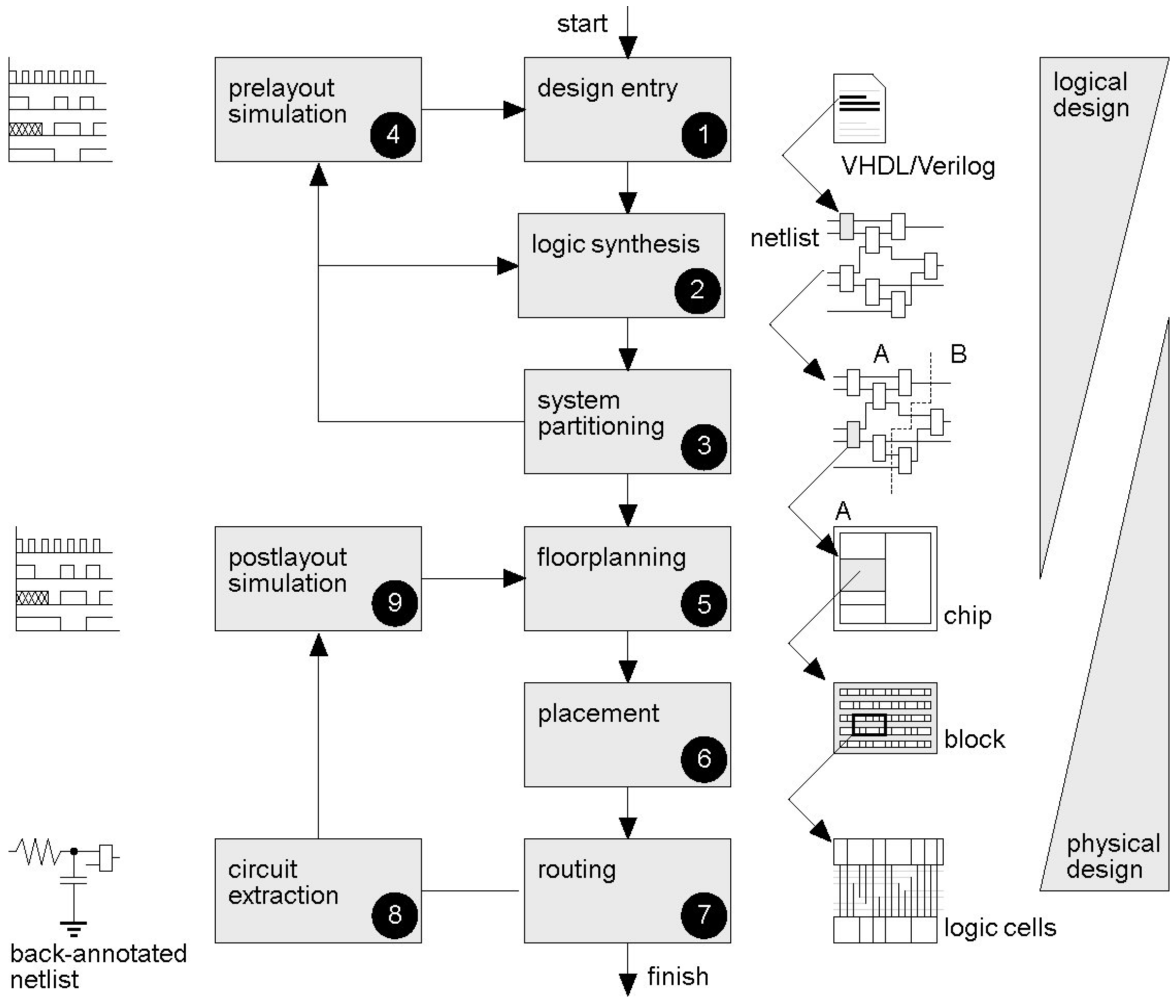
VLSICircuitDesignProcesses

- VLSIDesignFlow
- MOS Layers
- StickDiagrams
- DesignRulesandLayout
- Lamda(λ)baseddesignrulesfor wires, contacts and Transistors
- LayoutDiagramsforNMOSand CMOS Inverters and Gates
- ScalingofMOS circuits

VLSIDESIGNFLOW

A design flow is a sequence of operations that transform the IC designers' intention (usually represented in RTL format) into layout GDSII data.

Awell-tuneddesignflowcanhelpdesignersgothroughthechip-creationprocessrelativelysmoothly and with a decent chance of error-free implementation. And, a skilful IC implementation engineercan usethe design flowcreativelyto shorten thedesign cycle, resultingina higher likelihoodthat the product will catch the market window.



Front-enddesign(Logical design):

1. Design entry – Enter the design in to an ASIC design system using a hardware description language (HDL) or schematic entry

2. Logic synthesis – Generation of net list (logic cells and their connections) from HDL code. Logic synthesis consists of following steps: (i) Technology independent Logic optimization (ii) Translation: Converting Behavioral description tostructural domain (iii) Technologymappingor Library binding

3. Systempartitioning-Divide alargesysteminto ASIC-sized pieces

4. Pre-layout simulation - Check to see if the design functions correctly. Gate level functionality and timing details can be verified.

Back-enddesign(Physicaldesign):

5. Floorplanning -Arrangetheblocks ofthe netliston the chip

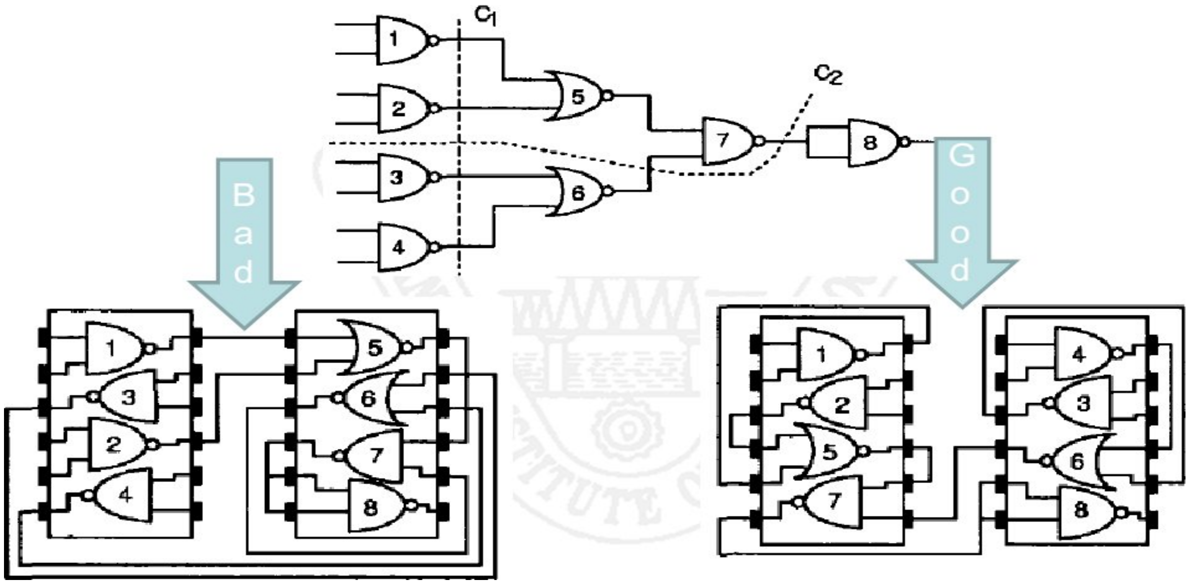
6. Placement-Decidethelocationsofcellsina block

7. Routing-Maketheconnectionsbetweencellsand blocks

8. CircuitExtraction -Determinethe resistance andcapacitanceofthe interconnect

9. Post-layoutsimulation-Checktoseethedesignstillworkswiththeaddedloadsofthe interconnect

Partitioning



MOS LAYERS

MOSdesignisaimedatturningaspecificationintomasksforprocessingsilicontomeetthe specification. We have seen that MOS circuits are formed on four basic layers

- N-diffusion
- P-diffusion
- PolySi
- Metal

which are isolated from one another by thick or thin (thinox) silicon silicon dioxide insulating layers. The thin oxide (thinox) mask region includes n-diffusion, p-diffusion, and transistor channels. Polysilicon and thinox regions interact so that a transistor is formed where they cross one another.

STICK DIAGRAMS

A stick diagram is a diagrammatic representation of a chip layout that helps to abstract a model for design of full layout from traditional transistor schematic. Stick diagrams are used to convey the layer information with the help of a color code.

“Astickdiagramisa cartoonofalayout.”

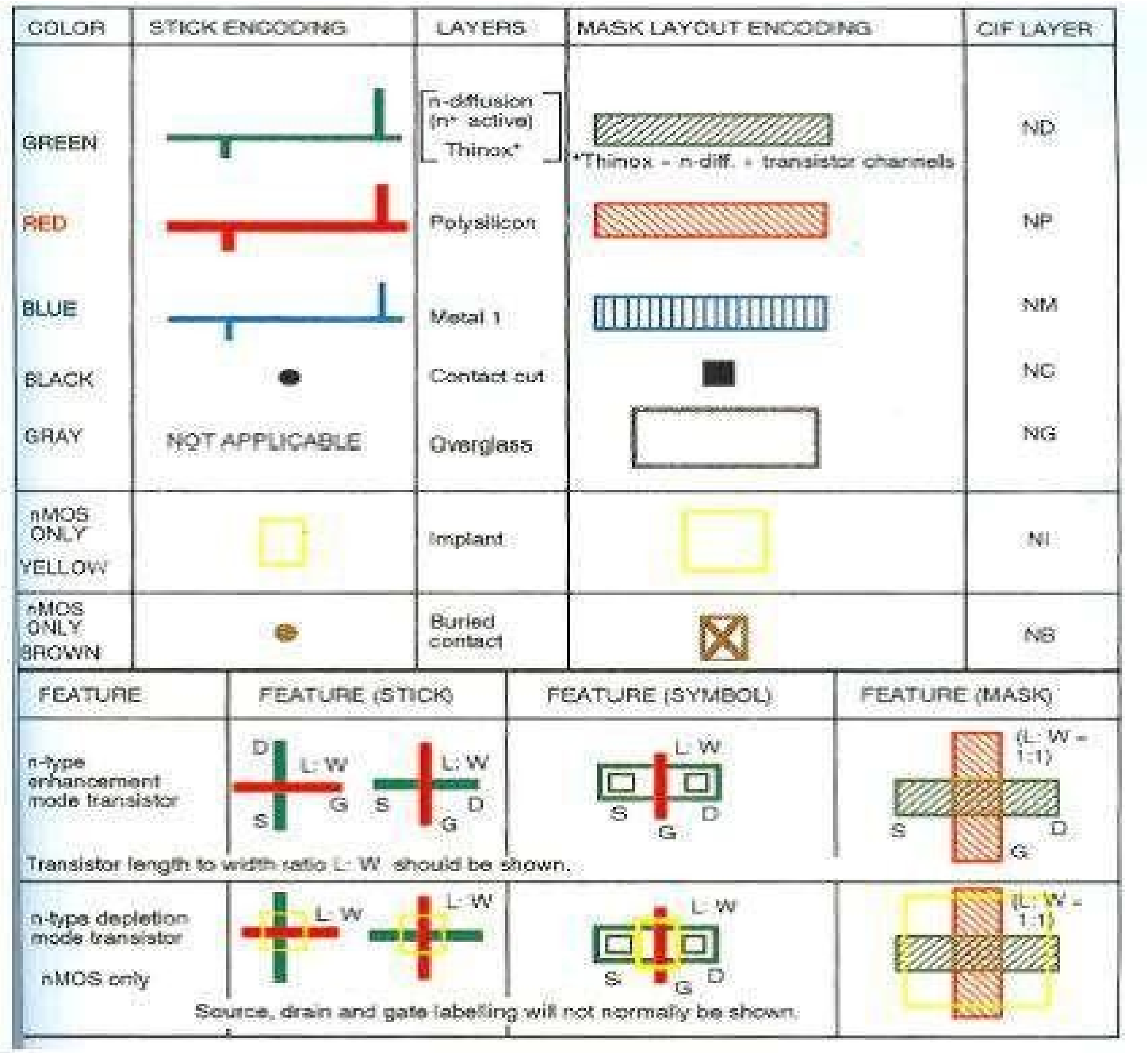
The designer draws a freehand sketch of a layout, using colored lines to represent the various process layers such as diffusion, metal and polysilicon. Where polysilicon crosses diffusion, transistors are created and where metal wires join diffusion or polysilicon, contacts are formed.

Forexample,inthecase ofnMOS design,

- Greencolorisusedforn-diffusion
- Redfor polysilicon
- Bluefor metal
- Yellowforimplant,and blackforcontactareas.

Monochromeencodingisalsousedinstickdiagramstorepresentthelayerinformation.

StickDiagrams–NMOSEncoding

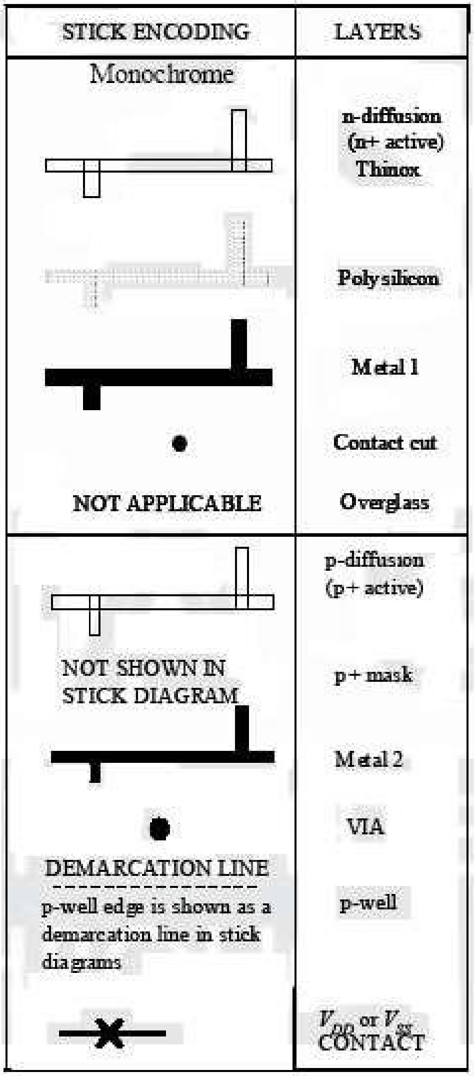


COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
GREEN		n-diffusion (n^+ active) Thinox*	*Thinox = n-diff. + transistor channels	ND
RED		Polysilicon		NP
BLUE		Metal 1		NM
BLACK	●	Contact cut	■	NC
GRAY	NOT APPLICABLE	Overglass		NG
nMOS ONLY YELLOW		Implant		NI
nMOS ONLY BROWN	●	Buried contact	☒	NB

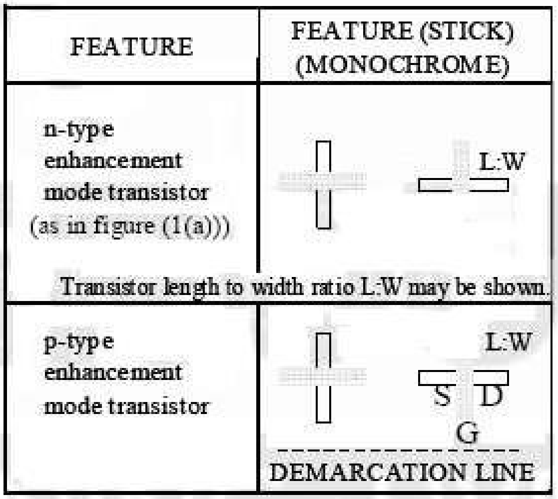
FEATURE	FEATURE (STICK)	FEATURE (SYMBOL)	FEATURE (MASK)
n-type enhancement mode transistor	D L:W G S L:W S D G	L:W S G D	(L:W = 1:1) S D G
Transistor length to width ratio L:W should be shown.			
n-type depletion mode transistor nMOS only	L:W L:W	L:W S G D	(L:W = 1:1)
Source, drain and gate labelling will not normally be shown.			

NMOSENCODING

CMOSENCODING



STICK ENCODING	LAYERS
Monochrome	
	n-diffusion (n+ active) Thinox
	Polysilicon
	Metal 1
●	Contact cut
NOT APPLICABLE	Overglass
	p-diffusion (p+ active)
NOT SHOWN IN STICK DIAGRAM	p+ mask
	Metal 2
●	VIA
DEMARCATION LINE p-well edge is shown as a demarcation line in stick diagrams	p-well
	V_{DD} or V_{SS} CONTACT

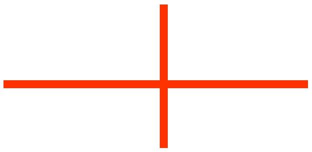


FEATURE	FEATURE (STICK) (MONOCHROME)
n-type enhancement mode transistor (as in figure (1(a)))	L:W
Transistor length to width ratio L:W may be shown.	
p-type enhancement mode transistor	L:W S D G DEMARCATION LINE

StickDiagrams–Some Rules

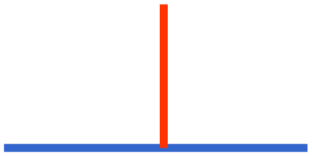
Rule1:

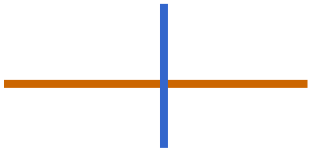
When two or more ‘sticks’ of the same type cross or toucheach other that represents electrical contact.

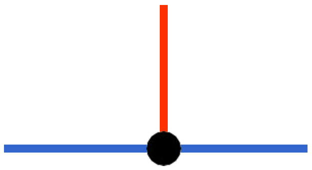


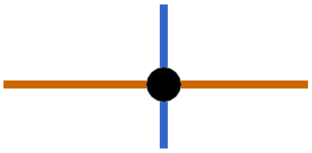
Rule2:

Whentwoormore“sticks”ofdifferenttypecrossortoucheachotherthereisnoelectrical contact. (If electrical contact is needed we have to show the connection explicitly)









Rule3:

Whenapolycrosses diffusionit representsa transistor.

Note: Ifacontactis shown thenit is***not***atransistor.

Rule4:

In CMOS ademarcation lineis drawnto avoid touchingofp-diffwith n-diff. All PMOS must lie on one side of the line and all NMOS will have to be on the other side.

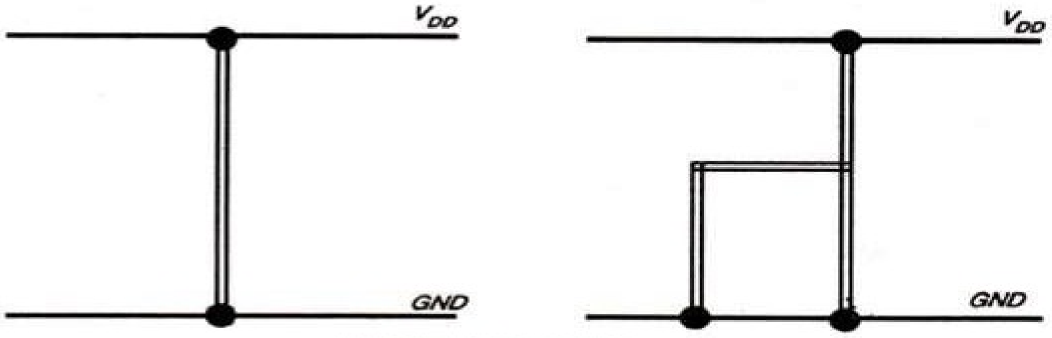
nMOSDesign Style:

TounderstandthedesignrulesfornMOSdesignstyle,letusconsiderasinglemetal,single polysilicon nMOS technology.

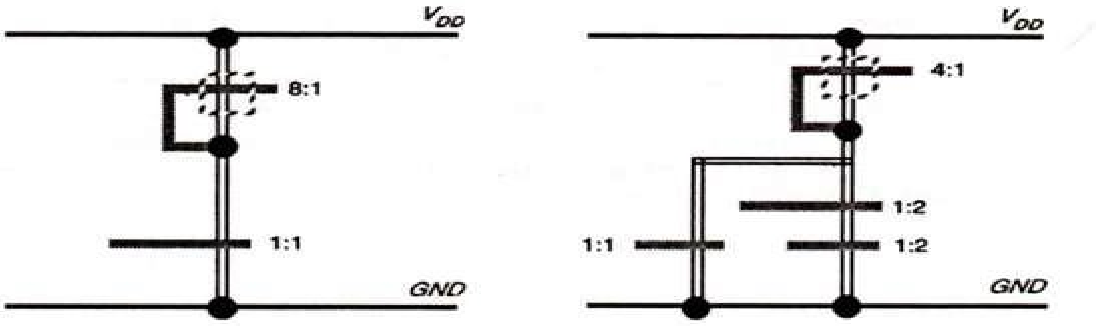
Thelayout ofnMOS isbased onthefollowingimportant features.

- ✓ n-diffusion[n-diff.] andotherthinoxideregions[thinox] (green);
- ✓ polysilicon1 [poly.]-sincethereis onlyonepolysilicon layer here (red);
- ✓ metal1 [metal]-sinceweuse onlyonemetal layerhere(blue);
- ✓ implant (yellow);
- ✓ contacts(blackorbrown[buried]).

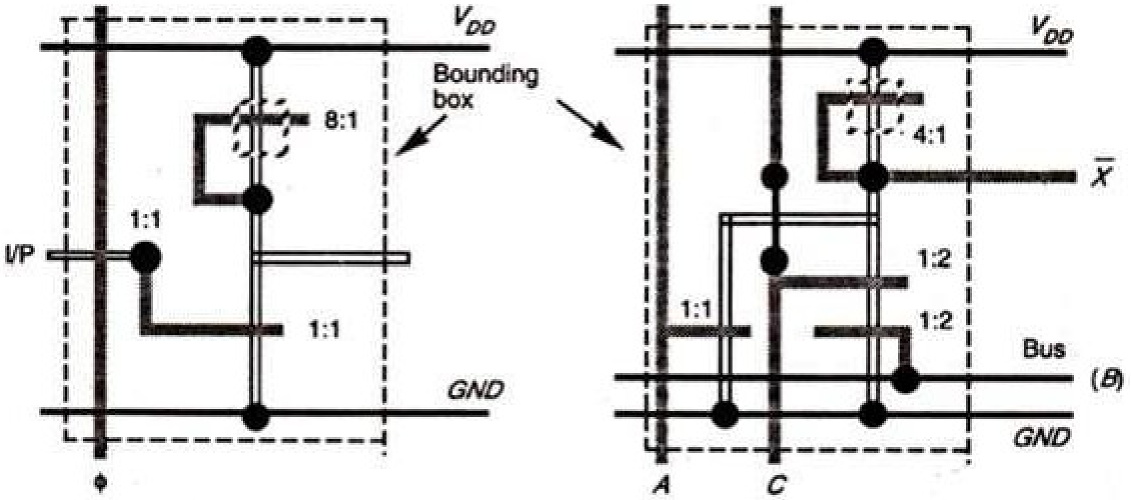
A transistor is formed wherever poly. crosses n-diff. (red over green) and all diffusion wires (interconnections) are n-type (green).When starting a layout, the first step normally taken is to drawthemetal (blue)V_{DD}andGNDrailsinparallelallowingenoughspacebetweenthem forthe other circuit elements which will be required. Next, thinox (green) paths may be drawn between the rails for inverters and inverter based logic as shown in Fig. below. Inverters and inverter- based logic comprise a pull-up structure, usually a depletion mode transistor, connected from the output point to V_{DD} and a pull down structure of enhancement mode transistors suitably interconnectedbetweentheoutputpointand GND.ThisisillustratedintheFig.(b).remembering that poly. (red) crosses thinox (green)wherever transistors are required. One should consider the implants (yellow) for depletion mode transistors and also consider the length to width (L:W)ratio for each transistor. These ratios are important particularly in nMOS and nMOS- likecircuits.



(a) Rails and thinox paths



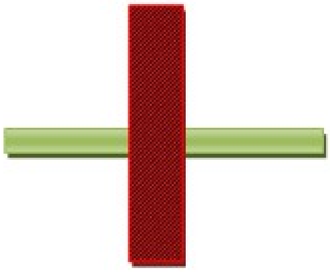
(b) Pull-up and pull-down structures (polysilicon), implants, and ratios



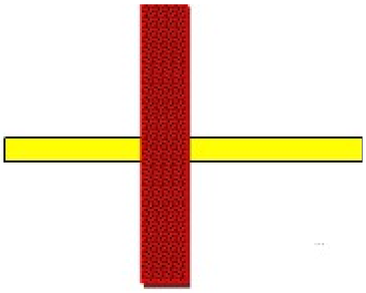
(c) Buses, control signals, interconnections, and 'leaf-cell' boundaries

CMOSDesignStyle:

TheCMOS design rules are almost similar and extensions of n-MOS design rules except the Implant(yellow) and the buried contact (brown). In CMOS design Yellow is used to identify p transistors and wires, as depletion mode devices are not utilized. The two types of transistors 'n' and 'p', are separated bythe demarcation line (representing the p-well boundary) above which all p-type devicesareplaced (transistorsand wires (yellow).The n-devices(green) areconsequently placed below the demarcation line and are thus located in the p-well as shown in the diagram below.

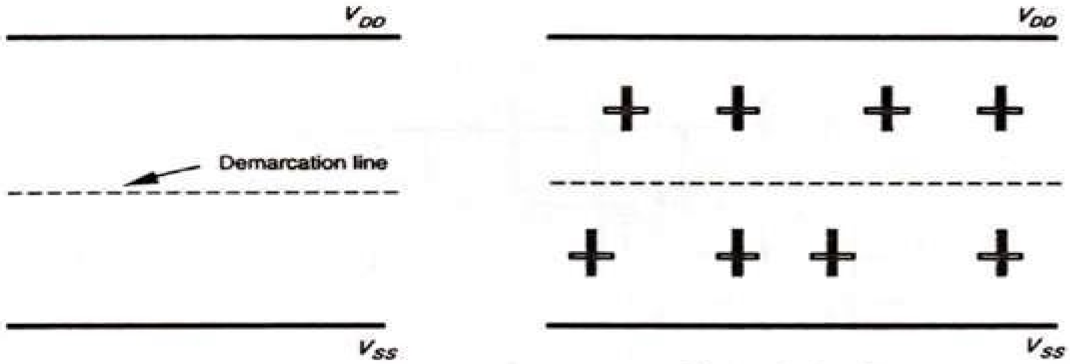


N-type (red over green)

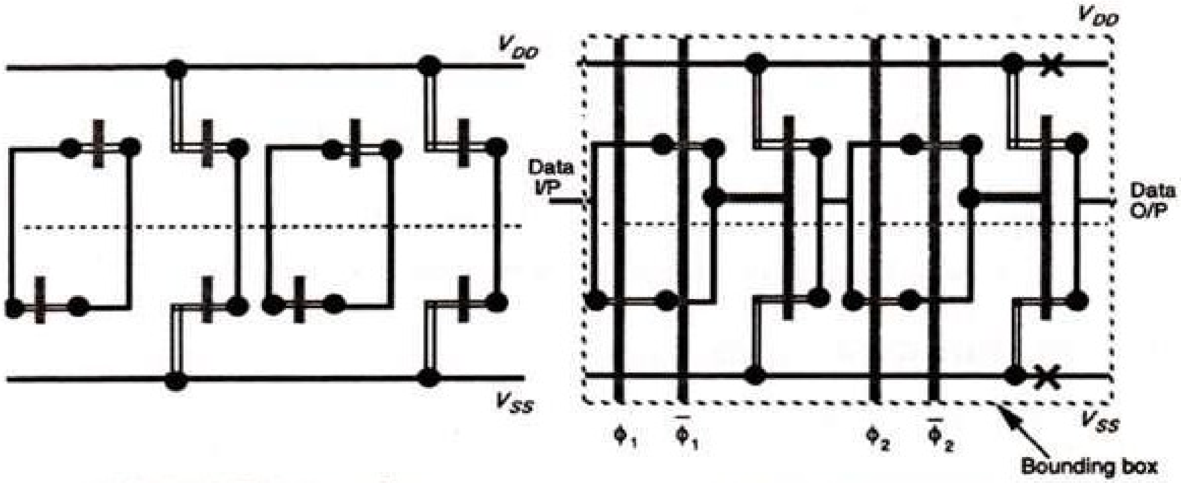


P-type (red over yellow)

Diffusion paths must not cross the demarcation line and n-diffusion and p-diffusion wires must not join. The 'n' and 'p' features are normally joined by metal where a connection is needed. Their geometrywill appear whenthestickdiagramistranslatedtoa masklayout. However, one must notforget to place crosses on VDD and Vss rails to represent the substrate and p-well connection respectively. The design style is explained bytakingthe example the design of a single bit shift register. The design begins with the drawing of the VDD and Vss rails in parallel and in metal and the creation of an (imaginary) demarcation line in-between, as shownin Fig.below. The n-transistors are then placed belowthis line and thus close to Vss, while p-transistors are placed above the line and below VDD In both cases, the transistors are conveniently placed with their diffusion paths parallel to the rails (horizontal in the diagram) as shown in Fig.(b). A similar approach can be taken with transistors in symbolic form.



(a) Rails and demarcation line (b) n- and p-transistors

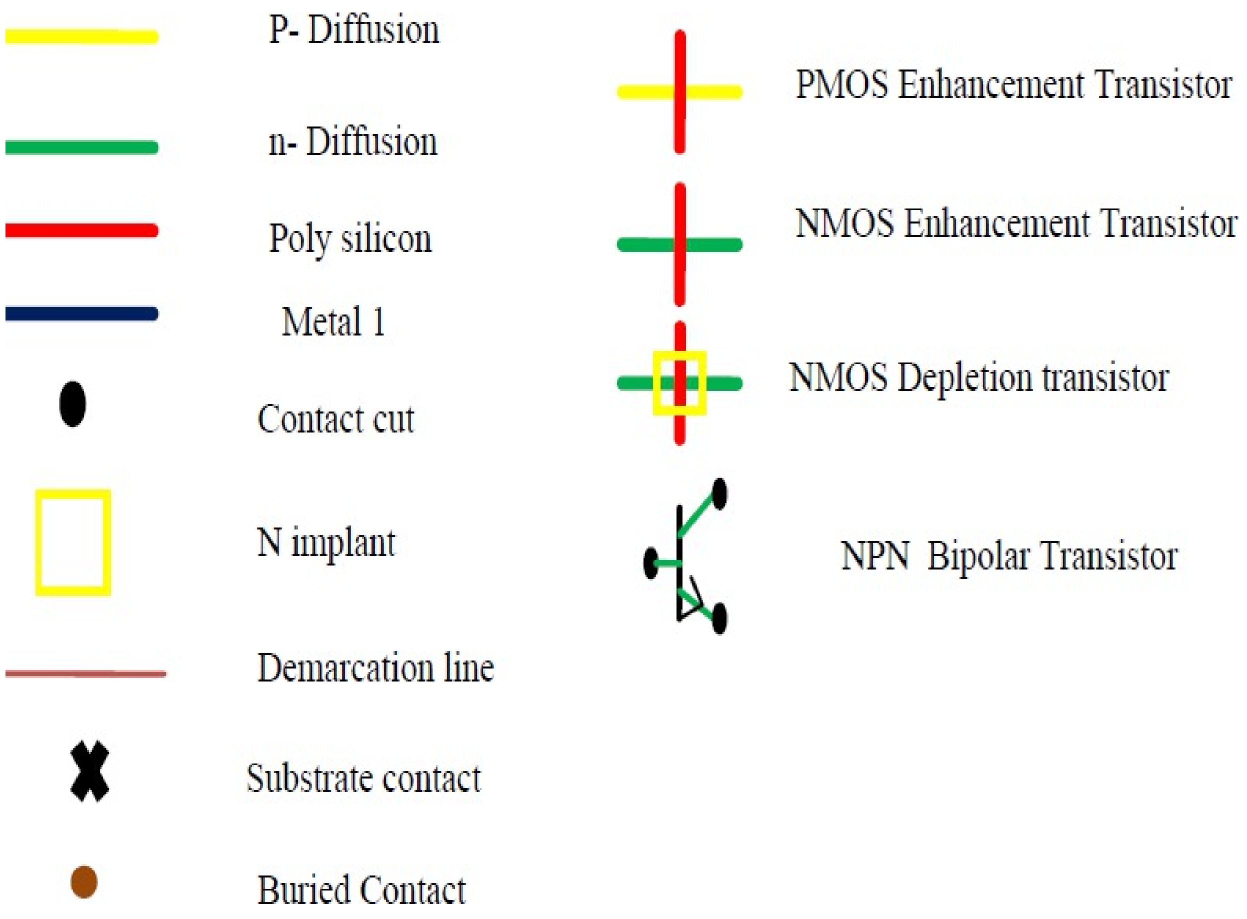


(c) Metal and diffusion connections (d) Remaining interconnections

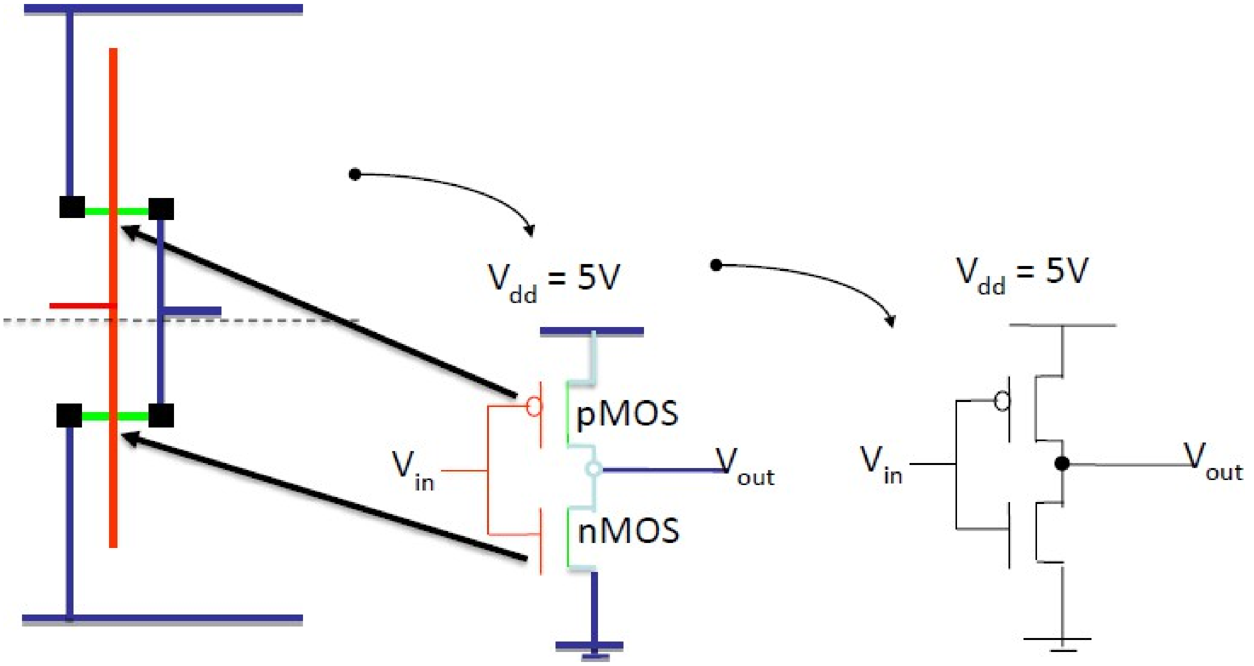
Fig.CMOS sticklayoutdesign style (a,b,c,d)

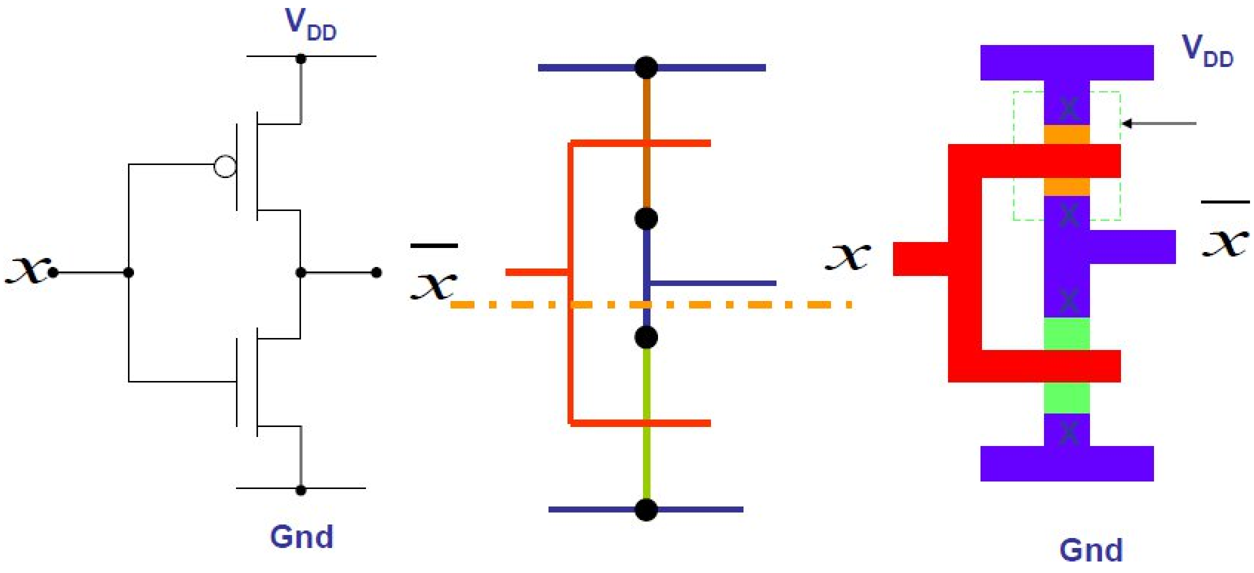
The n- along with the p-transistors are interconnected to the rails using the metal and connect as Shownin Fig.(d). It must be remembered that only metal and poly-silicon can cross the demarcation line but with that restriction, wires can run-in diffusion also. Finally, the remaining interconnections are made as appropriate and the control signals and data inputs are added as shown in the Fig.(d).

Stick Diagrams:

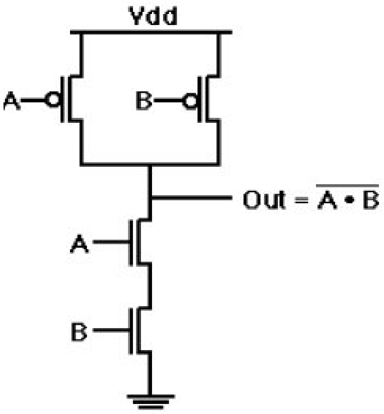


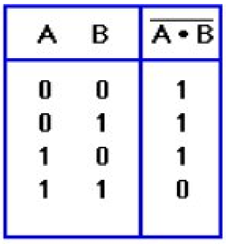
ExamplesofStickDiagramsCMOSInverter



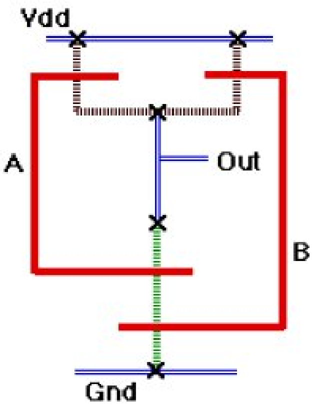


Contd….





A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

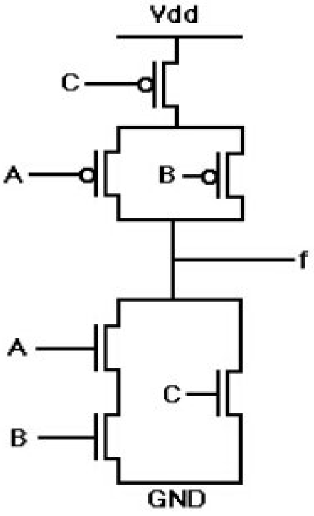


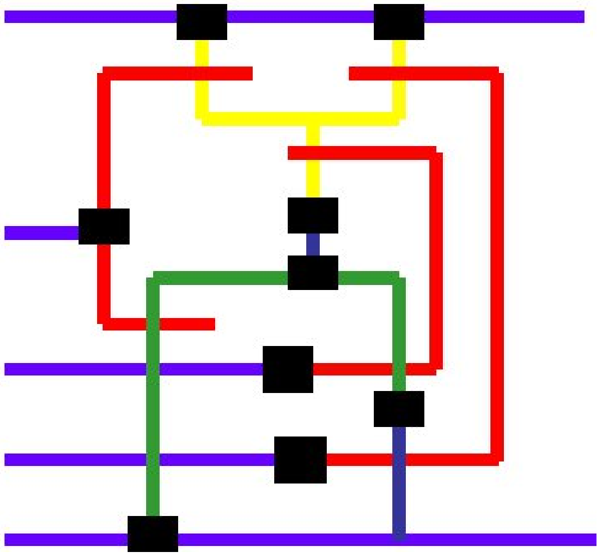
1. Pull-down: Connect to ground If A=1 AND B=1

2. Pull-up: Connect to Vdd If A=0 OR B=0

Fig.CMOSNANDgate

Example: $f = \overline{(A \cdot B) + C}$





DesignRulesandLayout

In VLSI design, as processes become more and more complex, need for the designer to understand the intricacies of the fabrication process and interpret the relations between the different photo masks is really troublesome. Therefore, a set of layout rules, also called **design rules**, has been defined. They act as an interface or communication link between the circuit designer and the process engineer duringthe manufacturingphase. The objective associated with layout rules is to obtain a circuit with optimum yield (functional circuits versus non-functional circuits) in as small as area possible without compromising reliability of the circuit. In addition, Design rules can be conservative or aggressive, depending on whether yield or performance is desired. Generally, they are a compromise between the two. Manufacturing processes have their inherent limitations in accuracy. So the need of design rules arises due to manufacturing problems like –

- Photoresistshrinkage, tearing.
- Variationsinmaterialdeposition,temperature andoxidethickness.
- Impurities.
- Variations across a wafer.

Theseleadtovariousproblemslike:

- **Transistorproblems:**

  Variations in threshold voltage: This may occur due to variations in oxide thickness, ion-implantation and poly layer. Changes in source/drain diffusion overlap. Variations in substrate.
- **Wiring problems:**

  Diffusion: There is variation in doping which results in variations in resistance, capacitance. Poly, metal: Variations in height, width resulting in variations in resistance, capacitance. Shorts and opens.
- **Oxideproblems:**

  Variationsin height.

  Lackofplanarity.

- **Via problems:**

  Viamaynotbecutallthe waythrough.

Undersizeviahastoomuchresistance.

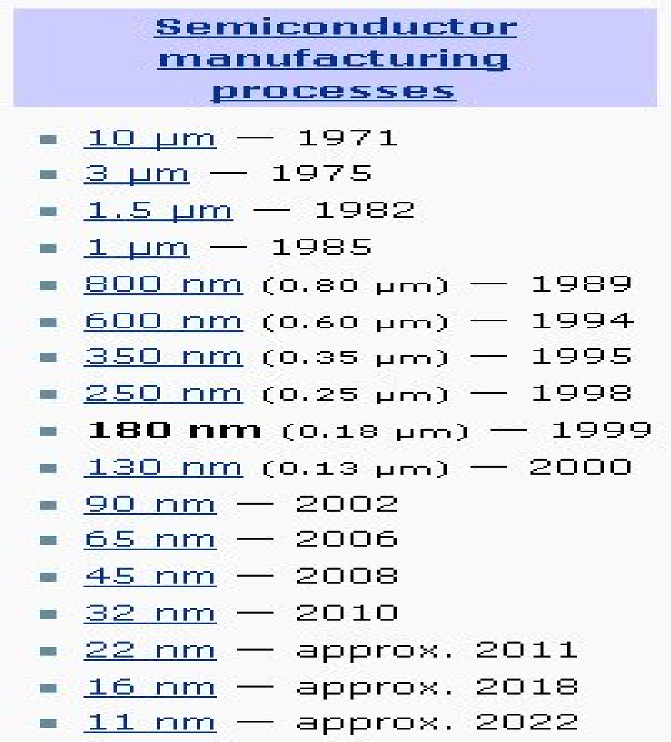
Via may be too large and create short.

To reduce these problems, the design rules specify to the designer certain geometric constraints on the layout artwork so that the patterns on the processed wafers will preserve the topology and geometryof the designs. This consists of minimum-width and minimum-spacing constraints and requirements between objects on the same or different layers.Apart from followinga definiteset of rules, design rules also come by experience.

Why weusedesignrules?

- Interfacebetweendesignerandprocessengineer
- Historically, the process technology referred to the length of the silicon channel between the source and drain terminals in field effect transistors.
- The sizes of other features are generally derived as a ratio of the channel length, where some may be larger than the channel size and some smaller.

For example, in a 90 nm process, the length of the channel may be 90 nm, but the width of the gate terminal may be only 50 nm.



Semiconductor manufacturing processes

- 10 µm — 1971
- 3 µm — 1975
- 1.5 µm — 1982
- 1 µm — 1985
- 800 nm (0.80 µm) — 1989
- 600 nm (0.60 µm) — 1994
- 350 nm (0.35 µm) — 1995
- 250 nm (0.25 µm) — 1998
- **180 nm** (0.18 µm) — 1999
- 130 nm (0.13 µm) — 2000
- 90 nm — 2002
- 65 nm — 2006
- 45 nm — 2008
- 32 nm — 2010
- 22 nm — approx. 2011
- 16 nm — approx. 2018
- 11 nm — approx. 2022

Designrulesdefinerangesforfeatures

Examples:

- min.wirewidths to avoid breaks
- min.spacingtoavoid shorts
- minimumoverlapstoensurecompleteoverlaps

Measuredin microns

Requiredforresolution/tolerancesofmasks

Fabrication processes defined by minimum channel width

Also minimum widthofpolytraces

Defines“howfast”afabricationprocessis

TypesofDesignRules

Thedesign rulesprimaryaddresstwo issues:

1. Thegeometricalreproductionoffeaturesthatcanbereproducedbythemaskmakingand lithographical process, and
2. Theinteractionbetweendifferentlayers.

Thereareprimarilytwoapproaches in describingthedesignrules.

1. Linearscalingis possibleonlyover alimited rangeof dimensions.
2. Scalable design rules areconservative .This results in over dimensioned and less dense design.
3. Thisruleis notused inreal life.

1. ScalableDesignRules(e.g.SCMOS,λ-baseddesignrules):

In this approach, all rules are defined in terms of a single parameter **λ**. The rules are so chosen that a design can be easily ported over a cross section of industrial process ,making the layout portable .Scaling can be easily done by simply changing the value of.

Thekeydisadvantages of thisapproach are:

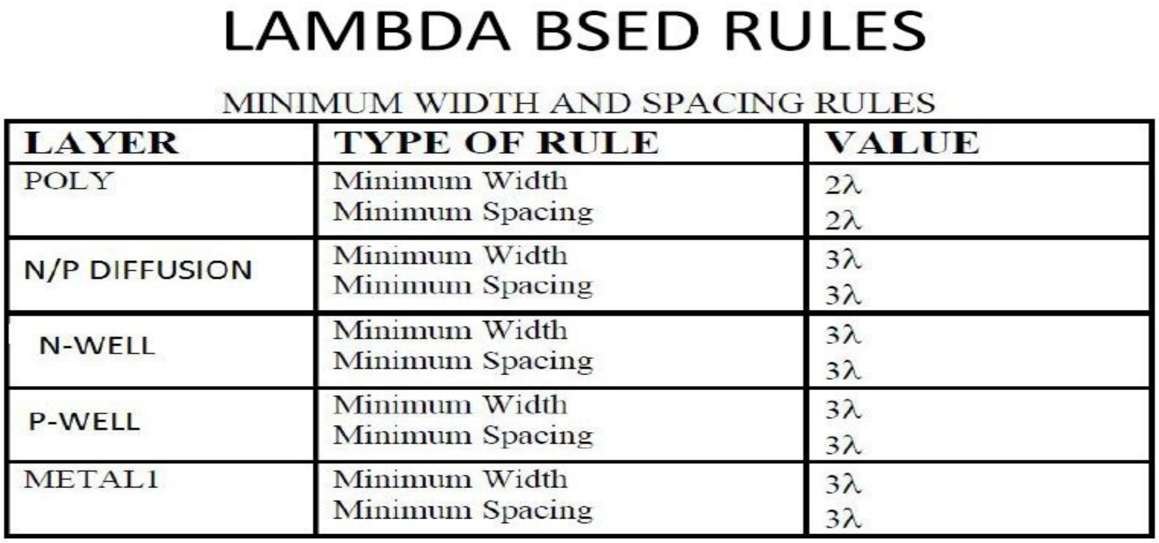
2. **AbsoluteDesign Rules(e.g.μ-baseddesignrules):**

In this approach, the design rules are expressed in absolute dimensions (e.g. 0.75μm) and therefore can exploit the features of a given process to a maximum degree. Here, scaling and porting is more demanding, and has to be performed either manually or using CAD tools .Also, these rules tend to be more complex especially for deep submicron.

The fundamental unity in the definition of a set of design rules is the minimum line width .It stands for the minimum mask dimension that can be safely transferred to the semiconductor material .Even for the same minimum dimension, design rules tend to differ from company to company, and from process to process. Now, CAD tools allow designs to migrate between compatible processes.

LAMBDA-BASED DESIGN RULES:-

- *Lambda-based*(scalableCMOS)designrulesdefinescalablerulesbasedonλ (which is half of the minimum channel length)
  - classesofMOSISSCMOSrules:SUBMICRON,DEEPSUBMICRON
- Stickdiagramisadraftofreallayout,itservesasanabstractviewbetweenthe schematic and layout.
- Circuitdesigneringeneralwanttighter,smallerlayoutsforimprovedperformance and decreased silicon area.
- Ontheotherhand,theprocessengineerwantsdesignrulesthatresultina controllable and reproducible process.
- Generallywefindtherehastobeacompromiseforacompetitivecircuittobe produced at a reasonable cost.
- Allwidths,spacing,anddistancesarewrittenintheform
- λ=0.5X minimumdrawn transistor length
- Design rulesbasedonsingleparameter,λ
- Simpleforthe designer
- Wideacceptance
- Providefeaturesize independent way of settingout mask
- Ifdesignrulesareobeyed,maskswillproduceworkingcircuits
- Minimumfeaturesizeisdefinedas2λ
- Usedtopreservetopologicalfeaturesonachip
- Preventsshorting,opens,contactsfromslippingoutofareatobe contacted



LAMBDA BSED RULES

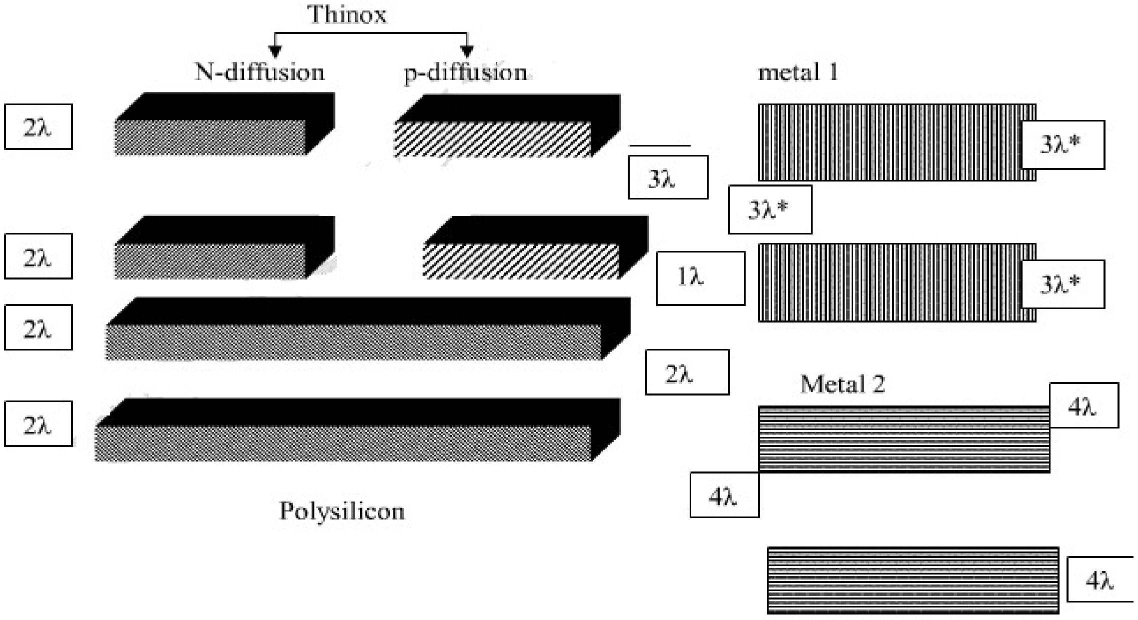
MINIMUM WIDTH AND SPACING RULES

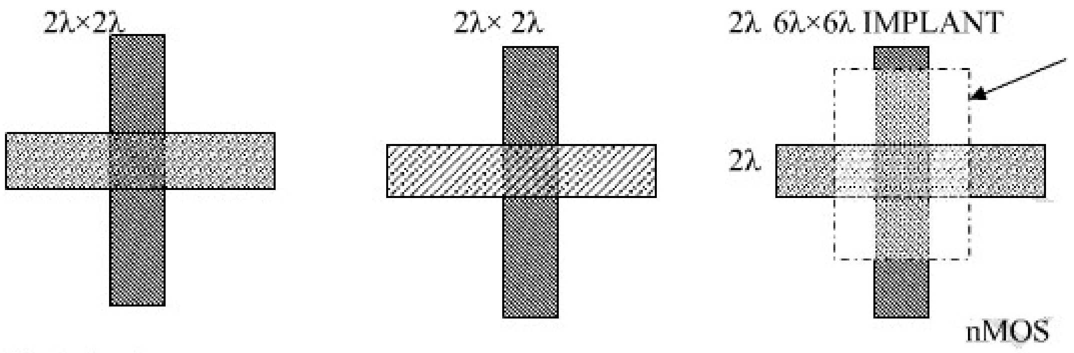
LAYER	TYPE OF RULE	VALUE
POLY	Minimum Width Minimum Spacing	2λ 2λ
N/P DIFFUSION	Minimum Width Minimum Spacing	3λ 3λ
N-WELL	Minimum Width Minimum Spacing	3λ 3λ
P-WELL	Minimum Width Minimum Spacing	3λ 3λ
METAL1	Minimum Width Minimum Spacing	3λ 3λ

DESIGNRULESFOR WIRES (nMOSandCMOS)

Design rules and layout methodology based on the concept of λ provide a process and feature size independent way of setting out mask dimensions to scale. All paths in layers are dimensioned in λ units and subsequently λ can be allocated an appropriate value compatible with the feature size of the fabrication process.

Minimum width specified) minimum separation (where





(depletion)

n MOS (enhancement) pMOS (enhancement)

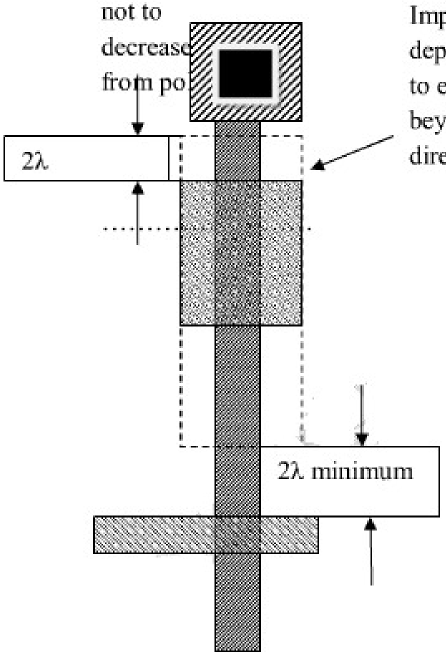
Separation from contact cut to transistor

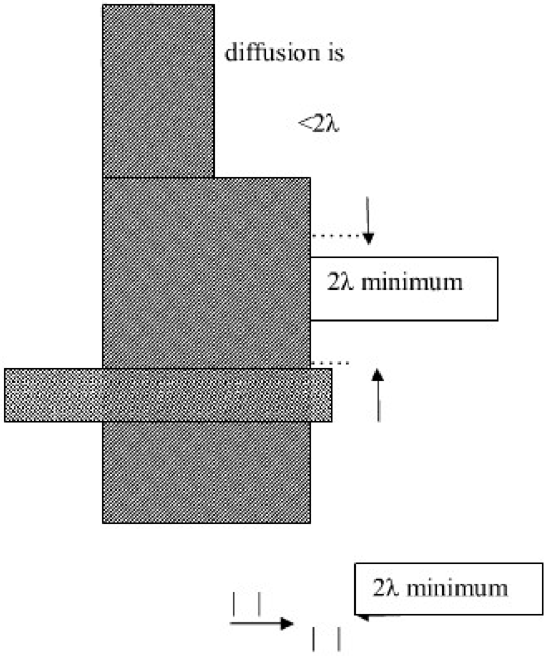
not to

decrease

from po

Implant for an nMOS depletion mode transistor to expend 2λ minimum beyond channel in all directions



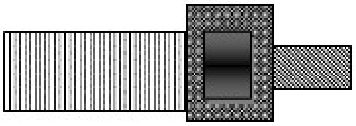


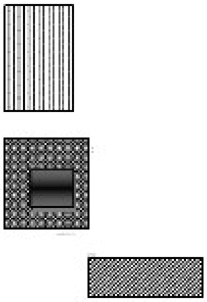
polysilicon to extend a minimum of 2λ beyond diffusion boundaries (width constant)

Separation from implant to another transistor

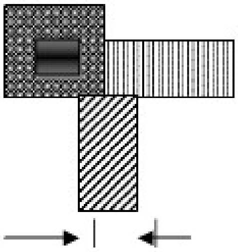
Key: ▨ polysilicon ▨ n-diffusion ▨ p-diffusion ▨ transistor channel ....
(Polysilicon over thinox)

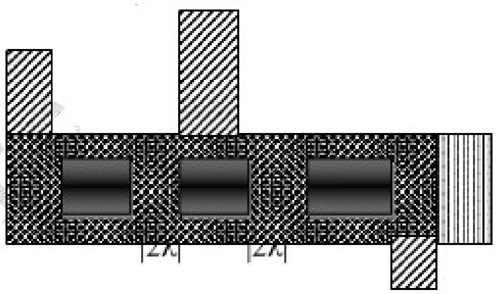
metal 1 to polysilicon or to diffusion





3λ minimum





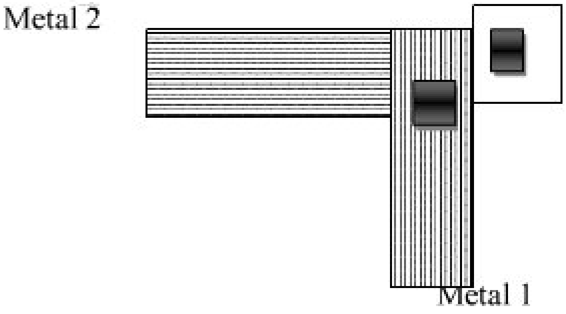
minimum separation multiple

cuts

2λ minimum

2λ×2λ cut centered on 4λ×4λ superimposed area of layers to be joined in all cases

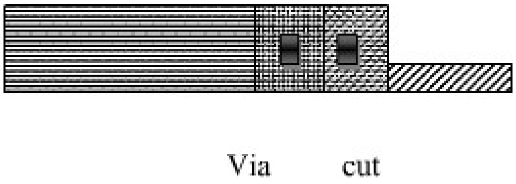
2λ minimum separation (if other spacing's allowed)



4λ×4λ area of overlap with

2λ×2λ via at center

Via and cut used
to connect metal 2
to diffusion →



Contacts (nMOS and CMOS)

CONTACTCUTS

Whenmakingcontactsbetweenpoly-siliconand diffusioninnMOScircuitsitshouldbe remembered that there are three possible approaches--poly. to metal then metal to diff., oraburied contact poly. to diff. , or a butting contact (poly. to diff. using metal). Among the three the latter two, the buried contact is the most widely used, because of advantage in space and a reliable contact. At one time butting contacts were widely used , but now a days they are superseded by buried contacts.

In CMOS designs, poly. to diff. contacts are always made via metal. A simple process is followed for making connections between metal and either of the other two layers (as in Fig.a), The2λ.x2λ.contactcutindicatesanareainwhichtheoxideistoberemoveddowntothe underlying polysilicon or diffusion surface. When deposition of the metal layer takes place themetal is deposited through the contact cut areas onto the underlying area so that contact is made between the layers.

The process is morecomplexfor connecting diffusion to poly-silicon using the buttingcontact approach (Fig.b), In effect, a 2λ. x 2λ contact cut is made down to each of the layers tobejoined.Thelayersarebuttedtogetherinsuchawaythatthesetwocontactcutsbecome contiguous.Sincethepoly-siliconanddiffusionoutlinesoverlapandthinoxideunderpoly siliconactsasamaskinthediffusionprocess,thepoly-siliconanddiffusionlayersarealso butted together. The contact between the two butting layers is then made by a metal overlay as shown in the Fig.

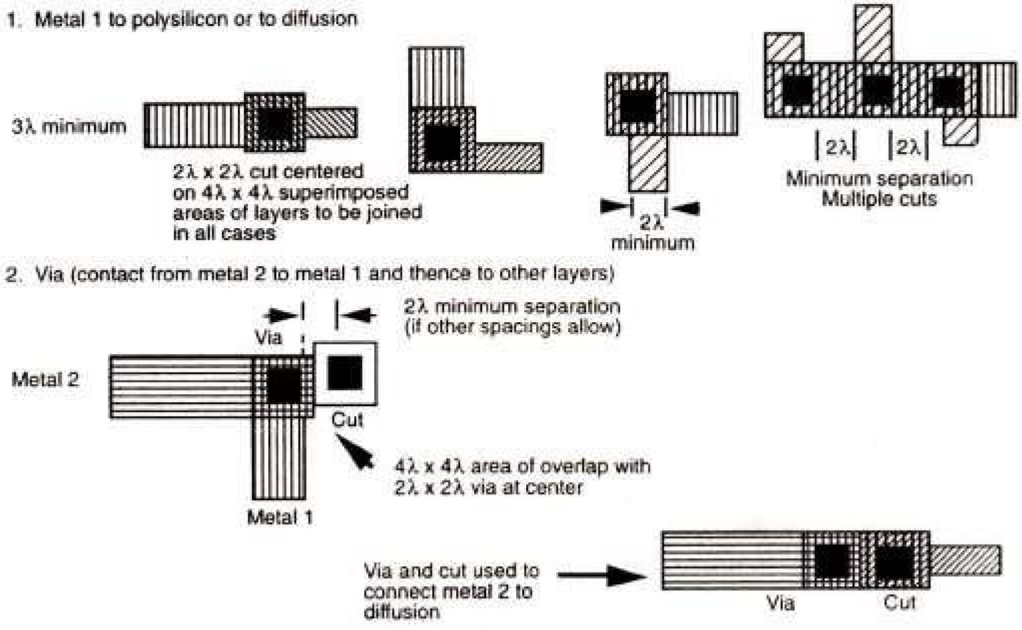


Fig.(a).n-MOS &C-MOS Contacts

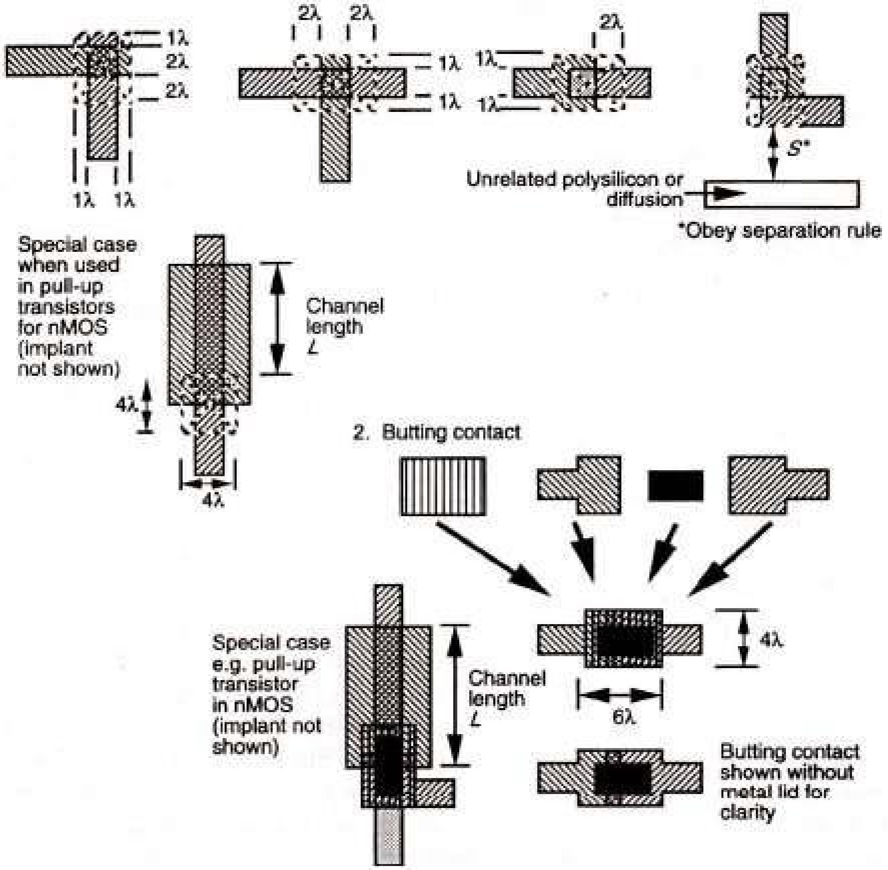


Fig.(b).Contactspoly-silicontodiffusion

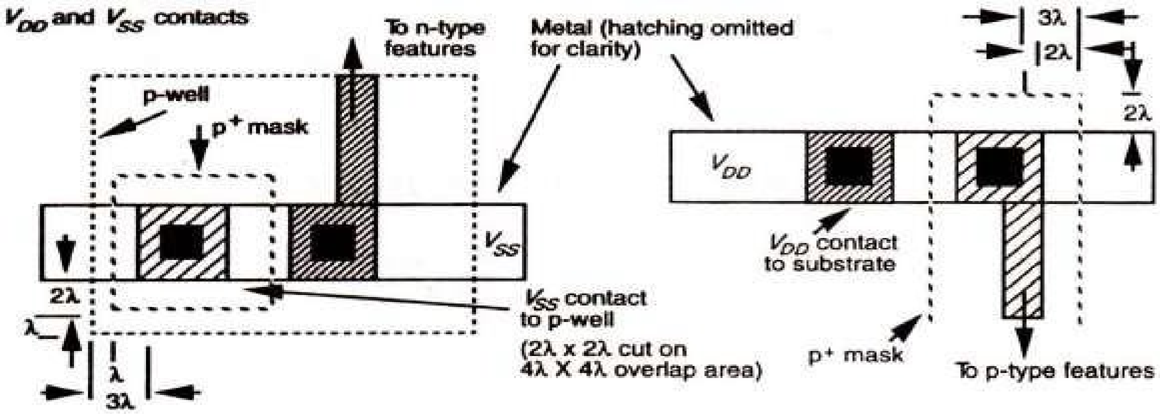
Inburiedcontactbasically,layersarejoinedover a2λ.x2λ.areawiththeburied contact cut extending by 1λ, in all directions around the contact area except that the contact cut extension is increased to 2λ. in diffusion paths leaving the contact area. This helps to avoid the formation of unwanted transistors. So this buried contact approach is simpler when compared to others. The, poly-silicon is deposited directly on the underlying crystalline wafer. Whendiffusion takes place, impurities will diffuse into the poly-silicon as well as into the diffusion region within the contact area. Thus a satisfactoryconnection between poly-silicon and diffusion is ensured. Buried contacts can be smaller in area than their butting contact counterparts and, since they use no metal layer, they are subject to fewer design rule restrictions in a layout.

Otherdesignrules

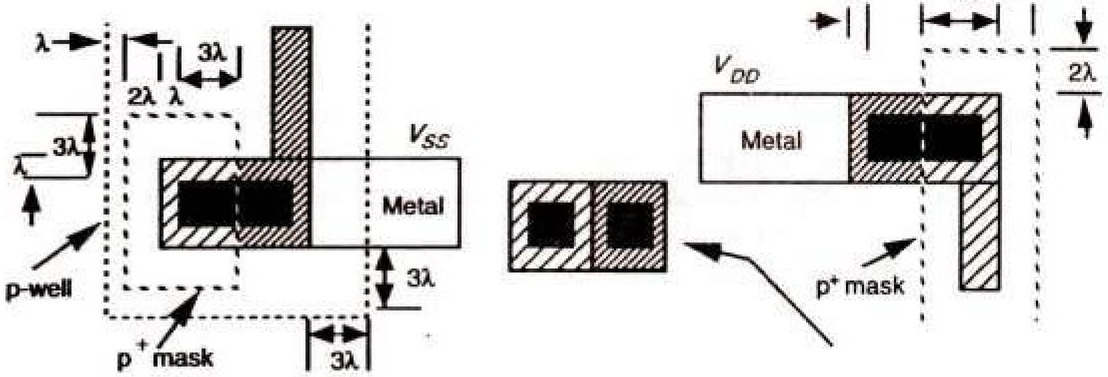
- DoubleMetal MOSprocess Rules
- CMOSfabricationismuchmorecomplexthannMOSfabrication
- 2umDouble metal,Double poly.CMOS/BiCMOS Rules
- 1.2umDoubleMetalsinglepoly.CMOS rules

CMOSLambda-basedDesign Rules:

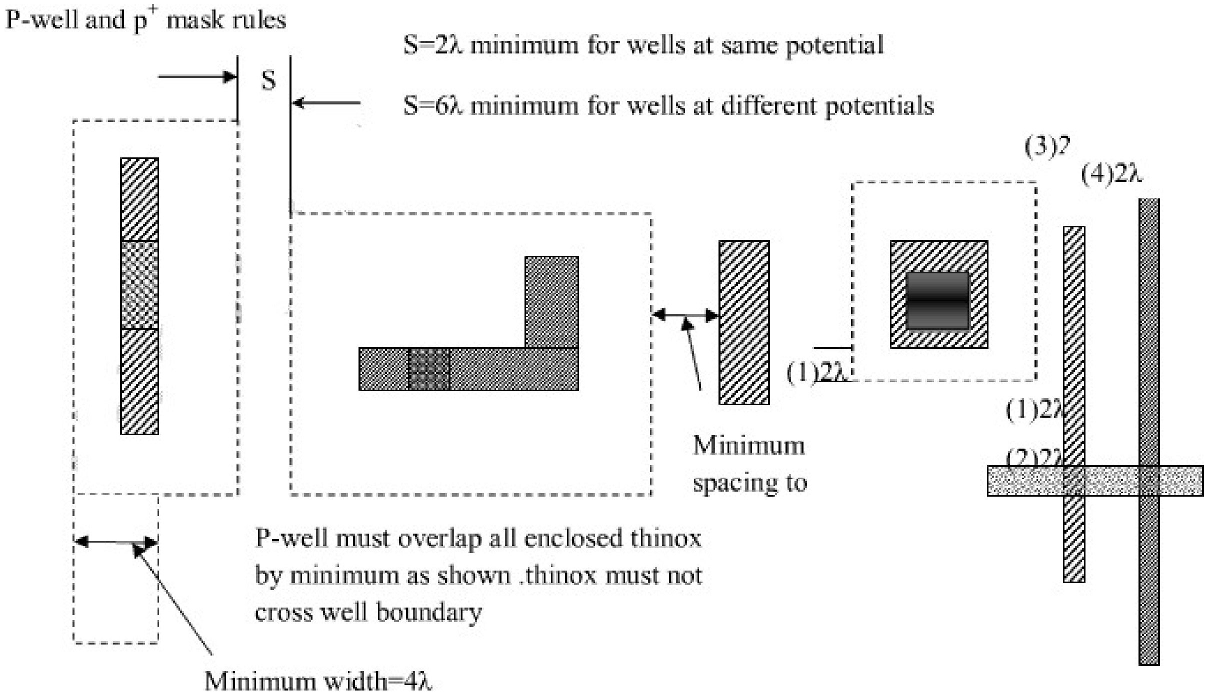
The CMOS fabrication process is more complex than nMOS fabrication. In a CMOS process, there are nearly 100 actual set of industrial design rules. The additional rules are concerned with those features unique to p-well CMOS, such as the p-well and p+ mask and the special 'substrate contacts. The p-well rules are shown in the diagram below



Inthediagram aboveeachofthearrangementscanbemergedintosinglesplitcontacts.



Fromtheabovediagram itisalso clearthatsplitcontacts mayalsobe madewithseparate cuts.



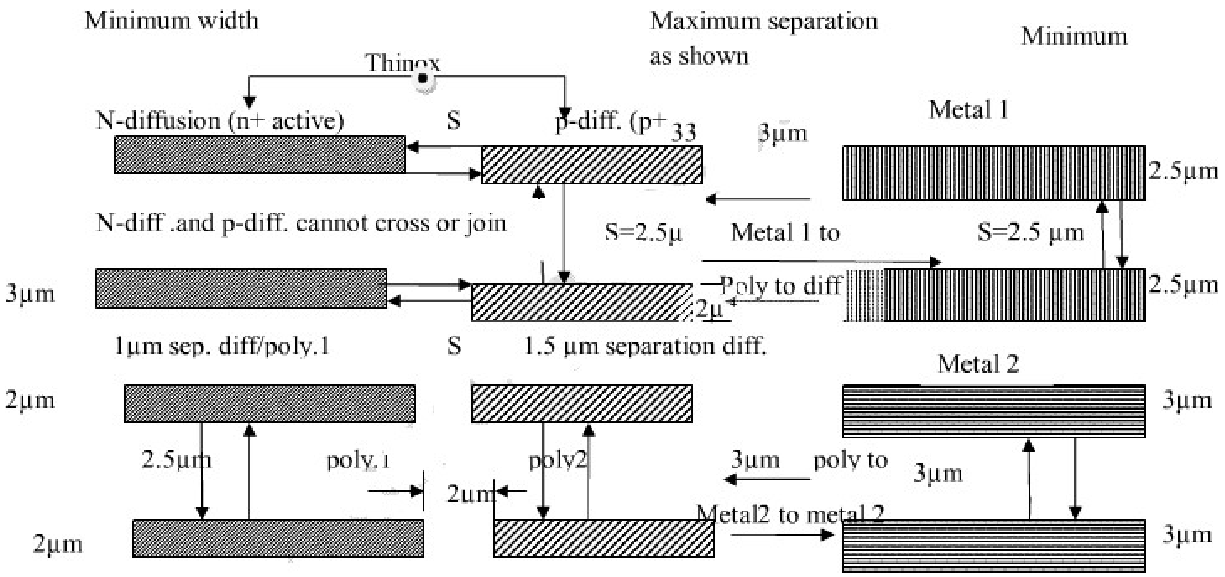
TheCMOSrules aredesigned basedon the extensionsofthe Mead and Conway concepts and also by excluding the butting and buried contacts the new rules for CMOS design are formed. These rules for CMOS design are implemented in the above diagrams.

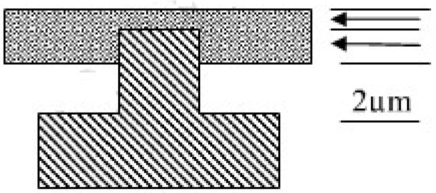
µMCMOS Design rules

The encoding is compatible with that already described where as following extension are made: n-well brown →

Poly 1 → red; poly 2 → orange; diff (n-active) → green; p Diff (p-active) → yellow.

For BiCMOS the following are added: buried n$^+$ sub collector- pale green; p-base--pink.

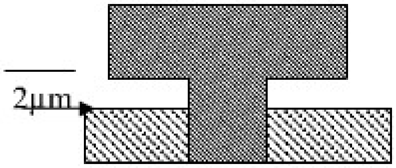




1.5 µm min.edge to edge

1.5 µm min. overlap

1.5µm min. overlap capacitors poly. 1/poly.2



Poly 1 Overlapping poly.2

Poly. 2 overlapping poly.1

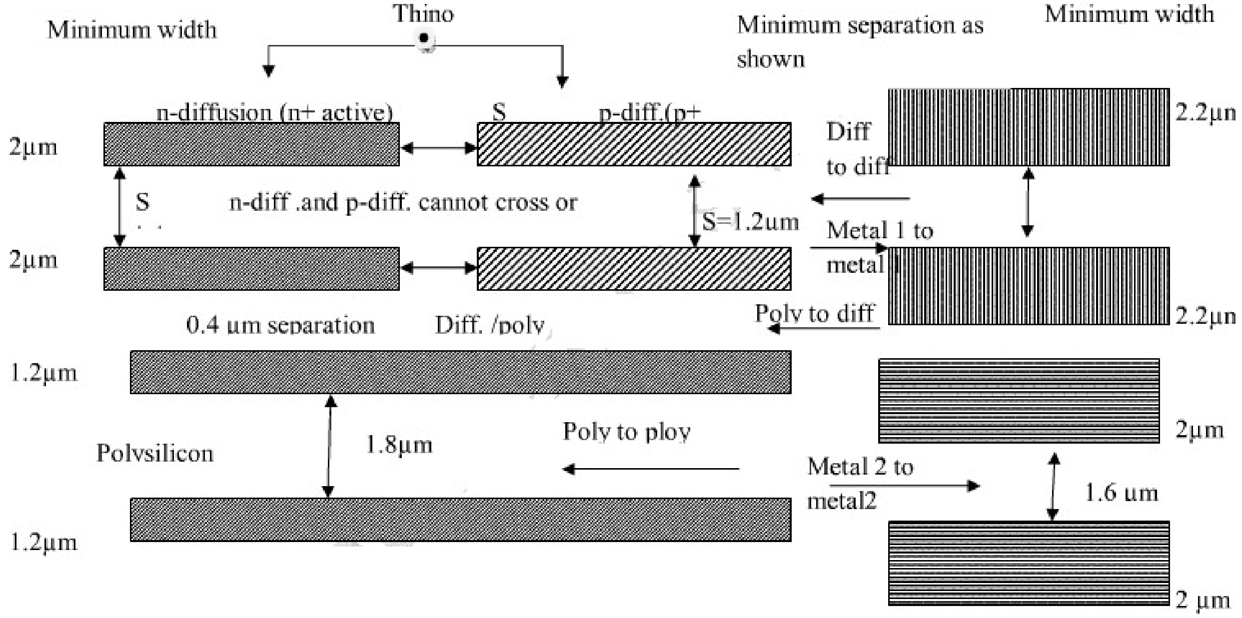
AVOID COINCIDENT EDGES WHERE METAL 1 AND METAL 2 RUNS FOLLOW THE SAME PATH FOR >25µm LENGTH (UNDER LAP METAL 1

Design rules for wires (interconnects) (orbit 2µm CMOS)

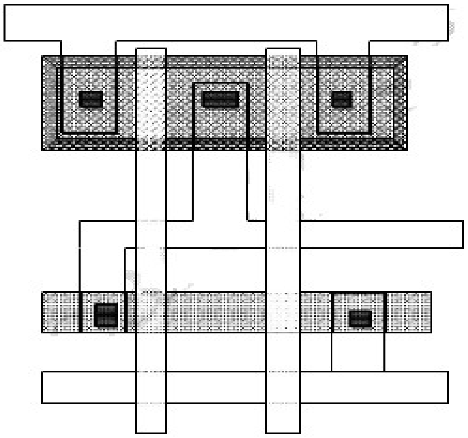
2µm DOUBLE METAL, SINGLE POLY CMOS RULES

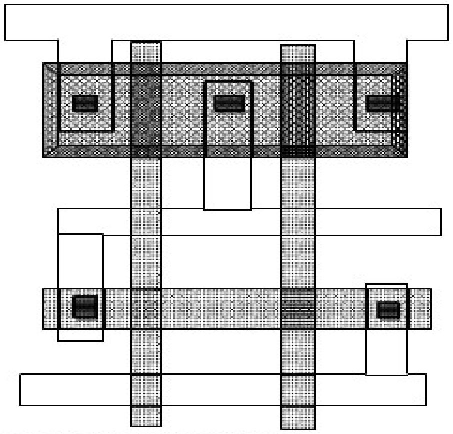
The orbit ™ 1.2µm rules provide improved feature size. A separate set of micro based design rules accompany them

Design rules for wires (interconnects) (orbit 1.2 µm CMOS)

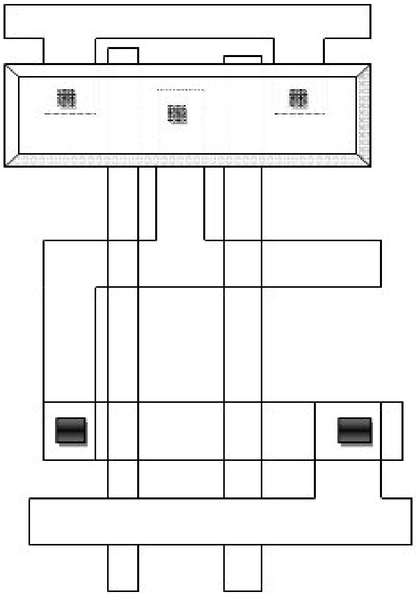


Avoid coincident edges where metal 1 and metal2 runs follow the same path for>25µm length (under lap metal 1 edges by 0.8 µm).

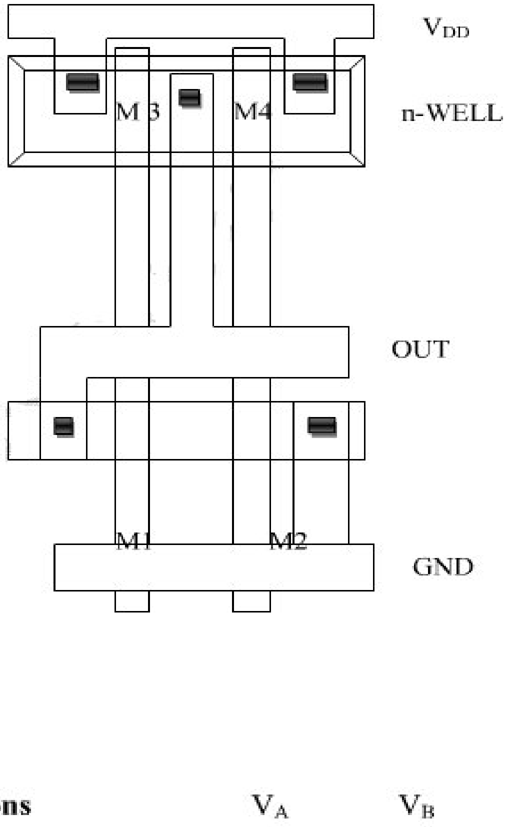




N-WELL AND ACTIVE AREA MASKs POLY MASK -> DEFINE NMOS
AND . ..
....PMOS
TRANSISTORS

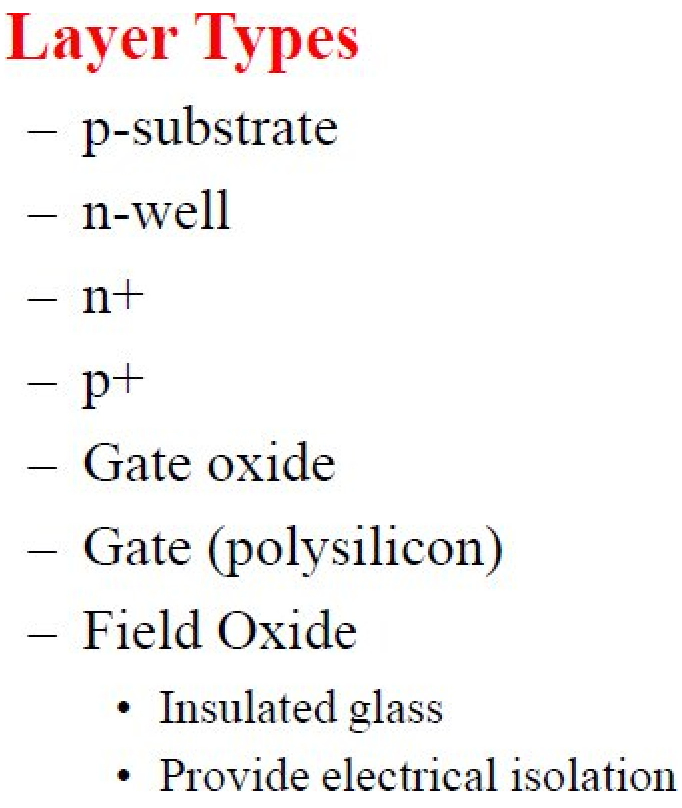


Metal mask for V_{DD}, GND and output connections



METAL –DIFFUSION
CONSTANT MASK

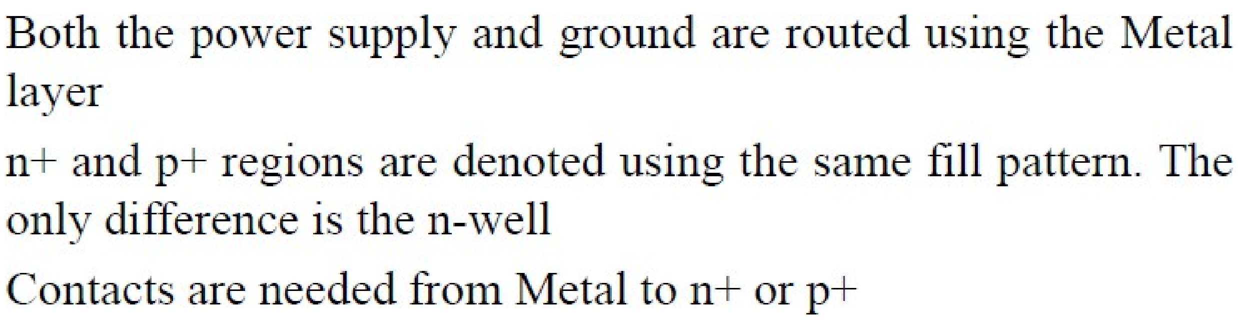
LayoutDiagramsforNMOSandCMOSInvertersandGates



Layer Types

- p-substrate
- n-well
- n+
- p+
- Gate oxide
- Gate (polysilicon)
- Field Oxide
  - Insulated glass
  - Provide electrical isolation

BasicGate Design

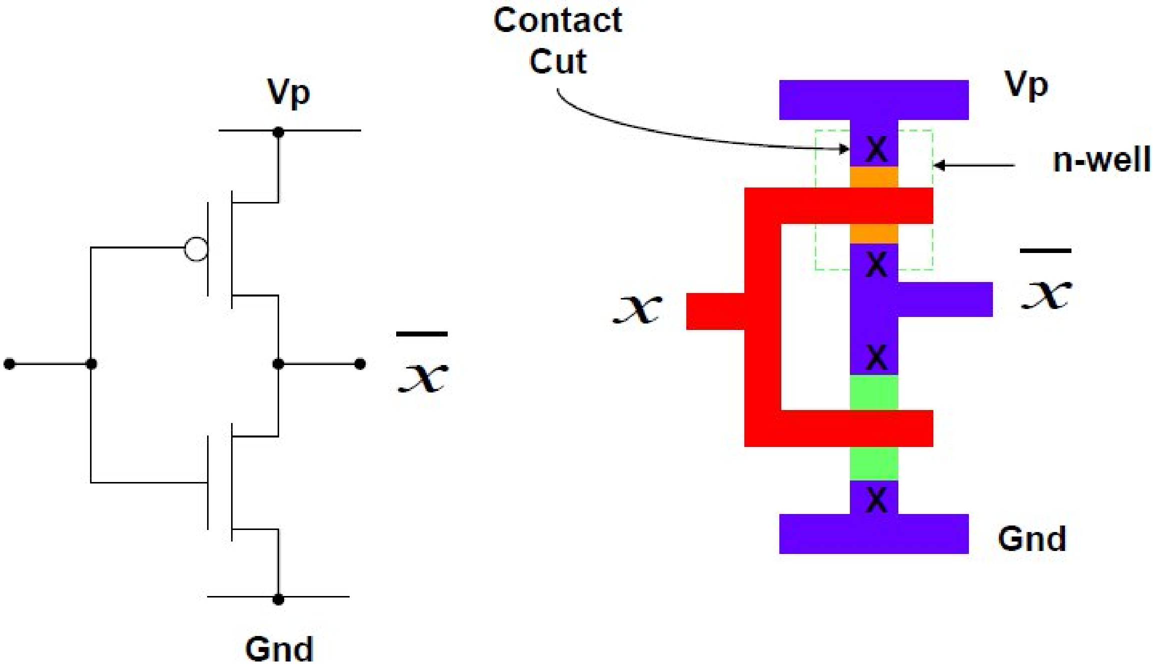


Both the power supply and ground are routed using the Metal layer

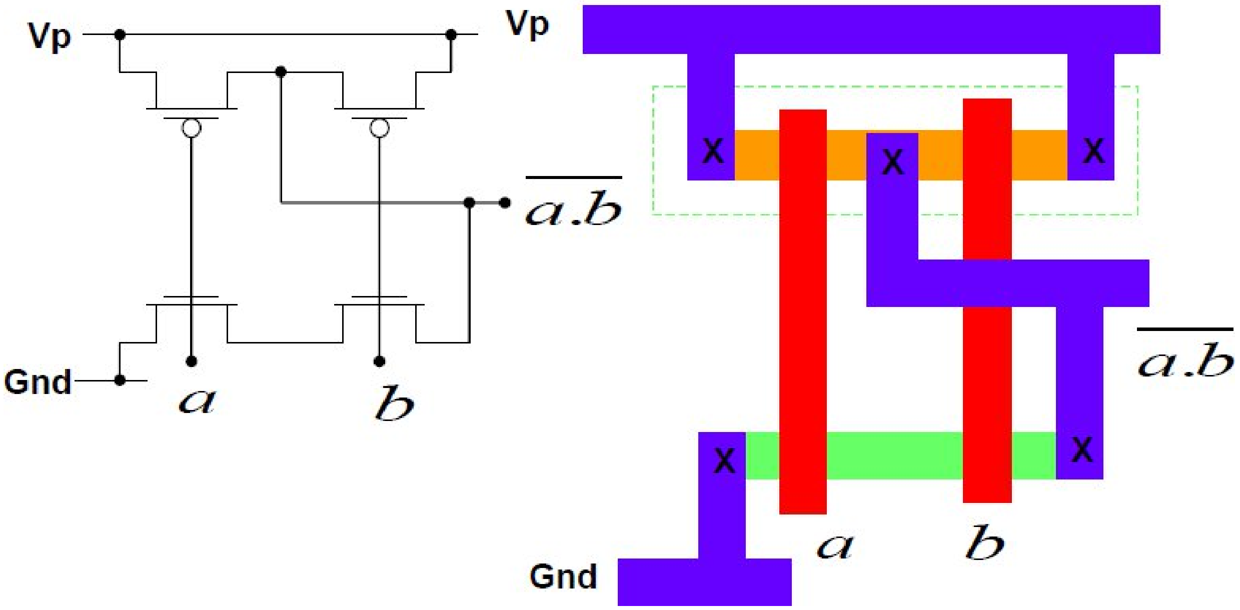
n+ and p+ regions are denoted using the same fill pattern. The only difference is the n-well

Contacts are needed from Metal to n+ or p+

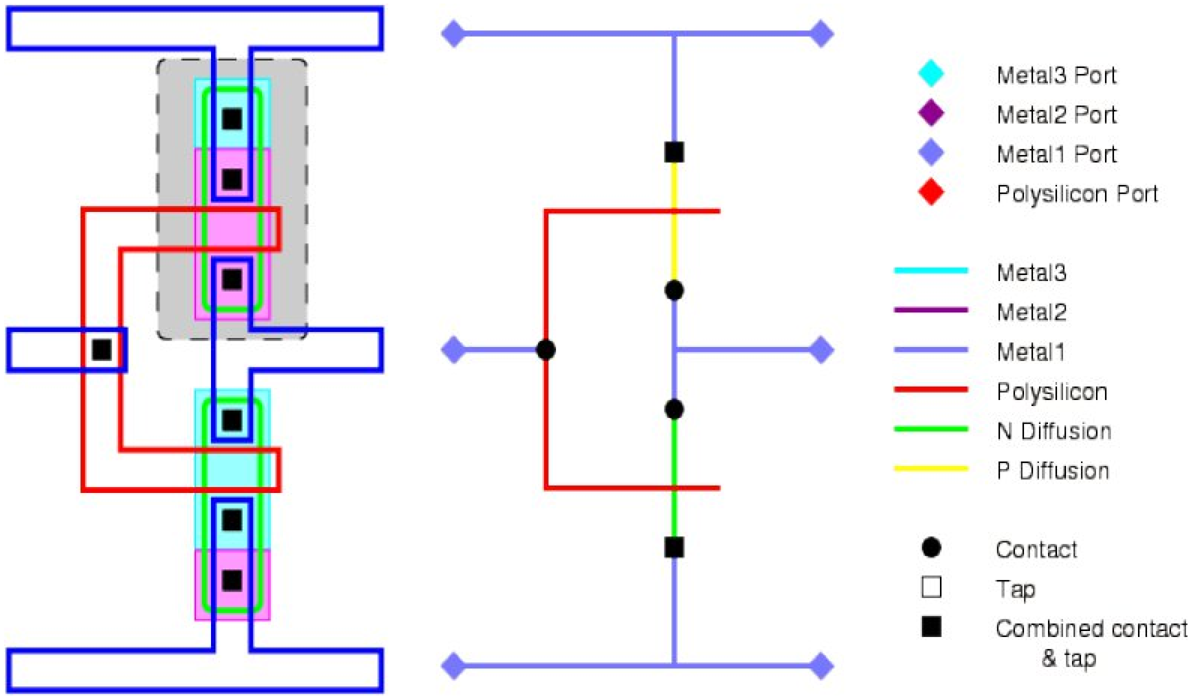
The CMOS NOT Gate



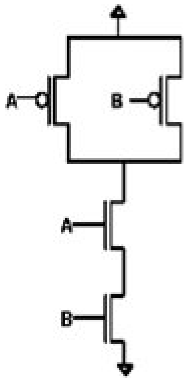
The CMOS NAND Gate

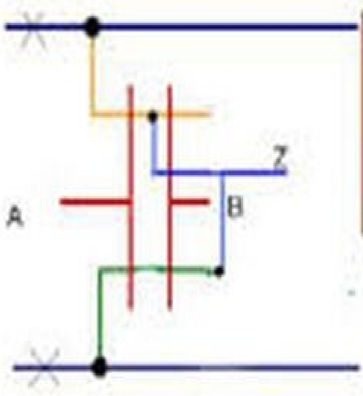


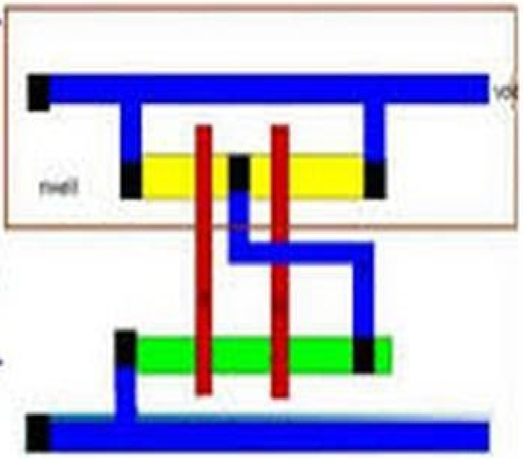
Layout&StickDiagramof CMOSInverter



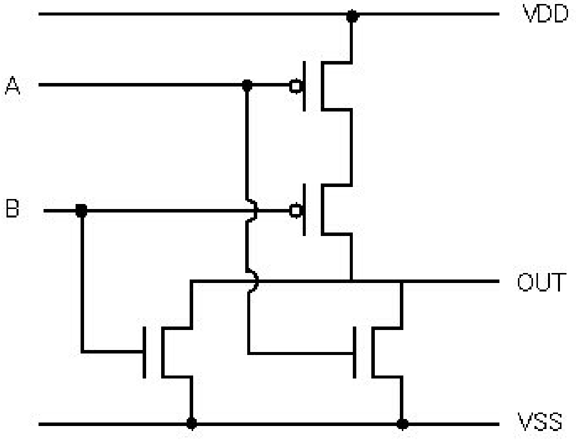
2inputNANDgate



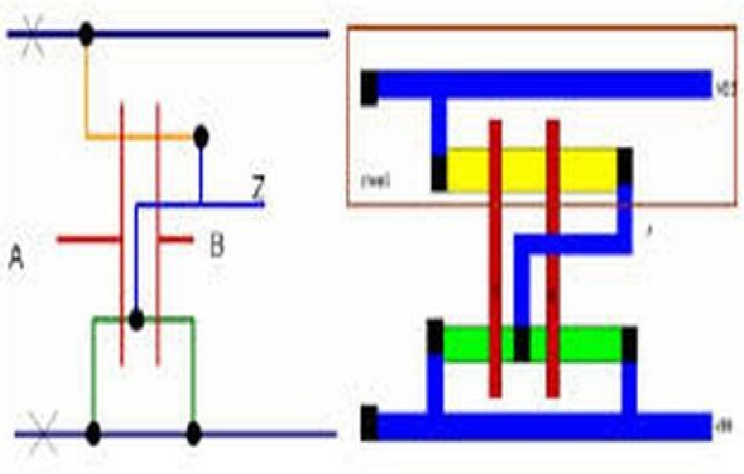




2inputNORgate



NOR gate in CMOS

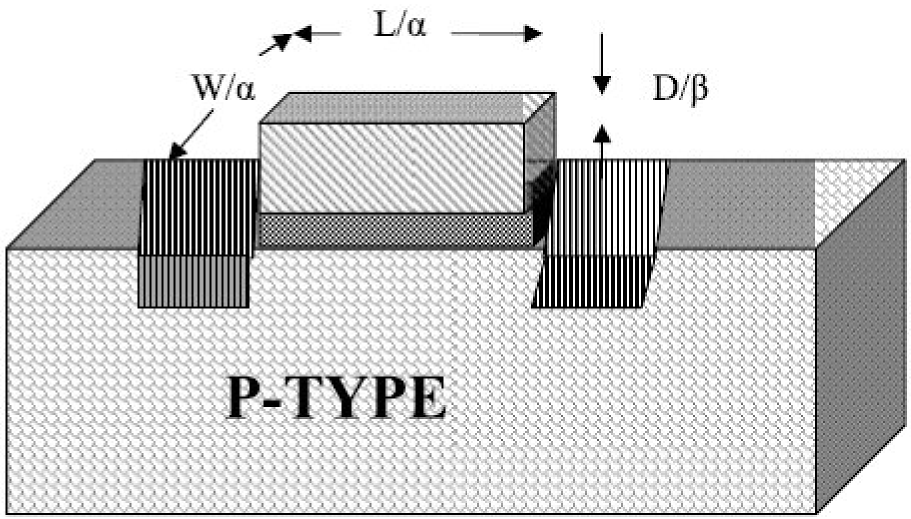


ScalingofMOS circuits

Scaling means to reduce the feature size and to achieve higher packing density of circuitry on a chip, Many figures of merit such as minimum feature size, number of gates on one chip, power dissipation, maximum operational frequency, die size, production cost can be improved by shrinking the dimensions of transistors, interconnections and the separation between features, and by adjusting the doping levels and supply voltages.

SCALING MODELS AND SCALING FACTORS:

The most commonly used models are the constant electric field scaling models and the constant voltage scaling model. One more model called as combined voltage and dimension scaling model is presented recently. The following figure indicates the device dimensions and substrate doping level which are associated with the scaling of a transistor.



Two scaling factors $1/\alpha, 1/\beta$ are used. $1/\beta$ is chosen as the scaling factor for supply voltage V_{DD} and gate oxide thickness D, and $1/\alpha$ is used for all other linear dimensions, both vertical and horizontal to chip surface.

SCALING FACTORS FOR DEVICE PARAMETERS:

GATE AREA AG :

$$A_g = L.W$$

Where L and W are the channel length and width respectively, both are scaled by $1/\alpha$. So Ag is scaled by $1/\alpha^2$

GATE CAPACITANCE PER UNIT ARE C_O OR C_{OX}:

$$C_o = E_{OX}/D$$

Where E_{OX} is the permittivity of the gate oxide (thinox) ($=E_{ins}.E_O$) and D is the gate oxide thickness which is scaled by $1/\beta$

Thus C_O is scaled by $1/1/\beta=\beta$

GATE CAPACITANCE C_g:

$$C_g = C_O\ L.W$$

Thus C_g is scaled by $\beta.1/\alpha^2=\beta/\alpha^2$

PARASITIC CAPACITANCE C_X:

C_X is proportional to A_X/d.

Where d is the depletion width around source or drain which is scaled by $1/\alpha$ and A_X is the area of depletion region around source or drain which is scaled by $1/\alpha_2.1/1/\alpha = 1/\alpha$

CARRIER DENSITY IN CHANNEL Q_{on}

$$\mathbf{Q_{on}=C_o.V_{gs}}$$

Where Qon is the average charge per unit area in the channel in the 'on' state. C_o is scaled by β and V_{gs} is scaled by $1/\beta$.

Thus Q_{on} is scaled by 1.

CHANNEL RESISTANCE R_{on}

$$\mathbf{R_{on}=L/W.Q_{on}.\mu}$$

Where μ is the carrier mobility in the channel and is assumed constant. Thus R_{on} is scaled by $1/\alpha.1/1/\alpha=1$.

GATE DELAY T_d

Td is proportional to $R_{on}.C_g$.

Thus T_d is scaled by β^2/α^4

MAXIMUM OPERATING FREQUENCY F_O:

$$\mathbf{F_o = W/L * \mu C_O V_{DD}/Cg}$$

Or f_o is inversely proportional to delay T_d. Thus f_o is scaled by $1/\beta/\alpha^2 = \alpha^2/\beta$

SATURATION CURRENT I_{DSS}:

$$\mathbf{I_{dss}=C_{o\mu}/2.W/L.\ (V_{gs}-V_t)^2}$$

Nothing that both V_{gs} and V_t are scaled by $1/\beta$,we have I_{dss} is scaled by $\beta(1/\beta)^2=1/\beta$.

CURRENTDENSITYJ:

$$J=I_{des}/A$$

Where A is the cross sectional area of the channel in the 'on' state which is scaled by $1/\alpha^2$

So, J is scaled by $1/\beta/1/\alpha^2=\alpha^2/\beta$.

SWITCHING ENERGY PER GATE E_g:

$$Eg=C_g/2.(V_{DD})^2$$

So Eg is scaled by $\beta/\alpha^2.1/\beta^2=1/\alpha^2\beta$

POWER DISSIPATION PER GATE P_g:

P_g comprise two components such that

$$P_g=P_{gs}+P_d$$

Where the static component

$$P_{gs}= (V_{DD})^2/R_{on}$$

And the dynamic component

$$P_{gd}=E_g f_o$$

It will be seen that both P_{gs} and P_{gd} are scaled by $1/\beta^2$

POWER DISSIPATION PER UNIT AREA:

$$P_a = P_g / A_g$$

So Pa is scaled by $1/\beta^2 / 1/\alpha^2 = \alpha^2/\beta^2$

POWER-SPEED PRODUCT P_T:

$$P_T = P_g . T_d$$

So PT is scaled by $1/\beta^2 . \beta/\alpha^2 = 1/\alpha^2\beta$

LimitationsofScaling:

Scaling may cause a problem which prevents further miniaturization.

Substrate doping: -

The built-in (junction) potential V_B, is small compared with V_{DD}.

(a) Substrate doping scaling factors:

As the channel length of a MOS transistor is reduced, the depletion region widths must also be scaled down to prevent the source and drain depletion regions

N_B is thus maintained at a satisfactory level in the channel region and thus problem is reduced. But depletion width d and built in potential V_B will impose limitations on scaling.

We have $E_{max} = 2V/d$

Where E_{max} is the maximum electric field induced in one-sided step junction

When N_B is increased by α and if $V_\alpha=0$, then V_β is increased by ln α and d is decreased by $\sqrt{\ln \alpha/\alpha}$.

There E is increased by inverse of this factor and reaches E_{crit}

Limits of miniaturization

The minimum size of transistor is determined by both process technology and the physics of the device itself.
Transistor size is defined in terms of channel length L. L can be decreased as long as there is no punch through i.e. The depletion region around source should not come closer to that around the drain. So L must be at least 2d from meeting. Depletion region width d for the junctions is given by

$$D=\sqrt{2E_{si}E_oV/qN_B}$$

Where

E_{si}= relative permittivity of silicon (~12)

E_O= permittivity of free space (=8.85x10^-14)

V=effective voltage across the junction

$V = V_{a+}V_B$

q=electron charge

N_B=doping level of substrate.

V_a= (maximum value =V_{DD})=applied voltage

V_B=built-in (junction) potential

And $V_B = KT/q. \ln (N_B N_D/n_i^2)$

Where N_D is the source or drain doping and n_i is the intrinsic carrier concentration in silicon.

Depletion width

When N_B is increased, the depletion width decreases and V_t increases which is not desirable.

We have $\mathbf{V_{drift} = \mu E}$

V_{drift} is the carrier drift velocity and **L=2d**

Transit time $\boldsymbol{\tau} = \mathbf{L/V_{drift}} \quad \mathbf{=2d/\mu E}$

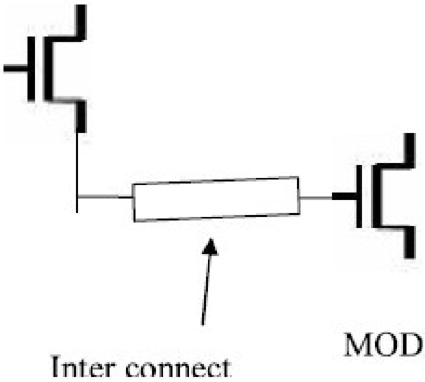
Limits due to interconnect and contact resistance

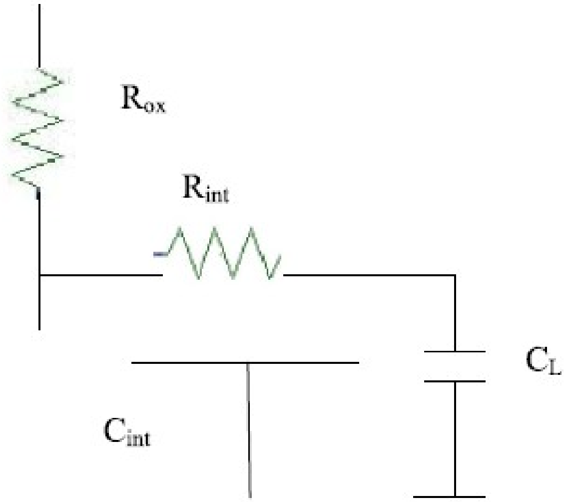
Since the width, thickness and spacing are scaled by $1/\alpha$, cross-section area must be scaled by $1/\alpha^2$ .Thus R is increased by α and I is scaled by $1/\alpha$. so IR drop remains constant. Thus driving capability and noise margins are degraded.

The propagation delay T_p along a single aluminum interconnect can be calculated from the following equation

$$\mathbf{Tp=R_{int}C_{int}+2.3(R_{on}C_{int}+R_{on}C_L+R_{int}C_L)}$$

$$\mathbf{Tp \neq (2.3R_{on}+R_{int}).Cint}$$





MODEL OF METAL INTERCONNECT

Now

$$\mathbf{R_{int}=\rho L/HW}$$

$$\mathbf{C_{int}=E_{ox}[1.15W/t_{ox}+2.28(H/t_{ox})^{0.222}]L}$$

Where R_{on} is the ON resistance of the transistor.

R_{int} is the resistance of the interconnect

C_{int} is the capacitance of interconnect

t_{ox} is the thickness of dielectric oxide.

ρ is the resistivity of interconnect L,W,H are the length, width and height of the interconnect.

Assignmentquestions:

1. Drawthecircuitdiagram;stickdiagramandlayout forCMOSinverter.
2. Explainaboutthevariouslayoutdesignrules.
3. DrawthestaticCMOSlogiccircuitforthefollowingexpression
    1. i)Y=(ABCD)′ii)Y=[D(A+BC)]′
4. ExplainindetailaboutthescalingconceptinVLSIcircuit Design.
5. DrawtheLayoutDiagramsforNANDGateusingnMOS..
6. Explainλ-basedDesignRulesinVLSIcircuit Design.
7. DrawtheLayoutDiagramsforCMOSInverter.
8. Discussaboutthestickdiagramsandtheircorrespondingmasklayout examples
9. Drawthestickdiagramofp-wellCMOSinverterandexplainthe process.
10. Explainaboutthe2µmCMOSDesignrulesanddiscusswithalayout example.
11. DrawandexplainthelayoutforCMOS2-inputNANDgate.
12. DrawtheflowchartofVLSIDesign flowandexplaintheoperationofeachstepindetail.
13. DrawthestickdiagramforthreeinputANDgate.
14. Whatisthepurposeofdesignrule? Whatisthepurposeofstickdiagram? Whatarethe different approaches for describing the design rule? Give three approaches for making contacts between poly silicon and discussion in NMOS circuit.