UNITIII

GATELEVELDESIGNANDBASICCIRCUIT CONCEPTS

GatelevelDesign:

- Logicgatesandothercomplexgates

- Switchlogic

- Alternategatecircuits

BasicCircuitConcepts:

- SheetResistanceRsanditsconceptsto MOS

- AreaCapacitancescalculations

- InverterDelays

- Fan-inandfan-out.

CMOSLogicgatesandothercomplexgates

Name	Logic symbol	Logic equation
INVERTER		Out=~in;
AND		Out=a&b;
NAND		Out=~(a.b);
OR		Out=(a|b);
NOR		Out=~(a|b);
XOR		Out=a^b;
XNOR		Out=~(a^b);

CMOSlogicgateconcept:

The structure of a CMOS logic gate is based on complementary networks of n-channel and p-channel MOS circuits. Recall that the pMOS switch is good at passing logic signal '1', while nMOS switches are good at passing logic signal '0'. The operation of the gate has two main configurations:

- the nMOS switch network is closed, the output s=0 (figure 6-6 left)
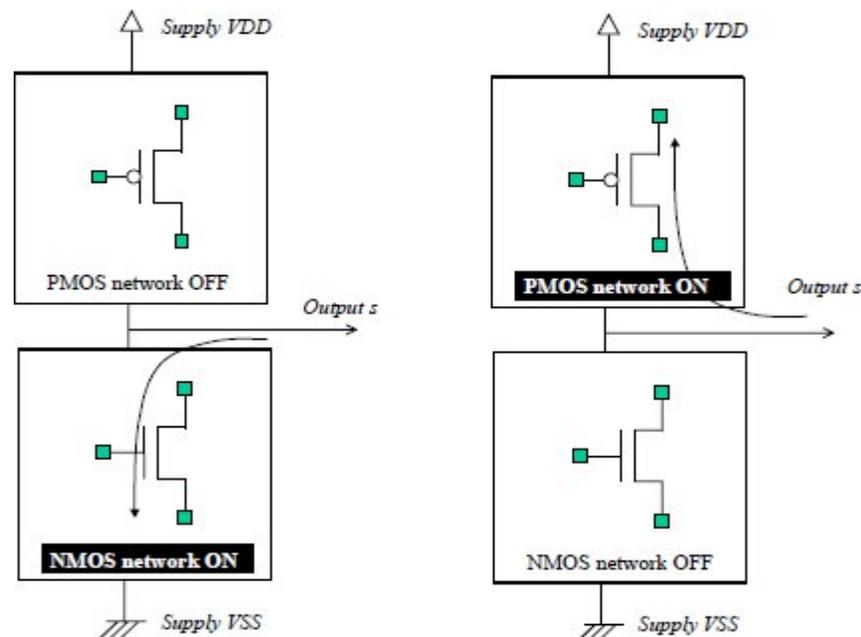- the pMOS switch network is closed, the output s=1 (figure 6-6 right)

Fig. 6-6. General structure of a CMOS basic gate

Using complementary pairs of nMOS and pMOS devices, either the lower nMOS network is active, which ties the output to ground, either the upper pMOS network is active, which ties the output to VDD. In conventional CMOS basic gates, there should exist no combination when both nMOS and pMOS networks would be ON. If this case had

happened, a resistive path would be created between VDD and VSS supply rails. The situation where neither nMOS and pMOS networks would be OFF should also be avoided, because the output would be undetermined.

CMOSStaticlogic

Static, fully complementary CMOS gate designs using inverter, NAND and NOR gates can build more complex functions. These CMOS gates have good noise margins and low static power dissipation at the cost of more transistors when compared with other CMOS logic designs. CMOS static complementary gates have two transistor nets (nMOS and pMOS) whose topologies are related. The pMOS transistor net is connected between the power supply and the logic gate output, whereas the nMOS transistor topology is connected between the output and ground (Fig. 5.1). We saw this organisation with the NAND and NOR gates, but we point out this topology to lead to a general technique to convert Boolean algebra statements to MOS electronic circuits.
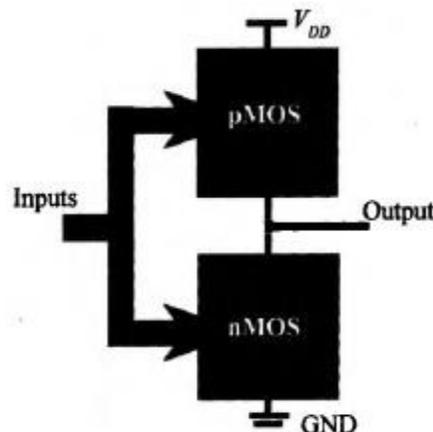

**Fig. 5.1** Standard configuration of a CMOS complementary gate.

DesignProcedure:

1. Derive the nMOS transistor topology with the following rules:
   • Product terms in the Boolean function are implemented with series-connected nMOS transistors.
   • Sum terms are mapped to nMOS transistors connected in parallel.
2. The pMOS transistor network has a dual or complementary topology with respect to the nMOS net. This means that serial transistors in the nMOS net convert to parallel transistors in the pMOS net, and parallel connections within the nMOS block are translated to serial connections in the pMOS block.
3. Add an inverter to the output to complete the function if needed. Some functions are inherently negated, such as NAND and NOR gates, and do not need an inverter at the output state. An inverter added to a NAND or NOR function produces the AND and OR function. The examples below require an inverter to fulfil the function.

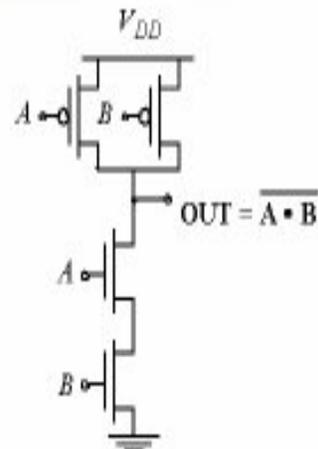## Examples:

Example Gate: NOR

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table of a 2 input NOR gate

$$OUT = \overline{A + B}$$
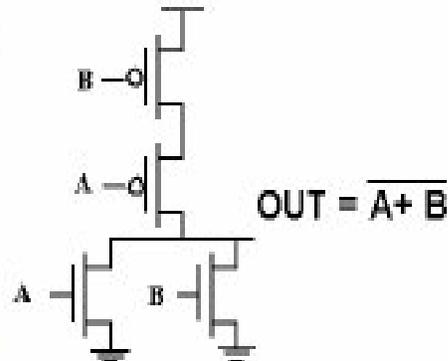
Example Gate: NAND

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate

$$OUT = \overline{A \cdot B}$$

PDN: $G = A\,B \quad \Rightarrow \quad$ Conduction to GND

PUN: $F = \overline{A} + \overline{B} = \overline{AB} \Rightarrow$ Conduction to V_{DD}

$$\overline{G(In_1, In_2, In_3, \ldots)} = F(\overline{In_1}, \overline{In_2}, \overline{In_3}, \ldots)$$

1.

Design a complementary static CMOS XOR gate at the transistor level. The XOR gate Boolean expression F has four literals and is $F = \bar{x}y + x\bar{y}$.

F is the sum of two product terms. The design steps are:

1. Derive the nMOS transistor topology with four transistors, one per literal in the Boolean expression. The transistors driven by $\bar{x}$ and y are connected in series, as well as the devices driven by x and $\bar{y}$. These transistor groups are connected in parallel, since they are additive in the Boolean function. The signals and their complements are generated using inverters (not shown). The nMOS transistor net is shown in Fig. 5.2.
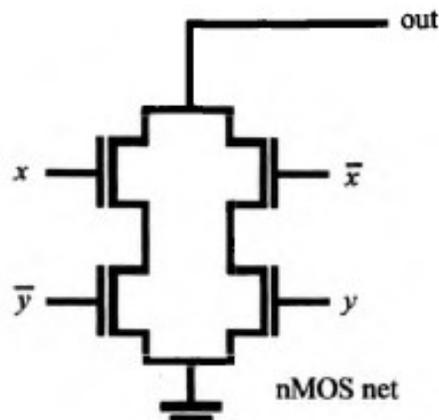

Fig. 5.2

2. Implement the pMOS net as a dual topology to the nMOS net. The pMOS transistors driven by $\bar{x}$ and y are connected in parallel, as are the devices driven by x and $\bar{y}$ (Fig. 5.3). These transistor groups are connected in series, since they are parallel connected in the nMOS net. The *out* node now implements $\bar{F}$.
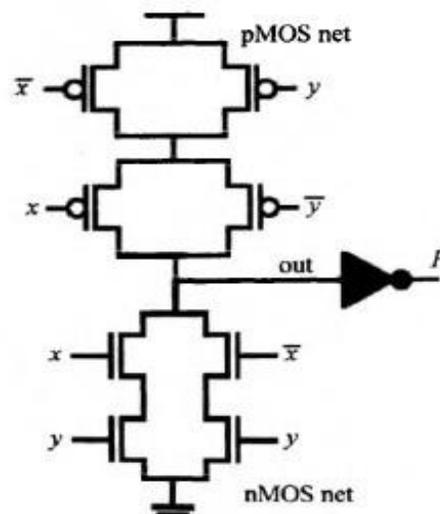

Fig. 5.3

3. Finally, add an inverter to obtain the function F, so that $F = \overline{out}$.

2. Design the nMOS transistor net for a Boolean function $F = x + \{\bar{y} \cdot [z + (t \cdot \bar{w})]\}$. We design this gate with a top-down approach. The nMOS transistor network is connected between the output and ground terminals, i.e., the lower box in Fig. 5.4(b). The higher-level function F is a sum of two terms:

$F = x + \{operation\ A\}$ where operation A stands for the logic within the brackets of F. The transistor version of this sum is shown in Fig. 5.4(a).
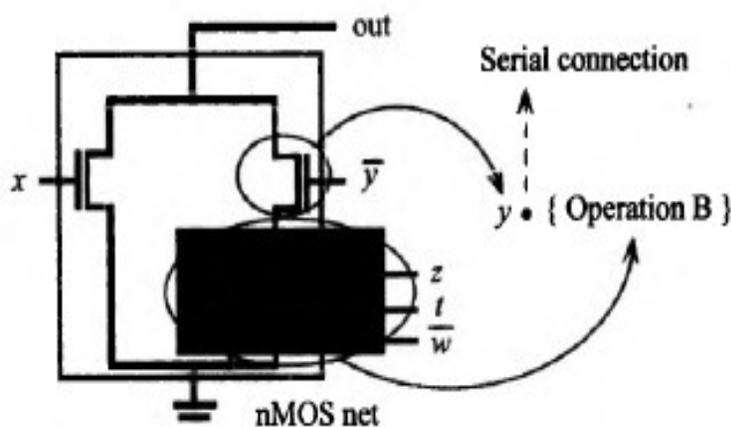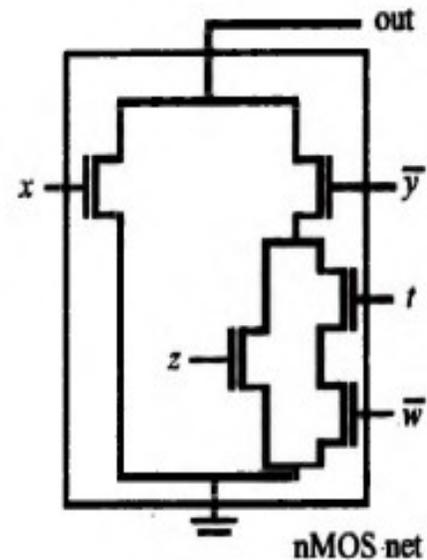

Fig. 5.4(a)   Fig. 5.4(b)

Hence, the design topology is a transistor controlled by input $\bar{y}$ in series with a third box that will implement *operation B*, as shown in Fig. 5.4. We then design the topology of box B. This is a transistor controlled by input z, in parallel with two transistors connected in series; one controlled by input t, and the other by input $\bar{w}$. The complete nMOS network is shown in Fig. 5.4(b). Once the nMOS block is designed, we build the pMOS block with a dual topological structure and then connect an inverter to its output, as shown in Fig. 5.6.

ComplexGates:

Complex Gate

◆ We can form complex combinational circuit function in a complementary tree. The procedure to construct a complementary tree is as follow:-

- Express the boolean expression in an inverted form
- For the n-transistor tree, working from the inner-most bracket to the outer-most term, connect the **OR** term transistors in parallel, and the **AND** term transistors in series
- For the p-transistor tree, working from the inner-most bracket to the outer-most term, connect the **OR** term transistors in series, and the **AND** term transistors in parallel

$$\overline{A^*B + C^*(D+E)}$$
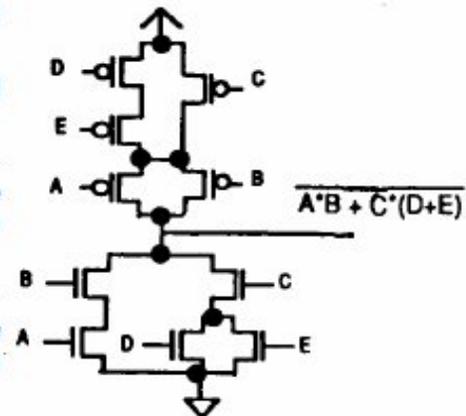
Example Gate: COMPLEX CMOS GATE

$$OUT = \overline{D + A\cdot(B+C)}$$
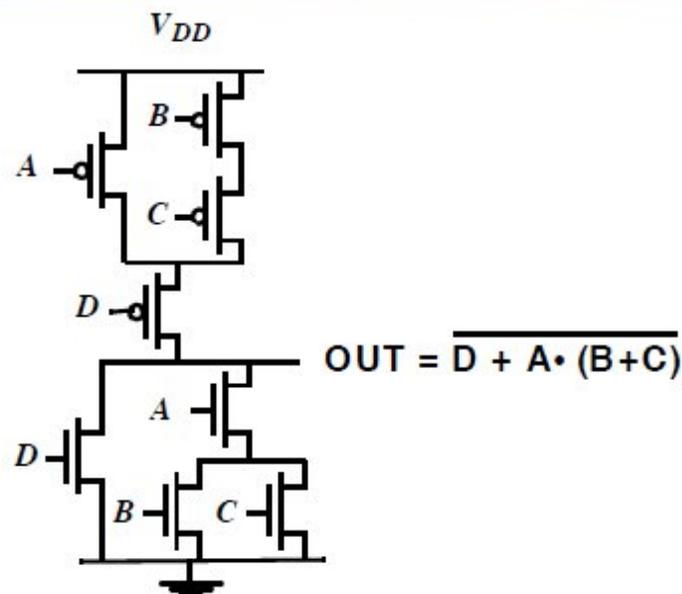
Transmissiongatelogic:

A **transmission gate** is an electronic element. It is a good non-mechanical relay, built with CMOS technology. Sometimes known as an analog gate, analog switch or electronic relay depending on its use. It is made by the parallel combination of an nMOS and a pMOS transistor with the input at the gate of one transistor being complementary to the input at the gate of the other.

A *transmission gate* is a essentiallya switchthat connects two points. Inorderto pass 0's and 1's equally well, a pair of transistors (one N-Channel and one P-Channel) is used as shown below:
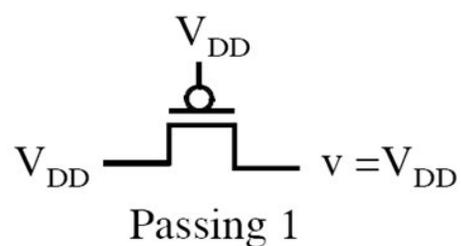

Circuit   Symbol
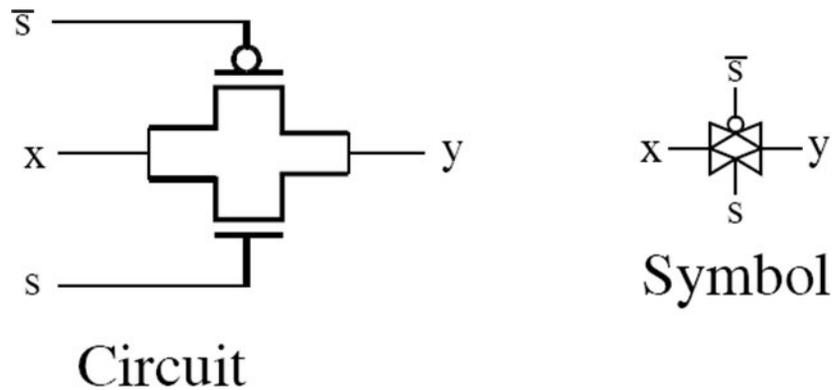
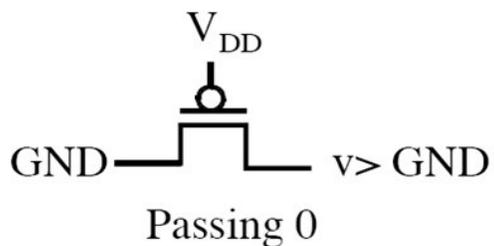Whens=1 thetwotransistorsconductand connect xandy

Thetoptransistorpassesxwhenit is1andthe bottomtransistorpassesxwhenit is0 When s = 0 the two transistor are cut off disconnecting x and y

N-ChannelMOSTransistorspassa0betterthana 1

Passing 0   Passing 1
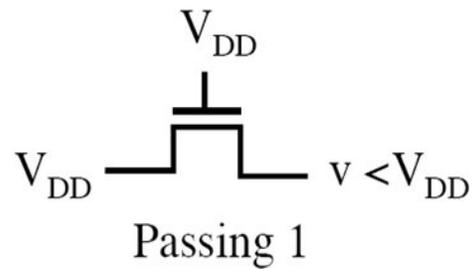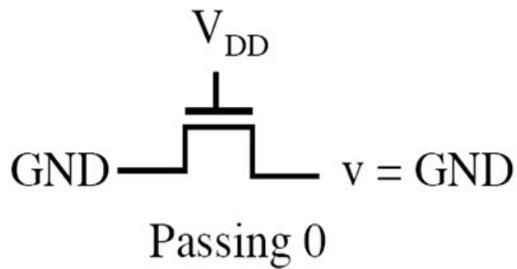
P-ChannelMOS Transistorspassa1 betterthana 0

Passing 0   Passing 1

This isthereasonthat N-Channeltransistorsareused inthepull-downnetworkand P-Channelin the pull-up network of a CMOS gate. Otherwise the noisemargin would be significantlyreduced.

Tristategates:

Many logic gates require a tri-state output—high, low, and high-impedance states. The high-impedance state is also called the high-Z state, and is useful when connecting many gate outputs to a single line, such as a data bus or address line. A potential conflict would exist if more than one gate output tried to simultaneously control the bus line. A controllable high-impedance-state circuit solves this problem.

There are two ways to provide high impedance to CMOS gates. One way provides tristate output to a CMOS gate by connecting a transmission gate at its output (Fig. 5.7). The control signal C sets the transmission gate conducting state that passes the non-tristated inverter output $\overline{out}$ to the tri-stated gate output out. When the transmission gate is off ($C = 0$), then its gate output is in the high-impedance or floating state. When $C = 1$, the transmission gate is on and the output is driven by the inverter.
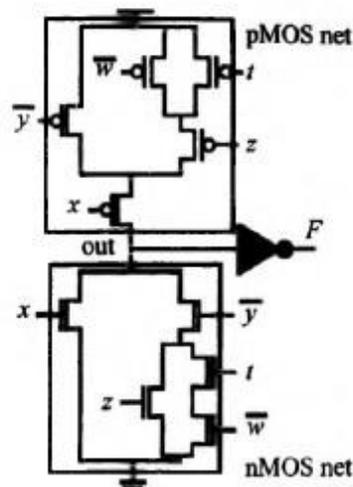

Fig. 5.6

A transmission gate connected to the output provides tri-state capability, but also consumes unnecessary power. The design of Fig. 5.7 contributes to dynamic power each time that the input and output ($\overline{out}$) are switched, even when the gate is disabled in the tri-state mode. Parasitic capacitors are charged and discharged. Since the logic activity at the input does not contribute to the logic result while the output is in tri-state, the power consumption related to this switching is **wasted.**

PassTransistorLogic

Pass Transistor Logic (PTL) describes severallogic families used in the design of integrated circuits. It reduces the count oftransistorsused to make different logicgates, by eliminating redundant transistors.

Advantages are the low number of transistors and the reduction in associated interconnects. The drawbacks are the limited driving capability of these gates and the decreasing signal strength when cascading gates. These gates do not restore levels since their outputs are driven from the inputs, and not from V_{DD} or ground.

A typical CMOS design is the gate-level multiplexer (MUX) shown in Fig. 5.9 for a 2-to-1 MUX
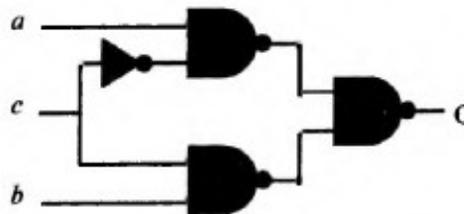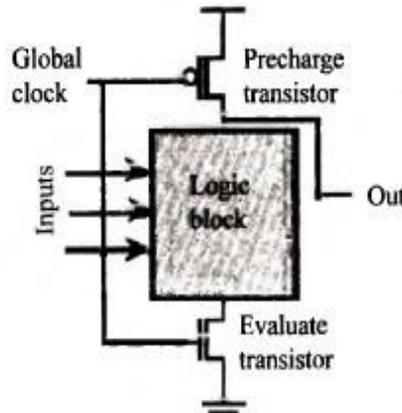

Fig. 5.9 (a) Standard 2-to-1 MUX design. (

DynamicCMOSlogic:

BasicStructureofa dynamicCMOS gate

This logic looks into enhancing the speed ofthe pullup device byprecharging the output node to V_{dd}. Hence we need to split the working of the device into precharge and evaluate stage for whichwe need a clock. Hence it is called as dynamic logic. The output node is precharged to $V_{dd}$by the pmos and is discharged conditionally through the nmos. Alternatively you can also have a p block and precharge the n transistor to V_{ss}. When the clock is low the precharge phase occurs.ThepathtoVssisclosedbythenmosi.e.thegroundswitch.Thepulluptimeis

improved because of the active pmos which is already precharged. But the pull down time increases because of the ground switch.

Thereareafewproblemsassociatedwiththedesign,like

- Inputshavetochangeduringtheprechargestageandmustbestableduringthe

  evaluate. If this condition cannot occur then charge redistribution corrupts the output node.

- A simple single dynamic logic cannot be cascaded. During the evaluate phase the first gate willconditionallydischarge but bythe time the second gate evaluates, there is going to be a finite delay. By then the first gate may precharge.

MeritsandDemerits:

1. They use fewer transistors and, therefore, less area.
2. Fewer transistors result in smaller input capacitance, presenting a smaller load to previous gates, and therefore faster switching speed.
3. Gates are designed and transistors sized for fast switching characteristics. High performance circuits use these families.

The logic transition voltages are smaller than in static circuits, requiring less time to switch between logic levels.
The disadvantages of dynamic CMOS circuits are

1. Each gate needs a clock signal that must be routed through the whole circuit. This requires precise timing control.
2. Clock circuitry runs continuously, drawing significant power.
3. The circuit loses its state if the clock stops.
4. Dynamic circuits are more sensitive to noise.
5. Clock and data must be carefully synchronized to avoid erroneous states.

DominoCMOSLogic

This logic is the most common form of dynamic gates, achieving a 20%-50% performance increase over static logic. When the nMOS logic block discharges the out node during evaluation (Fig. 5.12), the inverter output out goes high, turning off the feedback pMOS. When out is evaluated high (high impedance in the dynamic gate), then the inverter output goes low, turning on thefeedbackpMOS deviceand providing a low impedance pathtoV_{DD}, This prevents the out nodefrom floating, making it less sensitive to node voltage drift, noise and current leakage.

Domino CMOS allows logic gate cascading since all inputs are set to zero during precharge,avoiding erroneous evaluation from different delays. This logic allows static operation from the feedbacklatchingpMOS,butlogicevaluationstillneedstwosubcycles:prechargeandevaluation.

Dominologicuses onlynon-invertinggates,making itanincompletelog family.Toachieve inverted logic, a separate inverting path running in parallel with the non inverted one must be designed.
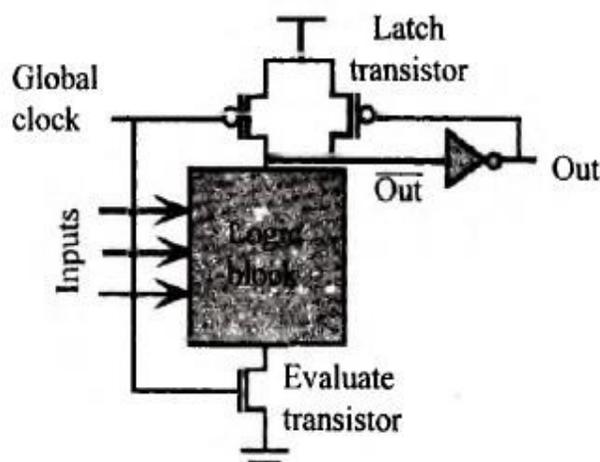

Fig. 5.12 Domino CMOS logic gate with feedback transistor.

Multiple output domino logic (MODL) is an extension of domino logic, taking internal nodes of the logic block as signal outputs, thus saving area, power, and performance. Compound domino logic is another design that limits the length of the evaluation logic to prevent charge sharing, and adds other complex gates as buffer elements (NAND, NOR, etc. instead of inverters) to obtain more area compaction. Self-resetting domino logic (SRCMOS) has each gate detect its own operating clock, thus reducing clock overhead and providing high performance.

NORA CMOS Logic. This design alternative to domino CMOS logic eliminates the output buffer without causing race problems between clock and data that arise when cascading dynamic gates. NORA CMOS (No-Race CMOS) avoids these race problems by cascading alternate nMOS and pMOS blocks for logic evaluation. The cost is routing two complemented clock signals. The cascaded NORA gate structure is shown in Fig. 5.13. When the global clock (GC) is low ($\bar{GC}$ high), the nMOS logic block output nodes are precharged high, while outputs of gates with pMOS logic blocks are precharged low. When the clock changes, gates are in the evaluate state.
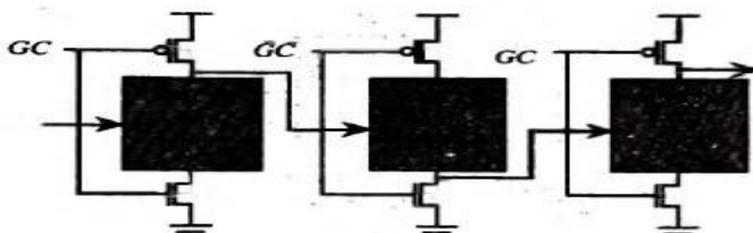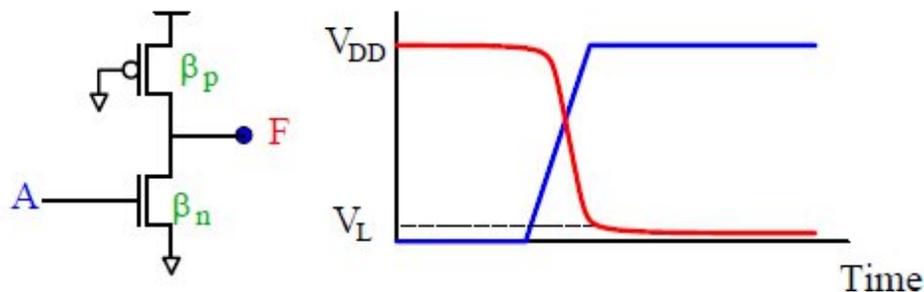

Fig. 5.13 NORA CMOS cascaded gates.

Pseudo–NMOSLogic:

pseudo-NMOS inverter

The inverter that uses a p-device pull-up or loads that has its gate permanently ground.Ann-devicepull-downordriver isdrivenwiththe input signal. Thisroughlyequivalent to useof adepletionload is**NMOS**technologyand isthuscalled '**Pseudo-NMOS**'.Thecircuit isused ina variety of CMOS **logic** circuits.

The low output voltage can be calculated as
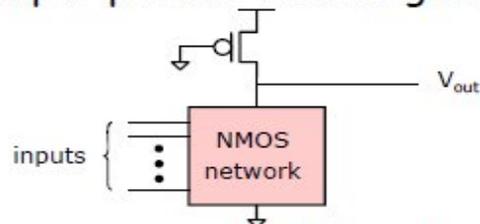
$$\beta_n (V_{DD} - V_{tn}) V_L = \frac{\beta_P}{2} (V_{DD} - |V_{tp}|)^2$$

for $V_{tn} = -V_{tp} = V_t$

$$V_L = \frac{\beta_P}{2\beta_n} (V_{DD} - V_T)$$

Thus V_L depends strongly on the ratio β_p / β_n
The logic is also called ratioed logic

An N-input pseudo-NMOS gate

Features of pseudo-NMOS logic
■ Advantages
 □ Low area cost→only N+1 transistors are needed for an N-input gate
 □ Low input gate-load capacitance→C_{gn}
■ Disadvantage
 □ Non-zero static power dissipation

BasicCircuitConcepts:

SheetResistanceRsanditsconceptstoMOS

Thesheet resistance isa measureofresistanceofthinfilmsthat haveauniformthickness. It is commonly used to characterize materials made by semiconductor doping, metal deposition, resistive paste printing, and glass coating.

Example ofthese processes are: doped semiconductor regions (eg: silicon or polysilicon) and resistors.

Sheet resistance is applicable to two-dimensional systems where the thin film is considered to be a two-dimensional entity. It is analogous to resistivity as used in three-dimensional systems. When the term sheet resistance is used, the current must be flowing along the plane of the sheet, not perpendicular to it.
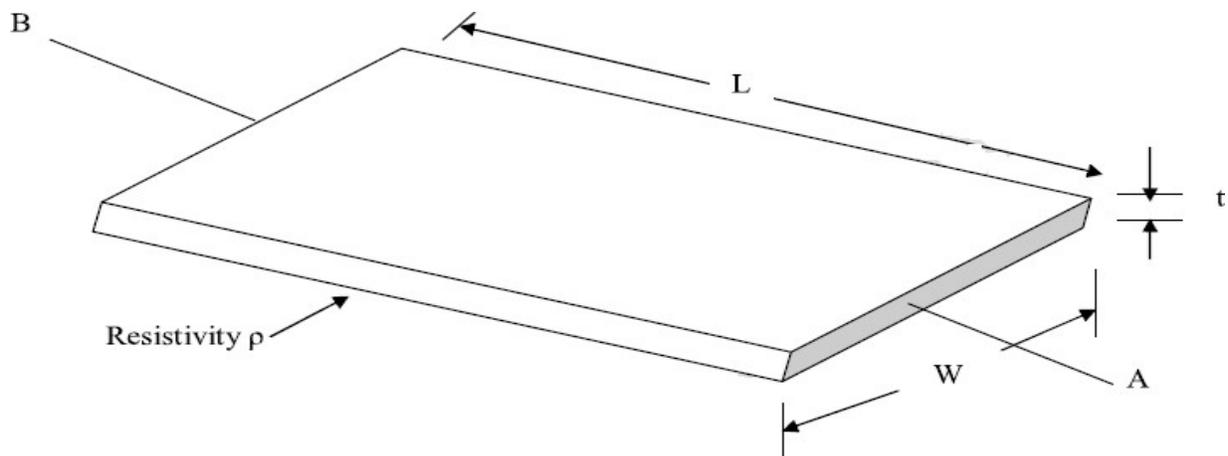
Model:

Consider a uniform slab of conducting material of resistivity ρ, of width W, thickness t, and length between faces L as shown below:

$$R_{AB} = \frac{\rho L}{tW} \quad \text{ohm}$$

Where A = cross section area.

Thus $R_{AB} = \frac{\rho L}{tW}$ ohm.

When L = W, i.e. a square resistive material, then

$$R_{AB} = \frac{\rho}{t} = R_s$$

Where R_s =ohm per square or sheet resistance.

Thus $R_s = \frac{\rho}{t}$ ohm per square.

It is completely independent of the area of the square.

TypicalsheetresistanceRsofMOSlayers

| Layer	R_s ohm per square		
	5μm	Orbit	1.2μm
Metal	0.03	0.04	0.04
Diffusion	$10 \rightarrow 50$	$20 \rightarrow 45$	$20 \rightarrow 45$
Silicide	$2 \rightarrow 4$	-	-
Polysilicon	$15 \rightarrow 100$	$15 \rightarrow 30$	$15 \rightarrow 30$
n-transistor channel	10^4	2×10^4	2×10^4
p-transistor channel	2.5×10^4	4.5×10^4	4.5×10^4

SHEET RESISTANCE CONCEPT APPLIED TO MOS TRANSISTORS AND INVERTERS

The simple n-type pass transistor has a channel length $L = 2\lambda$ and a channel width $W = 2\lambda$. The channel is square
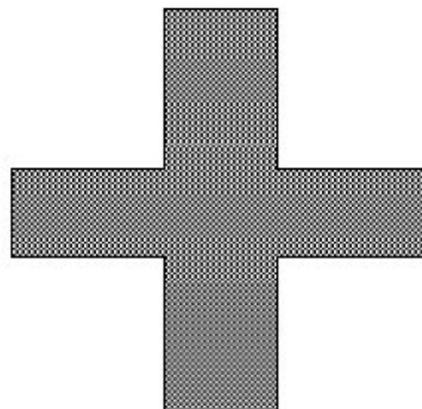
$$R = \text{square} \times R_s \frac{Ohm}{square} = R_s = 10^4 \text{ ohm.}$$

The length to width ratio, denoted by Z is 1:1 in this case. Consider one more structure as in diagram below.

L = 8 λ and W = 2 λ
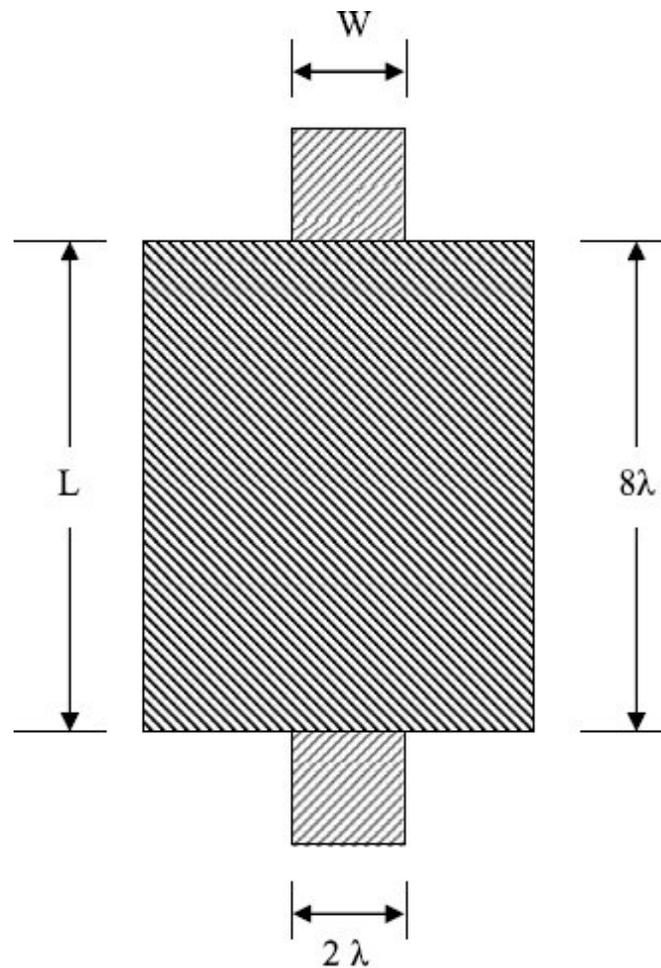
$$Z = \frac{L}{W} = 4$$

Channel resistance R = Z R$_s$ = 4 X 10^4 Ohm.

This channel can be taken as four 2 λ X 2 λ squares in series.

Calculation of ON Resistance of a Simple Inverter

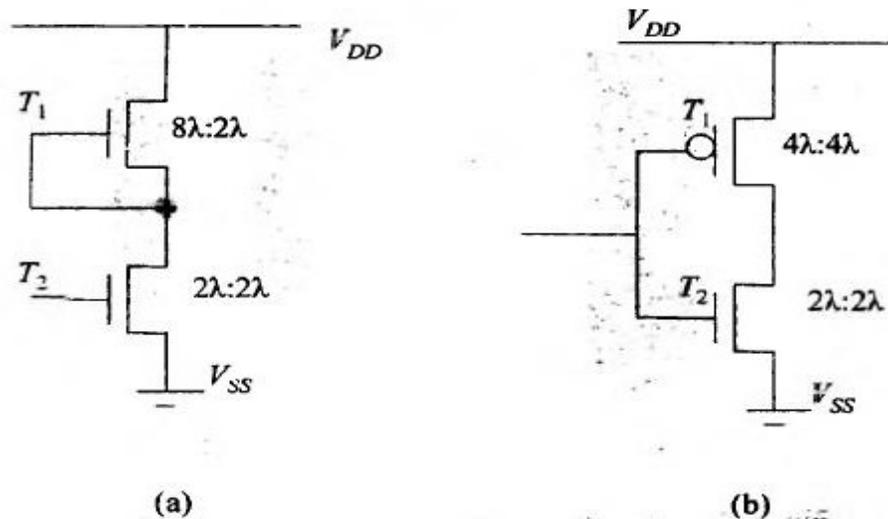Consider the simple nMOS inverter in Fig.

Fig.(a)NMOS Inverter(b)CMOSInverterresistancecalculations

- For the pull-up transistor (depletion mode MOSFET) the $L{:}W$ value is 4:1, hence the value of Z is 4. $R_{on} = 4$ and value of on resistance is $4R_s$, i.e., $4 \times 10^4 = 40$ kΩ.
- Similarly, for the pull down transistor (enhancement mode MOSFET) the $L{:}W$ value is 1:1 hence the value of Z is 1. $R_{on} = 1$ and value of resistance is $1R_s$, i.e., $1 \times 10^4 = 10$ kΩ.
- $Z_{p.u}$ to $Z_{p.d} = 4$:1 hence the ON resistance between V_{DD} and V_{SS} is the total series resistance, i.e., 40 kΩ + 10 kΩ = 50 kΩ.

Consider the simple CMOS inverter in Fig.

- For the pull-up transistor (p-enhancement mode MOSFET) the $L{:}W$ value is 1:1, hence, the value of Z is 4. $R_{on} = 4$ and value of on resistance is $4 R_s$, i.e., $1 \times 25 \times 10^4 = 25$ kΩ (from the table value of R_s for p-channel transistor is 2.5×10^4 ohm/square).
- Similarly, for the pull down transistor (n-enhancement mode MOSFET) the $L{:}W$ value is 1:1 hence the value of Z is 1. $R_{on} = 1$ and value of resistance is $1 R_s$, i.e., $1 \times 10^4 = 10$ kΩ.
- In this case, there is no static resistance between V_{DD} and V_{SS} since at any point of time only one transistor is ON, but not both.
- When $V_{in} = 1$, the ON Resistance is 10 kΩ, when $V_{in} = 0$ the ON Resistance is 25 kΩ.

AreaCapacitancescalculations

From the concept of the transistors, we studied, it is apparent that as gate is separated from the channel by gate oxide an insulating layer, it has capacitance. Similarly, different interconnects run on the chip and each layer is separated by silicon dioxide.

Area capacitance can be calculated as $C = \dfrac{\varepsilon_o \varepsilon_{ins} A}{D}$ farads

Where

D = Thickness of silicon dioxide

A = Area of plates

ε_{ins} = Relative permittivity of SiO_2 = 4.0

ε_o = 8.85 X 10^{-14} F/cm (permittivity of free space)

The layer area capacitance is in $pF/\mu m^2$ (where μm = micron = 10^{-6} meter)

Typical values of area capacitance are given below in Fig. :

Value in pF $\times 10^{-4}/\mu m^2$ (Relative values in brackets).

Capacitance	5 µm		2 µm		1.2 µm	
Gate to channel	4	(1.0)	8	(1.0)	16	(1.0)
Diffusion (active)	1	(0.25)	1.75	(0.22)	3.75	(0.23)
Polysilicon* to substrate	0.4	(0.1)	0.6	(0.075)	0.6	(0.038)
Metal 1 to substrate	0.3	(0.075)	0.33	(0.04)	0.33	(0.02)
Metal 2 to substrate	0.2	(0.05)	0.17	(0.02)	0.17	(0.01)
Metal 2 to metal 1	0.4	(0.1)	0.5	(0.06)	0.5	(0.03)
Metal 2 to polysilicon	0.3	(0.075)	0.3	(0.038)	0.3	(0.018)

Standardunitofcapacitance:

A standard unit is employed that can be used in calculations. The unit is denoted as C_g and is defined as the gate-to-channel capacitance of a MOS transistor having W = L = feature size, that is a 'standard' or 'feature size' square.

C_g may be evaluated for any MOS process.

For example, for 5µm MOS circuits
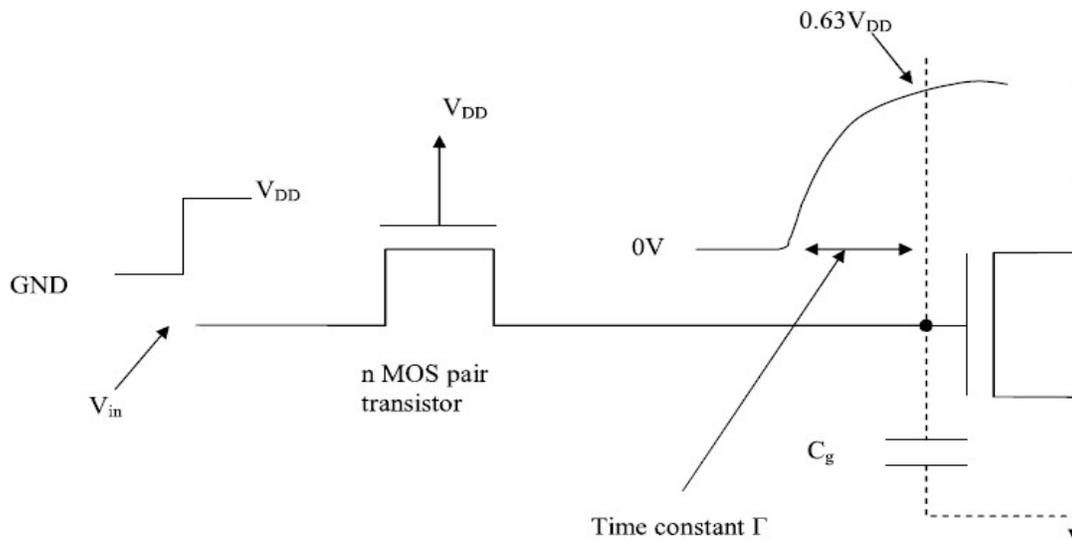
Area/standard square = 5µm X 5µm = $25\mu m^2$

Capacitance value $= 4 \times 10^{-4}$ pF/μm^2
Thus standard value of $C_g = 25 \ \mu m^2 \times 4 \times 10^{-4}$ pF/μm^2
$$= 0.01 \text{ pF}$$

For 2 μm MOS circuits $C_g = 0.0032$ pF and for 1.2 μm MOS circuits $C_g = 0.0023$ pF

CalculationofDelayunitτ

The delay unit Γ is the product of 1 R_s and 1 C_g

$$\Gamma = (1 \ R_s \ (\text{n-channel}) \times 1 \ C_g) \text{ seconds}$$

For 5μm technology
    $\Gamma = 10^4$ ohm X 0.01 pF
      $= 0.1$ n sec

For 2μm technology
    $\Gamma = 2 \times 10^4$ ohm X 0.0032 pF
      $= 0.064$ n sec

For 1.2μm (orbit) technology
    $\Gamma = 2 \times 10^4$ ohm X 0.0023 pF
      $= 0.046$ n sec

Practically $\Gamma = 0.2$ to 0.3 n sec for a 5μm technology because of circuit wiring and parasitic capacitances taken into account.

$$\tau \approx \tau_{sd} = \frac{L^2}{\mu_n V_{ds}} = \frac{25 \ \mu m^2 V \text{ sec}}{650 \ cm^2} \frac{}{3V} \ X \ \frac{10^9 \ n \sec cm^2}{10^8 \ \mu m^2}$$
$$= 0.13 \text{ n sec}$$

V_{ds} varies as C_g charges from 0 volts to 63% of V_{DD} in period Γ. Transit time and time constant Γ can be used inter changeably.
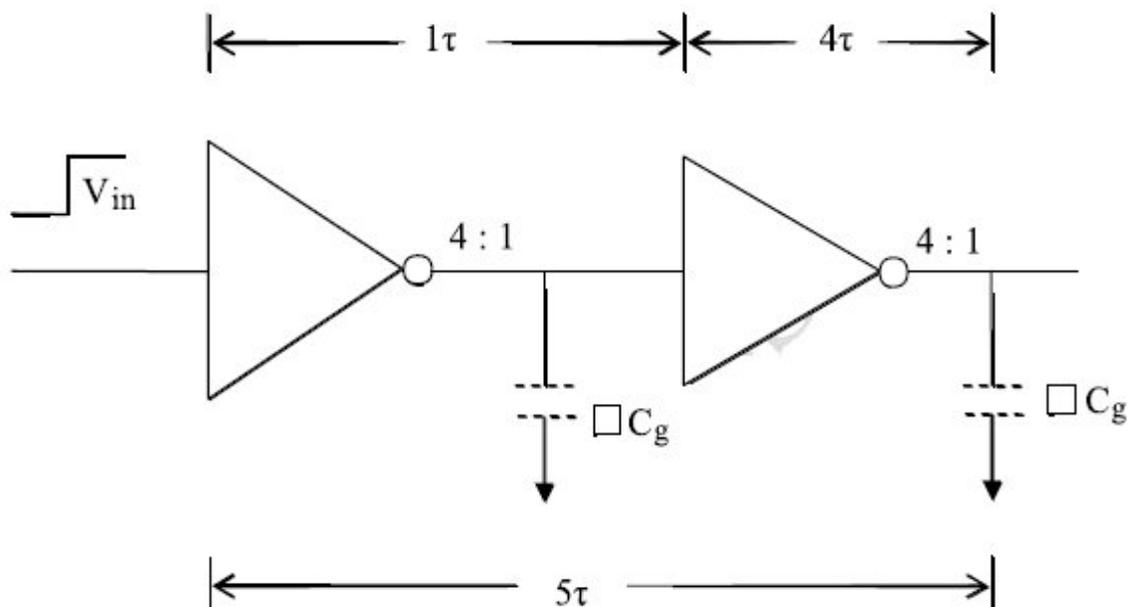
19

InverterDelays:

nMOS Inverter Pair Delay

Consider 4 : 1 ratio nMOS inverter. To get 4 : 1 Z_{pu} to Z_{pd} ratio, R_{pu} will be 4 R_{pd}

R_{pu} = 4 R_s = 40kΩ
Meanwhile R_{pd} = 1R_s = 10kΩ

Consider a pair of cascaded inverters, the delay over the pair is constant. This is observed in diagram below:

Assuming τ = 0.3 nsec, over all delay = $\tau + 4\tau = 5\tau$.

The general equation is $\tau_d = \left(1 + \dfrac{Z_{p.u}}{Z_{p.d}}\right)\tau$

Consider CMOS inverter, the nmos rule does not apply. The gate capacitance is

$2\,C_g$ Because the input is connected to both transistor gates.

Minimum Size CMOS Inveter Pair Delay

When considering CMOS inverters, the nMOS ratio rule no longer applies, but we must allow for the natural (R_s) asymmetry of the usually equal size pull-up p-transistors and the n-type pull-down transistors. Figure 5.21 shows the theoretical delay associated with a pair of minimum size (both n- and p-transistors) lambda-based inverters. Note that the gate capacitance (=2□C_g) is double that of the comparable nMOS inverter since the input to a CMOS inverter is connected to both transistor gates. Note also the allowance made for the differing channel resistances.

The asymmetry of resistance values can be eliminated by increasing the width of the p-device channel by a factor of two or three, but it should be noted that the gate input capacitance of the p-transistor is also increased by the same factor. This, to some extent, offsets the speed-up due to the drop in resistance, but there is a small net gain since the wiring capacitance will be the same.

Gate Level Design   □
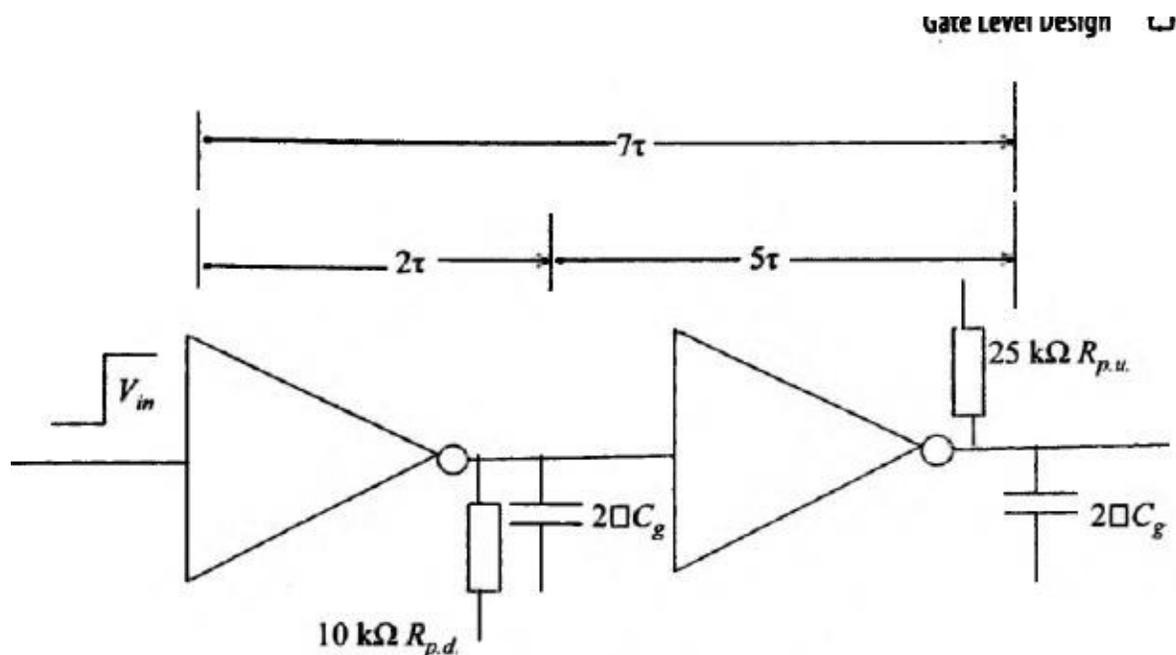
Fig. 5.21 Minimum size CMOS inverter pair delay.

FaninandFanout:

- Fan-In=Numberofinputsto alogicgate

  4inputNANDhasaFI=4

  2inputNORhasaFI =2,etc.(SeeFig.abelow.)

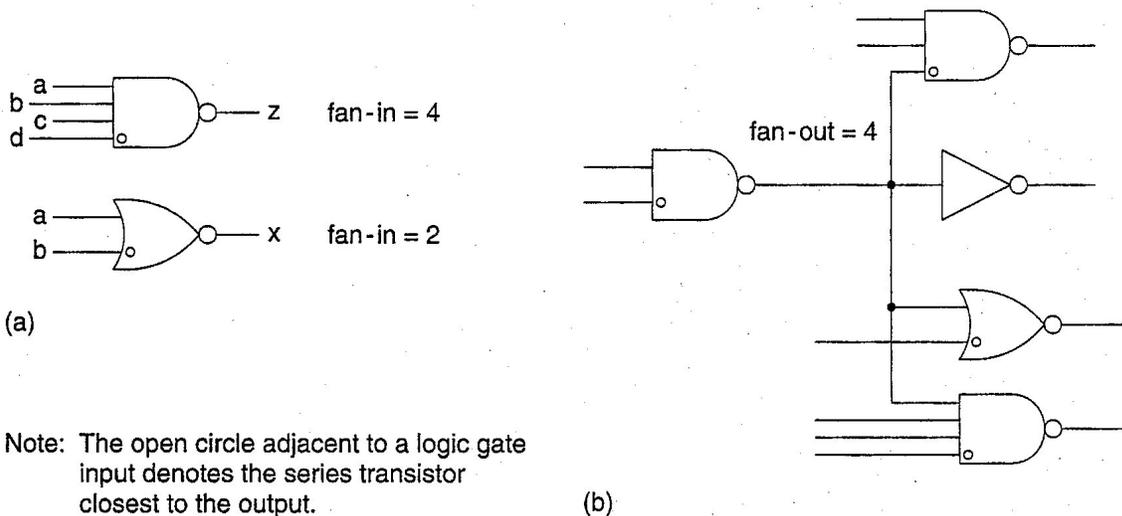- Fan-Out(FO)=Numberofgateinputswhicharedrivenbyaparticulargateoutput

  FO=4inFig.bbelowshowsanoutputwire feedinganinputonfourdifferent logic gates

- Thecircuit delayofagateisa functionofboththeFan-Inand theFan-Out. Ex.m-

  input NAND: $t_{dr}= (R_p/n)(mnC_d+ C_r+ kC_g)$

  $$=t_{internal-r}+kt_{output-r}$$

where n=widthmultiplier, m= fan-in, k= fan-out, Rp=resistanceofmin inverterPTx, Cg= gate capacitance, Cd = source/drain capacitance, Cr = routing (wiring) capacitance.
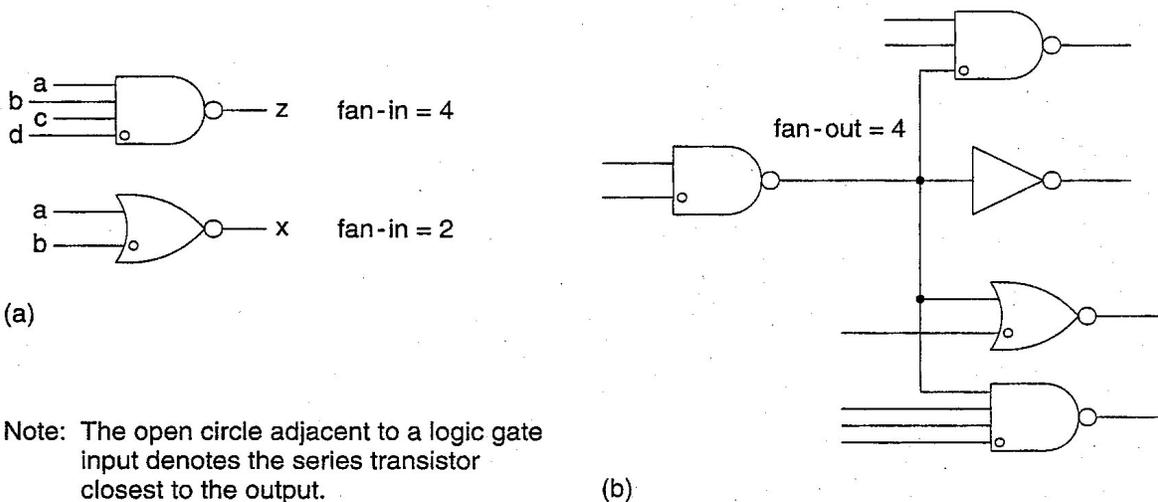

(a)

Note: The open circle adjacent to a logic gate
       input denotes the series transistor
       closest to the output.   (b)

•The circuit fall delay can be written in a similar manner.

Ex. m-input NAND: $\mathbf{t_{df} = m(R_n/n)(mnC_d + C_r + kC_g)}$

$$= \mathbf{t_{internal\text{-}f} + k\ t_{output\text{-}f}}$$

where n = width multiplier, m = fan-in, k = fan-out, Rn = resistance of min inverter NMOS Tx, Cg = gate capacitance, Cd = source/drain capac, Cr = routing (wiring) capac.

If we set $t_{dr} = t_{df}$ for the case of symmetrical rise and fall delay, we obtain that Rp = m Rn and therefore,

$$\mathbf{\beta_p W_p = (\beta_n W_n)/m}$$

(a)

Note: The open circle adjacent to a logic gate
       input denotes the series transistor
       closest to the output.   (b)

Summary

1. The **sheet resistance** is a measure of resistance of thin films that have a uniform thickness. It is commonly used to characterize materials made by semiconductor doping, metal deposition, resistive paste printing, and glass coating.
2. The resistance of the MOS layers depends on the thickness and the material of the layer. The resistance value of any square pattern is same as $W = L$.
3. Standard unit of capacitance is defined as gate to channel capacitance of a MOS transistor having $W = L$ = feature size that is standard.
4. Time constant $\tau = (1R_s\ (n\ \text{channel}) \times 1\ \square C_g)$ seconds.

AssignmentQuestions:

1. Describethefollowing:

   a) Pseudo-nMOSLogic

   b) DominoLogic.

2. Discussaboutthelogicsimplementedingate leveldesignandexplaintheswitchlogic implementation for a four way multiplexer.

3. Describeaboutthemethodsfordriving largecapacitiveloads.

4. Describeaboutthechoiceoffan–inandfan–outselectioningateleveldesign.

5. What arethealternategatecircuitsavailable?Explainanyoneofitemwithsuitable sketch by taking NAND gate as an example.

6. ExplaintheTransmissiongateandTristateinverterlogic.

7. DescribethenMOSandCMOSinverterpairdelays.