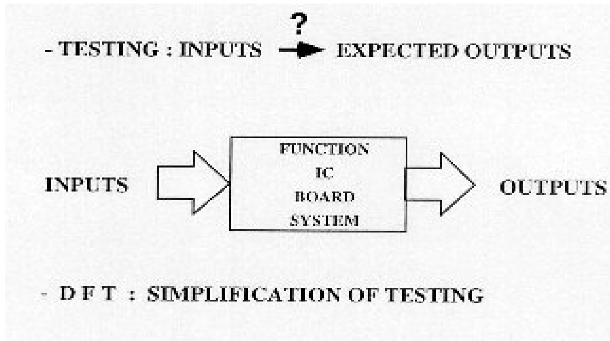
UNIT-V
CMOSTESTING

Needfortesting

Designof logic integratedcircuits inCMOS technologyis becoming moreand morecomplex since VLSI is the interest of many electronic IC users and manufacturers. A common problem to be solved by both users and manufacturers is the testing of these ICs.



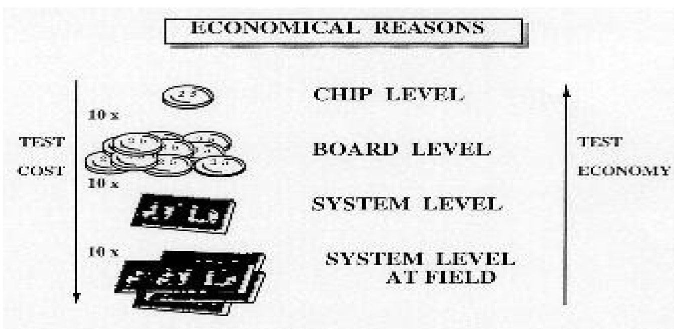
Testing can be expressed by checking if the outputs of a functional system (functional block, Integrated Circuit, Printed Circuit Board or a complete system) correspond to the inputs applied to it. If thetest of this functional system is positive, then thesystem is good for use. If the outputs are different than expected, then the system has a problem: so either the system is rejected (Go/No Go test), or a diagnosis is applied to it, in order to point out and probably eliminate the problem's causes.

Testing is applied to detect faults after several opera

tions : design, manufacturing, packaging and especiallyduringtheactivelifeof a system, andthus sincefailures causedbywear-out canoccur at any moment of its usage.
Design for Testability (DFT) is the ability of simplifying the test of any system. DFT could be synthesized by a set of techniques and design guidelines where the goals are :

- minimizingcostsofsystemproduction
- minimizingsystemtestcomplexity:testgenerationandapplication
- improvingquality
- Avoidingproblemsoftimingdiscordanceor blocknatureincompatibility.

Intheproductionprocess cycle, a fault canoccur atthe chip level. If a test strategyis consideredat the beginning of the design, then the fault could be detected rapidly, located and eliminated at a very low cost. When the faulty chip is soldered on a printed circuit board, the cost of fault remedy would be multiplied by ten. And this cost factors continues to apply until the system has been assembled and packaged and then sent to users.



ManufacturingTests:

Whereas verification or functionality tests seek to confirm the function of a chip as a whole, manufacturing tests are used to verify that every gate operates as expected. The need to do this arises from a number of manufacturing defects that might occur during either chip fabrication or accelerated lifetesting (wherethechip is stressed by over-voltageand over-temperatureoperation). Typical defects include the following:

- Layer-to-layershorts(e.g.,metal-to-metal)
- Discontinuouswires(e.g.,metalthinswhencrossingverticaltopologyjumps)
- Missingordamagedvias
- Shorts through the thin gate oxide to the substrate or well

Theseinturnleadtoparticular circuitmaladies, includingthefollowing

- Nodesshortedtopower orground
- Nodesshortedtoeachother
- Inputsfloating/outputsdisconnected

Tests are required to verify that each gate and register is operational and has not been compromised by a manufacturing defect. Tests can be carried out at the wafer level to cull out bad dies, or can be left until the parts are packaged. This decision would normally be determined by the yield and package cost. If the yield is high and the package cost low (i.e., a plastic package), then the part can be tested only once after packaging. However, if the wafer yield was lower and the package cost high (i.e., an expensive ceramic package), it is more economical to first screen bad dice at the wafer level. The length of the tests at the wafer level can be shortened to reduce test time based on experience with the test sequence.

Apart from the verification of internal gates, I/O integrity is also tested, with the followingtests being completed:

- I/Olevels(i.e., checkingnoisemarginforTTL,ECL, orCMOSI/O pads)
- Speedtest

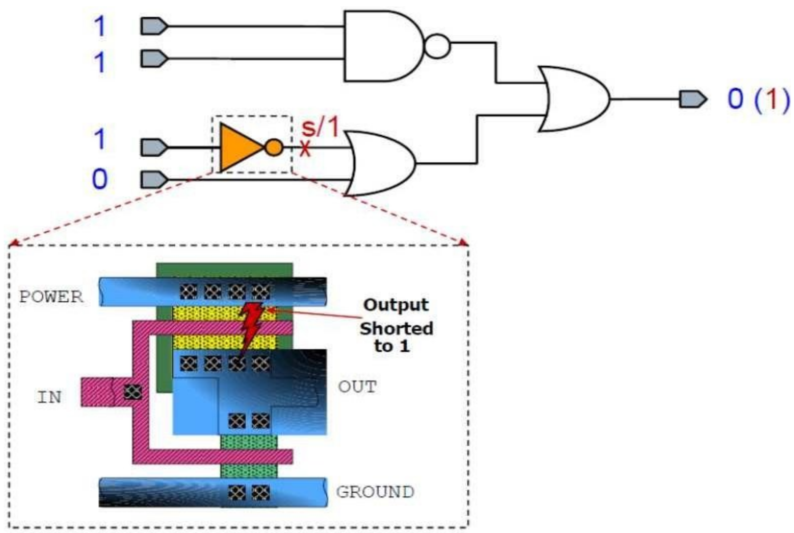
With the use of on-chip test structures described here, full-speed wafer testing can be completed witha minimumofconnectedpins. This can beimportant inreducingthecost ofthe wafer test fixture.

In general, manufacturing test generation assumes the function of the circuit/chip is correct. It requires ways of exercising all gate inputs and monitoring all gate outputs.

Test Principles: Thepurpose of manufacturingtest is toscreen out most of thedefectiveparts beforetheyareshippedtocustomers. Typicalcommercialproducts target a defect rateof350– 1000 defects per million (DPM) chips shipped.

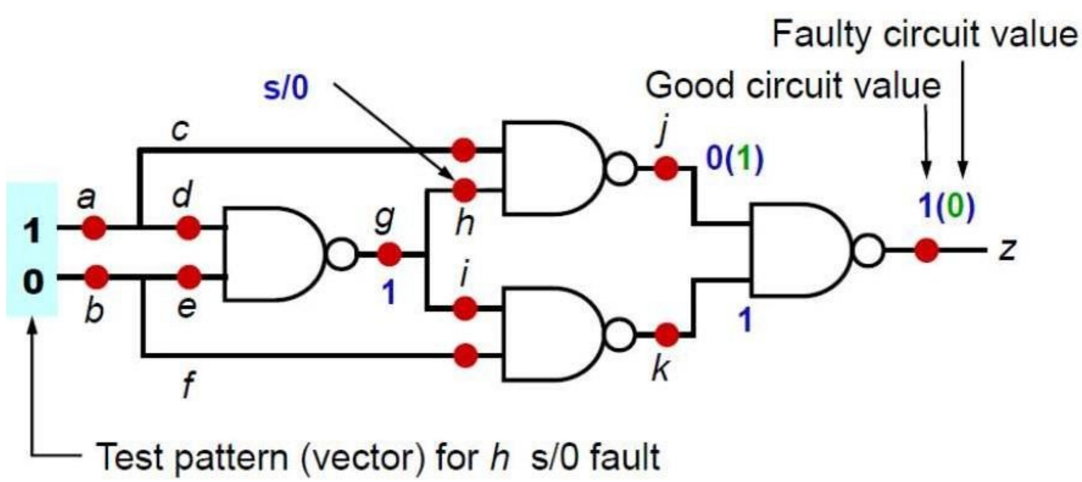
FaultModels

To deal with the existence of good and bad parts, it is necessary to propose a fault model; i.e., a model for how faults occur and theirimpact on circuits. The most popular modelis called the Stuck-Atmodel. The Short Circuit/ Open Circuit model can be a closer fit to reality,butisharder to incorporate intologic simulation tools.



Stuck-At Faults In the Stuck-At model, a faulty gate input is modeled as a stuck at zero (Stuck-At-0, S-A- 0) or stuck at one (Stuck-At-l, S-A-l). This model dates from board-level designs,whereitwasdeterminedtobeadequateformodelingfaults.Figureillustrateshow an S-A-0 or S-A-1 fault might occur. These faults most frequently occur due to gate oxideshorts(the nMOSgate to GNDorthe pMOSgate to VDD)ormetal-to-metal shorts.

Short-Circuit and Open-Circuit Faults Other models include stuck-open or shorted models. Two bridging or shorted faults are shown in Figure. The short S1 results in an S-A-0 fault at inputA,while short S2modifiesthe function of the gate.



It is evident that to ensure the most accurate modeling, faults should be modeled at the transistor level because it is only at this level that the complete circuit structure is known. For instance, in the case of a simple NAND gate, the intermediate node between the series nMOS transistors is hidden by the schematic. This implies that test generation should ideally take accountof possible shorts andopencircuits at the switch level. Expediencydictatesthatmost existingsystemsrelyonBooleanlogicrepresentationsofcircuitsandstuck-atfaultmodeling.

Observability

The observability of aparticularcircuit node is the degree towhich youcan observe that nodeat the outputs of an integrated circuit (i.e., thepins). This metric is relevant when you want to measure the output of a gate within a larger circuit to check that it operates correctly. Given the limited number of nodes that can be directly observed, it is the aim of good chip designers to have easily observed gate outputs. Adoption of some basic design for test techniques can aid tremendously in this respect. Ideally, you should be able to observe directly or with moderate indirection (i.e., you may have to wait a few cycles) every gate output within an integrated circuit. While at one time this aim was hindered by the expense of extra test circuitryand alack ofdesignmethodology,currentprocessesanddesignpracticesallowyou to approach this ideal.

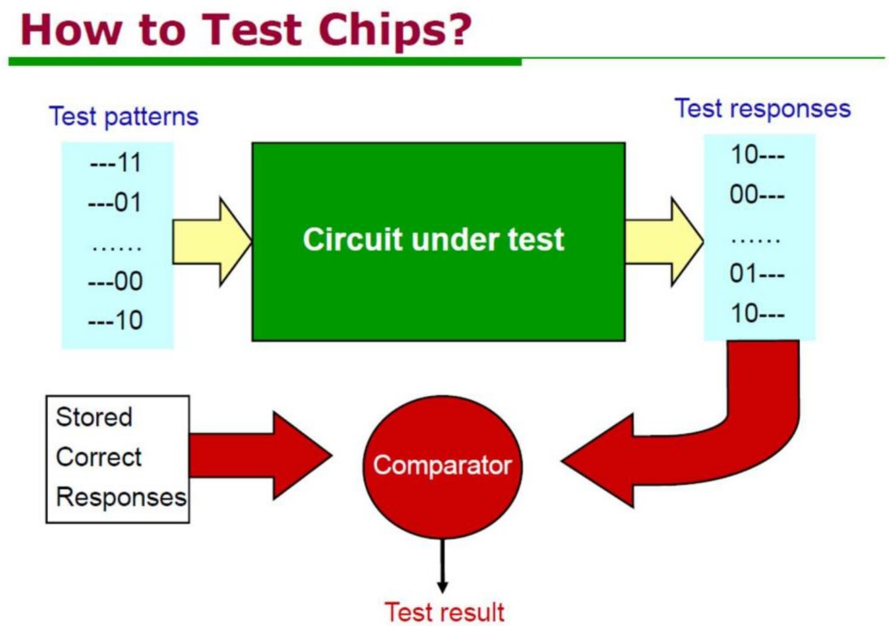
Controllability

The controllability of an internal circuit node within a chip is a measure of the ease of setting the node to a 1 or 0 state. This metric is of importance when assessing the degree of difficulty of testing a particular signal within a circuit. An easily controllable node would be directly settable via an input pad. A node with little controllability, such as the most significant

bit of a counter, might require many hundreds or thousands of cycles to get it to theright state. Often, you will find it impossible to generate a test sequence to set a number of poorly controllable nodes into the right state. It should be the aim of good chip designers to make all nodeseasily controllable.In common with observability, the adoption of some simple design for test techniques can aid in this respect tremendously. Making all flip-flops resettable via a global resetsignal isone steptoward good controllability.

FaultCoverage

A measure of goodness of a set of test vectors is the amount of fault coverage it achieves. That is, for the vectors applied, what percentages of the chip's internal nodes werechecked? Conceptually, the way in which the fault coverage is calculated is as follows. Eachcircuitnodeistakeninsequenceandheldto0(S-A-0),andthecircuitissimulated withthetestvectorscomparingthechipoutputswithaknowngoodmachine—acircuitwith nonodes artificiallysetto0(or1).Whenadiscrepancyisdetectedbetweenthefaulty machine and thegood machine, the fault is marked as detected and the simulation is stopped. Thisisrepeatedforsettingthenodeto1(S-A-1).Inturn,everynodeisstuck(artificially)at 1 and 0 sequentially. The fault coverage of a set of test vectors is the percentage of the total nodesthatcanbedetectedasfaultywhenthevectorsareapplied.Toachieveworld-class qualitylevels,circuitsarerequiredtohaveinexcessof98.5%faultcoverage.The Verification MethodologyManual is the bible for fault coverage techniques.



IDDQ TESTING: It is a simple method to identify defects on IC on the steady state power supply current. It is also a method for testing CMOS integrated circuits for the presence of manufacturing faults. It relies on measuring the supplycurrent (Idd) inthe quiescent state (whenthecircuitisnotswitchingand inputsareheldat staticvalues).The currentconsumed in the state is commonly called Iddq for Idd (quiescent) and hence the name. Iddq testing uses the principle that in a correctly operating quiescent CMOS digital circuit, there is no static current pathbetweenthepower supplyandground, except for a smallamount of leakage. Many common semiconductor manufacturing faults will cause the current to increase by orders of magnitude, which can be easily detected. This has the advantage of checking the chip for many possible faults with one measurement.Another advantage is that itmay catch faultsthatarenot found by conventional stuck-at fault test vectors. Iddq testing is somewhat more complex thanjust measuringthesupplycurrent. If a lineis shortedto Vdd, for example, it will still draw no extra current if the gate driving the signal is attempting to set it to '1'. However, a different vector set that attempts to set the signal to 0 will show a large increase in quiescent current, signalinga badpart.TypicalIddqtest vector sets may have20 or sovectors.NotethatIddqtest vectors require only controllability, and not observability. This is because the observability is through the shared power supply connection. Iddq testing has many advantages:

- □ Itisasimpleanddirecttestthatcanidentifyphysicaldefects.
- □ Theareaanddesigntimeoverheadareverylow.
- □ Testgenerationisfast.

□ Testapplicationtimeisfastsincethevectorsetsaresmall.

□ Itcatchessomedefectsthatothertests,particularlystuck-atlogictests,donot.

Drawback:Comparedtoscantesting, Iddq testingis time consuming, andthen more expensive, since is achieved by currentmeasurementsthat take muchmore time than reading digital pins in mass production.

AUTOMATICTESTPATTERNGENERATION(ATPG)

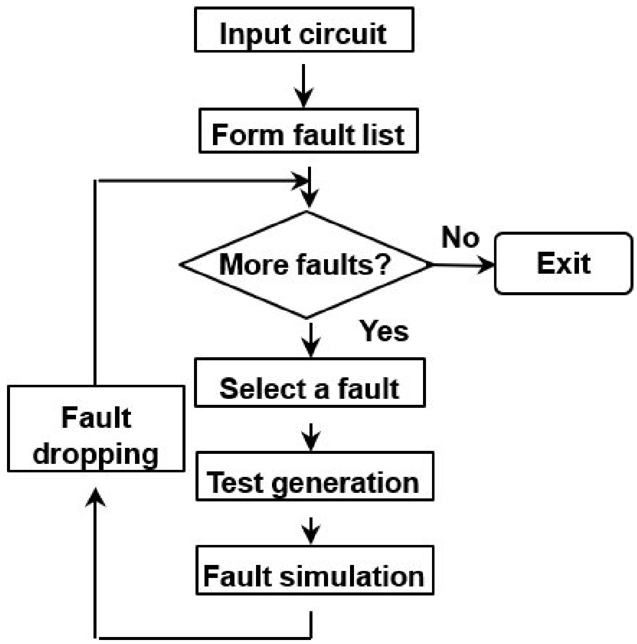
Historically,in the ICindustry,logicandcircuitdesignersimplementedthe functions at the RTL or schematic level, mask designers completed the layout, and test engineerswrote the tests. In many ways, the test engineers were the Sherlock Holmes of the industry, reverse engineering circuits and devising tests thatwould test the circuitsin an adequate manner. For the longest time, test engineers implored circuit designers to include extra circuitry to ease the burden of test generation. Happily, as processes have increased in density and chips have increased in complexity, the inclusion of test circuitry has become less of an overhead for both the designer and the manager worried about the cost of the die. In addition, as tools have improved, more of the burden for generating tests has fallen on the designer. To deal with this burden, Automatic Test Pattern Generation (ATPG) methods have been invented. The use of some form of ATPGisstandard formostdigital designs.

It is the process of generating test patterns for a given fault model. If we go by exhaustive testing, in the worst case, we may require 2n (where n stands for no. of primary inputs) assignments to be applied for finding test vector for a single stuck-at fault. It is impossible for us to manually use exhaustive testing or path sensitization method to generate a test pattern forchips consisting ofmillions of transistors. Hence,we need an automated process,a.k.a.Automatic TestPattern Generation(ATPG).

A cycle of ATPG can generally be divided into two distinct phases: 1) creation of the test; and 2) application of the test.During the creation of the test, appropriate models for the device circuitare developed atgateortransistorlevelin such away thattheoutput responses of a faulty device for a given set of inputs will differ from those of a good device. This generationoftestisbasicallyamathematicalprocessthatcanbedoneinthreeways:

1)bymanualmethods;2)byalgorithmicmethods(withorwithoutheuristics);and
3) by pseudo-random methods. The software used for complex ATPG applications are quite expensive, but the process of generating a test needs to be done only once at the end of the design process.

When creating a test, the goal should be to make it as efficient in memory space and timerequirementsasmuchaspossible.Assuch,theATPGprocessmustgeneratethe minimum or near minimum set of vectors needed to detect all the important faults of a device. The main considerations for test creation are: 1) the time needed to construct the minimal test set; 2) the size of the pattern generator, or hardware/software system needed to properly stimulate the devices under test; 3) the size of the testing process itself; 4) the time needed to load the testpatterns; and5) theexternalequipmentrequired(ifany).



DESIGNSTRATEGIESFORTEST,

Design for Testability The keys to designing circuits that are testable are controllability and observability. Restated, controllability is the ability to set (to 1) and reset (to 0) every node internal to the circuit. Observability is the ability to observe, either directly or indirectly, the state of any node in the circuit. Good observability and controllability reduce the cost of manufacturing testing because they allow high fault coverage with relatively few test vectors. Moreover, theycanbe essential to silicondebug because physicallyprobinginternal signals has become so difficult.

We will first cover three main approaches to what is commonly called Design for Testability (DFT). Thesemay be categorizedasfollows:

Ad hoctesting

Scan-based approaches

Built-inself-test(BIST)

AdHocTesting

Ad hoc test techniques, as their name suggests, are collections of ideas aimed atreducing the combinational explosion of testing. They are summarized here for historical reasons. They areonly useful for small designs where scan, ATPG, and BIST are not available. A complete scan-based testing methodology is recommended for all digital circuits.Havingsaidthat, the following are commontechniquesfor ad hoc testing:

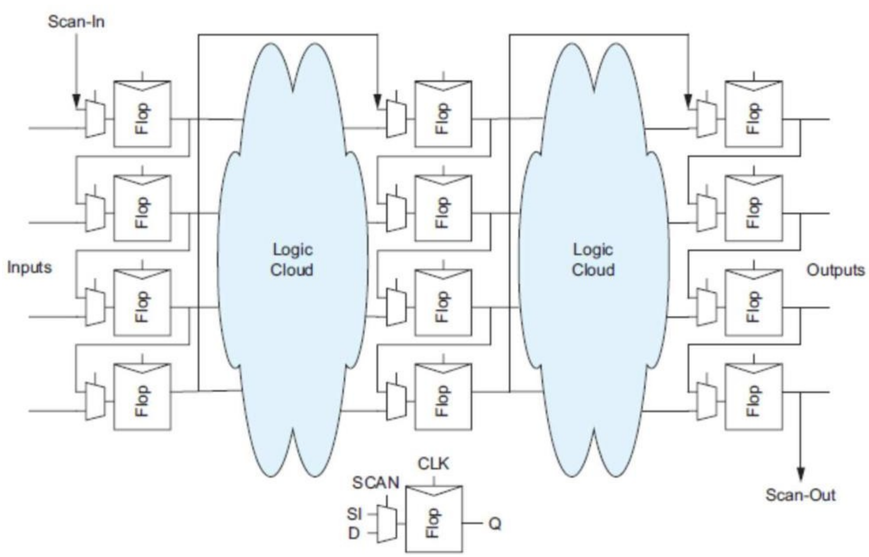
- Partitioninglargesequentialcircuits
- Addingtestpoints
- Addingmultiplexers
- Providingforeasy
- statereset

A technique classified in this category is the use of the bus in a bus-oriented system for test purposes. Each register has been made loadable from the bus and capable of being driven onto the bus.Here,theinternallogicvaluesthatexistonadatabus areenabledonto thebus for testing purposes. Frequently, multiplexers can be used to provide alternative signal paths during testing. In CMOS, transmission gate multiplexers provide low area and delay overhead. Anydesignshouldalwayshaveamethodofresettingtheinternalstateofthechipwithina single cycle or at most a few cycles. Apart from making testing easier, this also makes simulation faster as a few cycles are required to initialize the chip.

In general, ad hoc testing techniques represent a bag of tricks developed over the years by designers to avoid the overhead of a systematic approach to testing, as will be described in the next section. While these general approaches are still quite valid, process densities and chip complexities necessitate a structured approach to testing.

SCANBASEDTECHNIQUE

The scan-design strategy for testing has evolved to provide observability and controllability at each register. In designs with scan, the registers operate in one of two modes. In normal mode, they behave as expected.In scan mode, they are connected to form a giantshift register called a scan chain spanning the whole chip. By applying N clock pulses in scan mode, all N bits of state in the system can be shifted out and new N bits of state can be shifted in. Therefore, scan mode gives easy observability and controllability of every register in the system.



Modern scan is based on theuse of scan registers, as shown in Figure. Thescan register is a D flip-flop preceded by a multiplexer. When the SCAN signal is deasserted, the register behaves as a conventional register, storing data on the D input. When SCAN is asserted, thedata is loaded from the SI pin, which is connected in shift register fashion to the previous register Q output in thescan chain. For thecircuit to load thescan chain, SCAN is asserted and CLKispulsedeighttimestoloadthefirsttworanksof4-bitregisterswithdata.SCANis deasserted and CLK is asserted for one cycle to operate the circuit normally with predefined inputs. SCANisthen reasserted andCLK assertedeighttimesto readthe stored data out. At the same time, the new register contents can be shifted in for the next test. Testing proceeds in this manner ofseriallyclockingthedatathroughthescanregister totheright pointinthecircuit, running a single system clock cycle and serially clocking the data out for observation. In this scheme, every input to the combinational block can be controlled and every output can be observed.Inaddition,runningarandom patternof1sand0sthrough the scanchaincantest the chain itself.

Test generation for this type of test architecture can be highly automated. ATPG techniques can be used for the combinational blocks and, as mentioned, the scan chain is easily tested. The prime disadvantage is the area and delay impact of the extra multiplexer in the scan register.Designers(andmanagersalike) are in widespread agreementthatthiscost ismore than offset by the savings in debug time and production test cost.

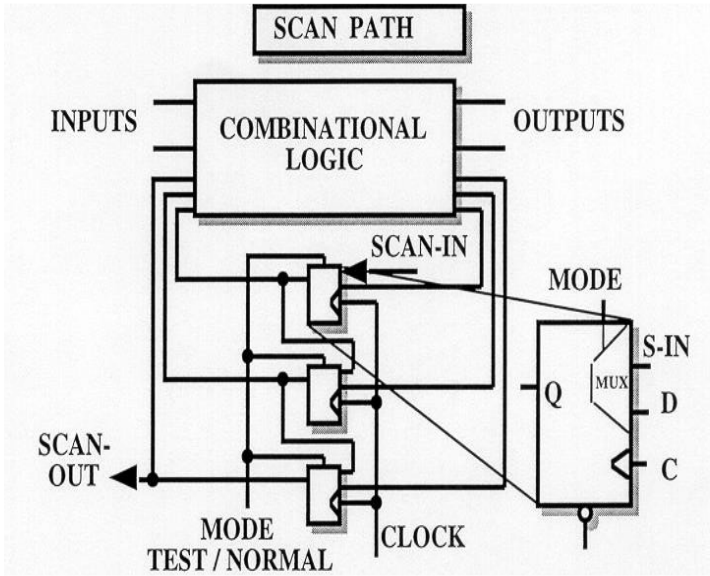
ScanDesignTechniques

Theset of designfor testability guidelines presentedaboveis a set of adhoc methods to design random logic in respect with testability requirements. The scan design techniques are a set of structured approaches to design (for testability) the sequential circuits.

The major difficulty in testing sequential circuits is determining the internal state of the circuit. Scandesigntechniques aredirectedat improvingthecontrollabilityandobservability of the internal states of a sequential circuit. By this the problem of testing a sequential circuit is reducedtothat oftestinga combinationalcircuit, sincetheinternalstates ofthecircuit areunder control.

8.8.1ScanPath

Thegoal ofthescanpathtechniqueis toreconfigurea sequentialcircuit, for thepurpose of testing, into a combinational circuit. Since a sequential circuit is based on a combinational circuit andsome storageelements, thetechniqueof scanpathconsists inconnectingtogether all thestorage elements to forma long serial shift register. Thus theinternal state of thecircuit can be observed and controlled by shifting (scanning) out the contents of the storage elements. The shift register is then called a scan path.



Thestorage elements can either beD, J-K, or R-S types of flip-flops, but simple latches cannot beused inscanpath. However, thestructureof storageelements is slightlydifferent than classical ones. Generallytheselectionof theinput sourceis achievedusinga multiplexer onthe data input controlled by an external mode signal. This multiplexer is integrated into the D-flip- flop, in our case; the D-flip-flop is then called MD-flip-flop (multiplexed-flip-flop).

The sequential circuit containing a scan path has two modes of operation : a normal mode and a test mode which configure the storage elements in the scan path.

In the normal mode, the storage elements are connected to the combinational circuit, in the loops of the global sequential circuit, which is considered then as a finite state machine.

In the testmode, the loops are broken and the storage elements are connected togetheras a serial shift register (scan path), receiving the same clock signal. The input of the scan path is called scan-in and the output scan-out. Several scan paths can be implemented in one same complex circuit if it is necessary, though having several scan-in inputs and scan-out outputs.

A large sequential circuit can be partitioned into sub-circuits, containing combinational sub-circuits, associated with one scan path each. Efficiency of the test pattern generation for a combinational sub-circuit is greatly improved by partitioning, since its depth is reduced.

Before applying test patterns, the shift register itself has to be verified by shifting in all ones i.e. 111...11, or zeros i.e. 000...00, and comparing.

Themethodoftestingacircuit withthescanpathis asfollows:

1. Settestmodesignal,flip-flopsacceptdatafrominputscan-in

2. Verifythescanpathbyshiftinginandouttestdata

3. Settheshiftregistertoaninitialstate

4. Applyatest patterntotheprimaryinputsofthecircuit

5. Setnormalmode,thecircuitsettlesandcanmonitor theprimaryoutputsofthecircuit

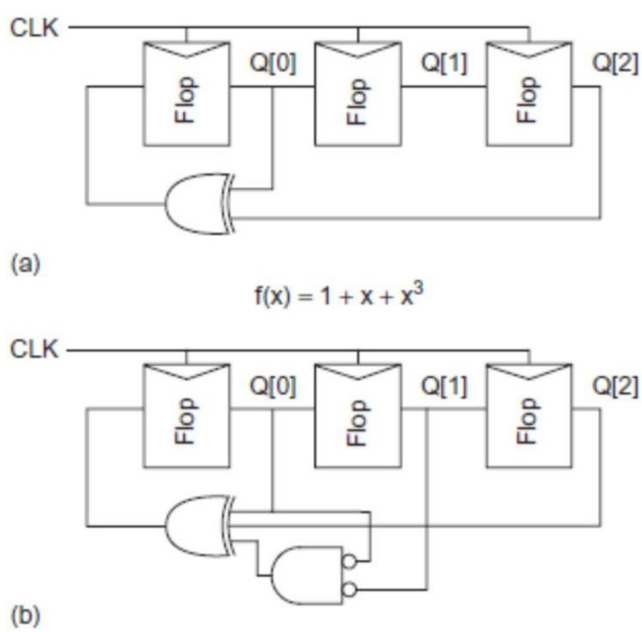
6. Activatethecircuitclockforonecycle

7. Returntotestmode

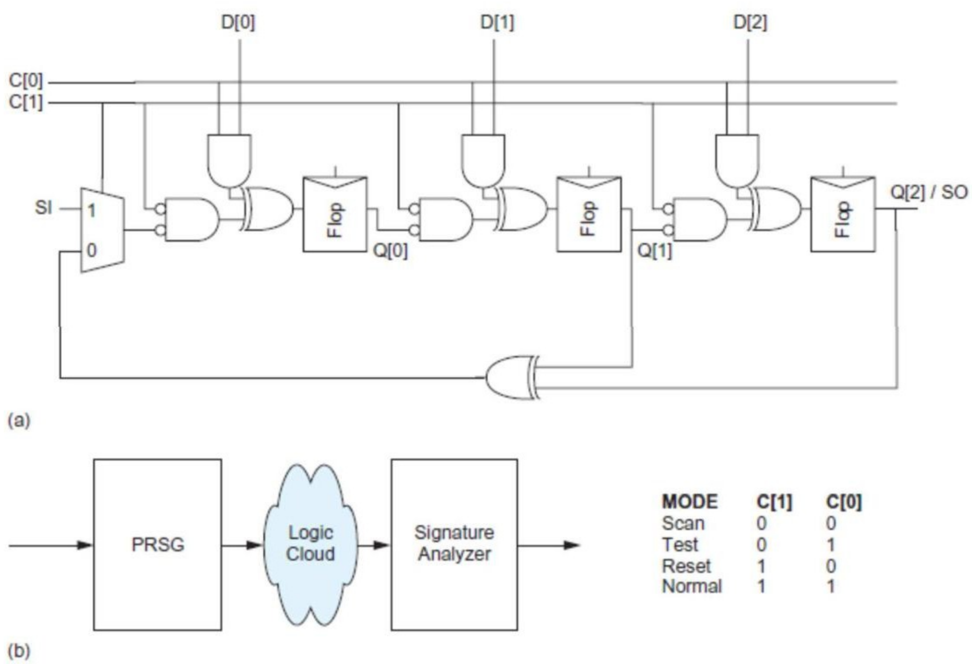
8. Scanout thecontentsoftheregisters,simultaneouslyscaninthenext pattern

SELF-TESTAPPROACHES:BUILT-INSELF-TEST(BIST)

Self-test andbuilt-intest techniques, astheir names suggest, relyonaugmentingcircuits to allow them to perform operations upon themselves that prove correct operation. These techniques add area to the chip for the test logic, but reduce the test time required and thus can lower the overall system cost. [Stroud02] offers extensive coverage of the subject from the implementer's perspective.

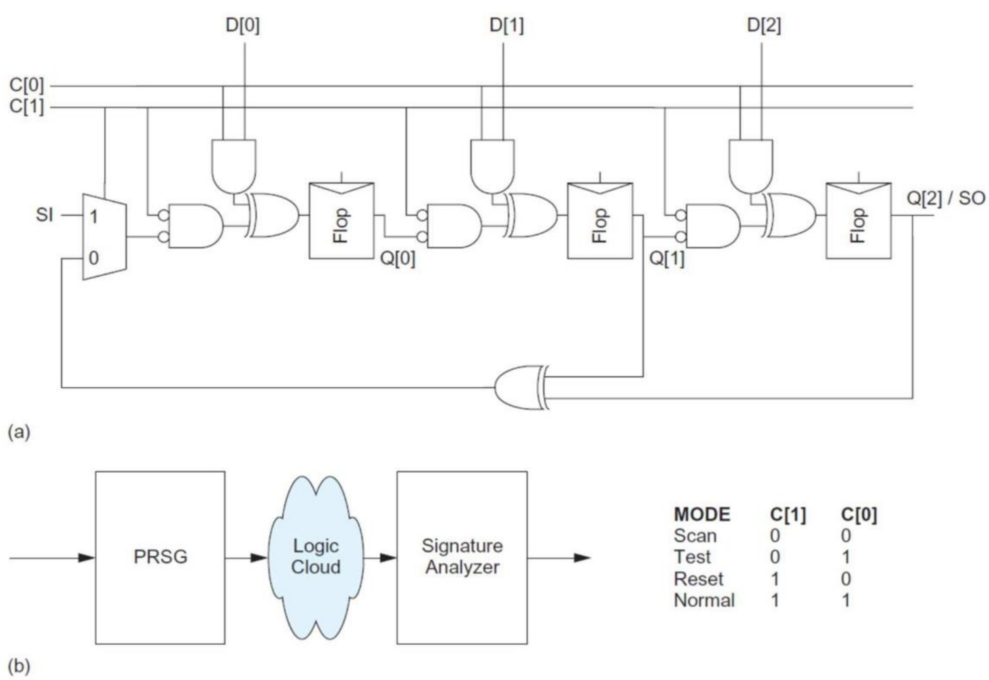


One method of testing a module is to use signature analysis or cyclic redundancy checking. This involves using a pseudo-random sequence generator (PRSG) toproduce the input signals for a section of combinational circuitry and a signature analyzer to observe the output signals. A PRSG of length n is constructed froma linear feedback shift register (LFSR), which in turn is made of n flip-flops connected in a serial fashion, as shown in Figure (a). The XOR of particular outputs are fed back to the input of the LFSR. An n-bit LFSR will cycle through 2n–1statesbefore repeating the sequence.LFSRs are discussedfurtherin Section They are described by a characteristic polynomial indicating which bits are fed back. A complete feedback shift register (CFSR), shown in Figure (b), includes the zero state that may be required in some testsituations.An n-bitLFSRis converted to an n-bitCFSR by adding ann – 1 input NOR gate connected to all but the last bit. When in state 0…01, the next state is 0…00. When in state 0…00, the next state is 10…0. Otherwise, the sequence is the same. Alternatively, the bottom n bits of an n + 1-bit LFSR can be used to cycle through the all zeros state without the delay of the NOR gate.



A signature analyzer receives successive outputs of a combinational logic block and produces a syndrome that is a function of these outputs. The syndrome is reset to 0, and then XORed with the output on each cycle. The syndrome is swizzled each cycle so that a fault in one bit is unlikely to cancel itself out. At the end of a test sequence, the LFSR contains the syndromethatisafunctionofallpreviousoutputs.Thiscanbecomparedwiththecorrect syndrome (derived by running a test program on the good logic) to determine whetherthe circuit is good or bad. If the syndrome contains enough bits, it is improbable that a defective circuit will produce the correct syndrome.

The combination of signature analysis and the scan technique creates a structure known as BIST—for Built-In Self-Test or BILBO—for Built-In Logic Block Observation The 3-bit BIST register shown in Figure is a scannable, resettable register that also can serve as a pattern generator and signature analyzer. C[1:0] specifies the mode ofoperation.In the resetmode (10), all the flip-flops are synchronously initialized to 0.In normal mode (11), the flip-flops behave normally with their D input and Q output. In scan mode (00), the flip-flops are configured as a 3-bit shift register between SI and SO. Note that there is an inversion between each stage. In test mode (01), the register behaves as a pseudo- random sequence generator or signatureanalyzer. IfalltheD inputs areheldlow, theQ outputs loop througha pseudo-random bit sequence, which can serve as the input to the combinational logic. If the D inputs are taken from the combinational logic output, they are swizzled with the existing state to produce the syndrome. Insummary, BIST isperformedbyfirstresettingthe syndrome intheoutput register. Then both registers are placed in the test mode to produce the pseudo-random inputs and calculate the syndrome. Finally, the syndrome is shifted out through the scan chain.



Various companies have commercial design aid packages that automatically replace ordinary registers with scannable BIST registers, check the fault coverage, and generate scripts for production testing. As an example, on a WLAN modem chip comprising roughly 1 million gates, a full at-speed test takes under a second with BIST. This comes with roughly a 7.3% overhead in the core area (but actually zero because the design was pad limited) and a 99.7% fault coverage level. The WLANmodem parts designed in this way were fully tested in less than ten minutes on receipt of first silicon. This kind of test method is incredibly valuable for productivity in manufacturing test generation.

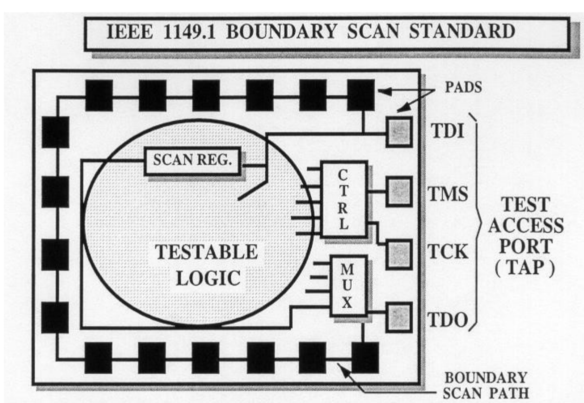
MemoryBIST

On many chips, memories account for the majority of the transistors. A robust testing methodology must be applied to provide reliable parts. In a typical MBIST scheme,multiplexers are placed on the address, data, and control inputs for the memory to allow direct access during test. During testing, a state machine uses these multiplexers to directly write a checkerboard pattern of alternating 1s and 0s. The data is read back, checked, then the inverse pattern isalso applied and checked.ROMtestingiseven simpler:Thecontentsare read outto a signature analyzer to produce a syndrome.

BoundaryScanTest(BST)

Boundary Scan Test (BST) is a technique involving scan path and self-testingtechniques to resolve the problem of testing boards carrying VLSI integrated circuits and/or surface mounted devices (SMD).

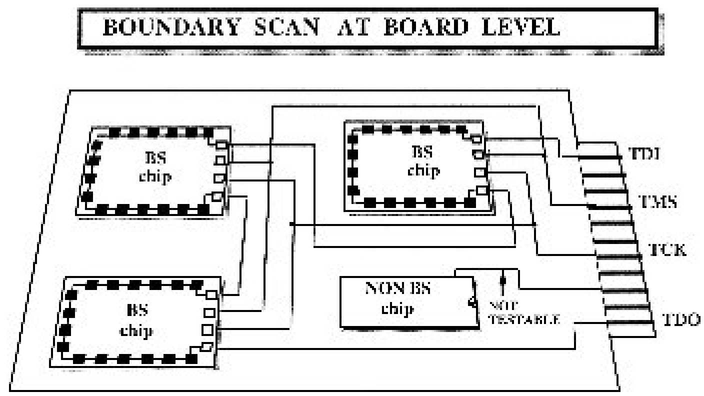
Printed circuit boards (PCB) are becoming very dense and complex, especially with SMD circuits, that most test equipment cannot guarantee a good fault coverage.



BST consists in placing a scan path (shift register) adjacent to each component pin and to interconnect the cells in order to form a chain around the border of the circuit. The BST circuits contained on one board are then connected together to form a single path through the board.

Theboundaryscanpathisprovidedwithserialinputandoutputpadsandappropriate clockpadswhichmakeit possibleto:

- Testtheinterconnectionsbetweenthevarious chip
- Delivertestdatatothechipsonboardforself-testing
- Testthechipsthemselveswithinternalself-test



TheadvantagesofBoundaryscantechniquesareasfollows:

- NoneedforcomplextestersinPCBtesting
- Testengineersworkissimplifiedandmoreefficient
- Timetospendontest patterngenerationandapplicationis reduced
- Faultcoverageisgreatlyincreased.

BS Techniques are grouped by the IEEE Standard Organization in a "standard testaccess port andboundaryscanarchitecture", namelyIEEEP1149.1-1990.TheJoint Test Action Group (JTAG), formed basically in 1986 at Philips, is an international committee composed of IC manufacturers who have set the technical development of the IEEE P1149 standard and promoted its use by all sectors of electronics industry.

TheIEEE 1149 is a family of overall testability bus standards, defined by theJoint Test Action Group (JTAG), formed basically in 1986 at Philips. JTAG is an international committee composed of European and American IC manufacturers. The "standard Test Access Port and Boundary Scan architecture", namely IEEE P1149.1 accepted by the IEEE standard committee in February1990, is the first one of this family. Several other ongoing standards are developed and suggested as drafts to the technical committee of the IEEE 1149 standard in order to promote their use by all sectors of electronics industry.